PM10025A Datasheet

Motor MCU with 48Mhz ARM Cortex-M0

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Contents

1 Introduction

This document is the datasheet of PM10025 series. PM10025 series are motor-specific MCU developed by Panjit. The part numbers are listed below：

- **PM10025A(TSSOP28)**
- **PM10025NT(QFN32)**
- **PM10025PT(LQFP32）**
- **PM10025NF(QFN48)**
- **PM10025PF(LQFP48)**

Users can refer to the 'PM10025 User Manual' for detailed information on its functions.

2 Product Description

The PM10025 microcontrollers incorporate the high-performance Arm® Cortex®-M0 32-bit RISC core at 48Mhz frequency, embedded 32 Kbyte Flash and 4 Kbyte SRAM.

All devices offer one 16-bit advanced timer (with three asymmetric dead-zone non-overlapping complementary PWM outputs), one 32-bit general-purpose timer, one 16-bit general-purpose timer, and one 16-bit basic timer.

The PM10025 microcontrollers integrate one built-in simple RTC, support one alarm clock function capable for Standby modes.

The PM10025 operate in low power mode, one 12-bit ADC with dual simple-and-hole and up to 10 external channels, three PGA-mode operational amplifiers (OPAs), four comparators with threshold PGAs, POR/PDR/BOR reset functions, and one internal reference voltage for ADCs.

All pins (except for VCC, GND, and NRST pins) on the PM10025 can configured as GPIOs, peripheral I/O, or be connected to external interrupt, maximizing pins for applications where pin count is a constraint.

PM10025 supports general flash write/read protection and special flash encryption by Panjit.

PM10025 is equipped with multiple communication interfaces: 2 UART serial ports, 1 high-speed SPI channel, and 1 I2C channel.

PM10025 integrates a hardware Division/Square Root operation unit (DVSQ), enhancing software processing capabilities and enabling rapid response to external events.

PM10025 supports Sleep and Stop modes, making it suitable for applications with stringent power efficiency requirements.

These features make the PM10025 microcontrollers suitable for applications such as square wave drive control of bldc motor applications:

- **Electric tools**
- **Industrial Fans**
- **Compressors**
- **Electric Vehicle**
- **Range Hoods**
- **Vacuum cleaners**
- **Water pumps**
- **Air conditioner**

2.1 Product Features

- **CPU Core**
  - **ARM® Cortex®-M0**
  - **Maximum clock frequency:48MHz**
  - **24-bit SysTick Timer**
- **Operating Voltage Range**
  - **Single power input range(Main Power VDD):2.2V~5.5V**
- **Operating Junction Temperature Range**
  - **-40°C ~ +105°C**
- **General Operating Current**
  - **Run Mode**
    - 2mA@5V@8MHz
    - 7.6mA@5V@48MHz
  - **Run Mode**

- 0.8mA@5V@40kHz
- 1.7mA@5V@8MHz
- 4.7mA@5V@48MHz

■ **Stop Mode**

- Normal mode:0.35mA@5V@40kHz
- Low-Power mode:8.83μA@5V@40kHz

◆ **Memory**

■ **32 Kbyte Flash**

- When the CPU frequency is at or below 24 MHz, zero wait-state cycle access to Flash memory is supported.
- The Flash memory features data security protection, with options for setting separate read and write protections
- Supports instruction and data encryption for Flash storage, which can prevent physical attacks on the Flash content.

■ **4Kbyte SRAM**

◆ **Clock**

■ **High-Speed External（HSE）：4~32MHz**

■ **Low-Speed External（LSE）：32.768kHz**

■ **High-Speed Internal（HSI）：8/12/48MHz**

■ **Low-Speed Internal（LSI）：40kHz**

■ **PLL Clock：1~48MHz**

■ **External Inputs Clock (GPIO)：5~30MHz**

◆ **Reset**

■ **External Pin Reset (NRST Pin)**

■ **Option Bytes Loader Reset**

■ **Window Watchdog Counter Termination（WWDG Reset）**

■ **Independent Watchdog Counter Termination（IWDG Reset）**

■ **Power Reset（POR/PDR/BOR）**

■ **Software Reset（SW Reset）**

■ **Low-Power Management Reset**

◆ **General-purpose inputs/outputs (GPIO)**

■ **Supports up to 44 GPIO ports**

◆ **DMA Controller**

■ **Equipped with 5 channels, allows for the selection of different request sources**

■ **Supports various peripherals triggers such as TIM, SPI, I2C, UART, ADC, etc.**

◆ **Data Communication Interface**

■ **2 UART**

■ **1 I^2C**

- Transmission rates of 1Mbps/400kbps/100kbps
- Supports data receive wakeup in Stop mode

■ **1 High-Speed SPI**

- Maximum transmission rate of 18 Mbps

◆ **Timer**

■ **1 x 16-bit advanced-control timer specifically for motors (TIM1)**

- 4 PWM outputs, of which three have deadband complementary PWM outputs
- Supports braking through external pin signals and internal comparator output signals.
- Supports multi-point comparison output trigger for ADC on CC1~CC6 channels

- **2 General-Purpose Timers**
  - 1 x 32-bit general-purpose timer (TIM2)
  - 1 x 16-bit general-purpose timer (TIM3)
- **1x 16-bit basic timer (TIM6)**

◆ **Division and Square Root Calculation（DVSQ）**

- **Supports 32-bit fixed-point division, capable of simultaneously providing quotient and remainder.**
- **Supports high-precision square root calculation for 32-bit fixed-point numbers.**

◆ **Analog integrated circuits**

- **1 x 12-bit dual-channel Sample and Hold SAR ADC with up to 10 external analog signal input channels**
  - 12-bit resolution
  - Maximum conversion frequency: 1MSPS
  - 2 independent sample and hold capacitor, allowing simultaneous sampling of two signals.
  - Supports four independent conversion queues and one test queue
  - Performs conversions in automatic continuous mode and scan mode
  - Supports channel replacement in the regular queue
  - Supports multiple hardware trigger sources, including TIM1_TRGO, TIM1_CCx, and GPIO input events
  - Supports the function of averaging the data of multiple channels in regular queues
  - Independent register for each channel to save data
- **Internal Reference Voltage**
  - The output of the internal reference voltage is connected to an independent ADC channel.
- **4 × Voltage Comparators**
  - The reference voltage for comparators is derived either from an external signal input or an internal 8-bit DAC.
  - The output from comparators can be utilized as a break signal for the advanced timer.
- **3 × Operational Amplifiers**
- **Programmable amplification factor.**
- **The output signal from amplifiers can be routed to pins or an ADC sampling channel.**

◆ **96-bit Unique ID (UID)**

- **Utilized as the serial number and security key.**
- **Employed to initiate the secure boot process.**

◆ **CPU Trace and Debug**

- **SWD debug ports**
- **ARM® CoreSight™ debug components (ROM-Table, DWT, BPU)**
- **Customized DBGMCU debug controller (low-power mode simulation control, debugged peripheral clock control, debug and trace interfaces allocation)**

◆ **Reliability**

- **Passed tests at HBM5500V/CDM2000V/LU250mA levels.**

2.2 Device Overview

Table 2-1 PM10025 Series Features

Feature		PM10025A	PM10025NT	PM10025PT	PM10025NF	PM10025PF
GPIO		26	28	28	44	44
Package		TSSOP28	QFN32	LQFP32	QFN48	LQFP48
Operating Voltage		2.2V~5.5V				
Operating Temperature		-40°C ~ +105°C				
Memory	Flash(Kbyte)	32				
	SRAM(Kbyte)	4				
CPU	Core	Cortex®-M0				
	Operating Frequency	48MHz				
DMA(channels)		1（5 channels）				
Division/Square Root Calculation (DVSQ)		1				
Clock	LSI	40kHz				
	HSI	8 MHz /12 MHz /48MHz				
	PLL Clock	Supported				
	HSE	4~32MHz				
	LSE	Not Supported			32.768kHz	
Timer	Advanced Timer	1（16 bit）：TIM1				
	General-Purpose Timer	1（32 bit）：TIM2 1（16 bit）：TIM3				
	Basic Timer	1（16 bit）：TIM6				
	Simple RTC	1 Independent 32-bit Counter (operable in low-power mode)				
	System Tick Timer	1				
	IWDG	1				
	WWDG	1				
Communication Peripherals	UART	2				
	I2C	1				
	SPI	1				
ADC	ADC (external channels)	1（7）	1（8）		1（10）	
	Reference	Internal Reference Voltage				
	ADC Conversion Frequency	1MSPS				
	ADC Accuracy	12 bit				
Voltage Comparator (COMP)		4				
Operational Amplifier (OPAMP)		3				
96-bit UID		1				

3 Ordering Information

3.1 Ordering Information

Table 3-1 PM10025A Product Ordering Information

Order number	Marking ID	Package	Description
PM10025AB	PM10025A BYMDNN	TSSOP-28	Halogen Free RoHS compliant in Tube 5000pcs

3.2 Marking Information

Table 3-2 PM10025A Product Marking Information

Marking	Package	Definition
PM10025A BYMDNN	TSSOP-28	Product code : PM10025A Package code : B Y : Year code M : Month code D : Day code NN: Serial Number

4 Function Introduction

4.1 Block Diagram

A 32 Kbyte Flash memory is integrated for storing programs and data.

The ARM® Cortex®-M0, a 32-bit RISC processor, offers exceptional computational performance and enhanced system responses to interrupts. The inclusion of the ARM® Cortex®-M0 core ensures that the entire series is compatible with all ARM tools and software.

Take PM10025PF series as an example:

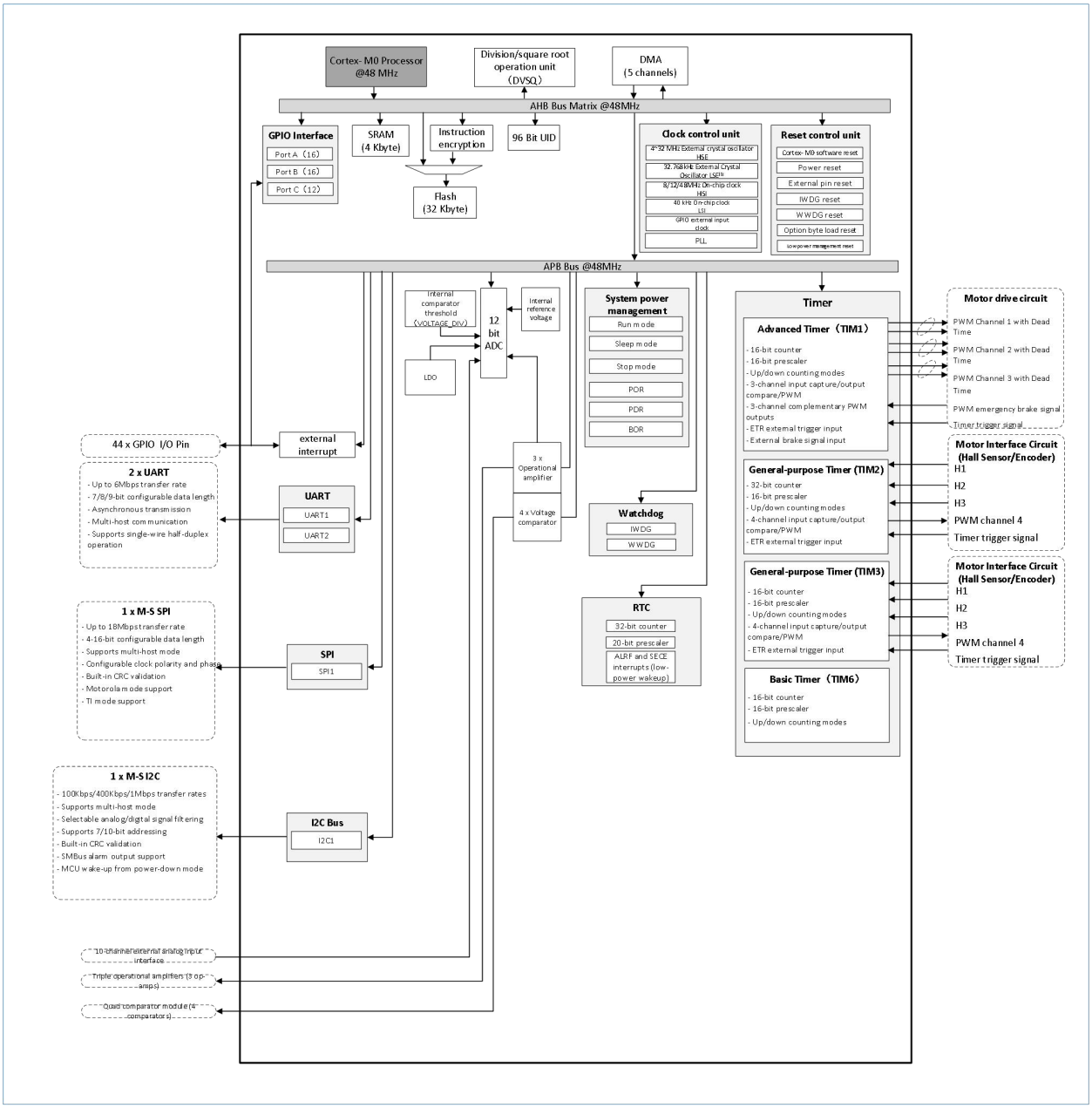

Figure 4-1 PM10025PF Block Diagram

Figure 4-1 Note：

(1). Only packages with 48 pins offer LSE.

4.2 Memory Mapping Configuration

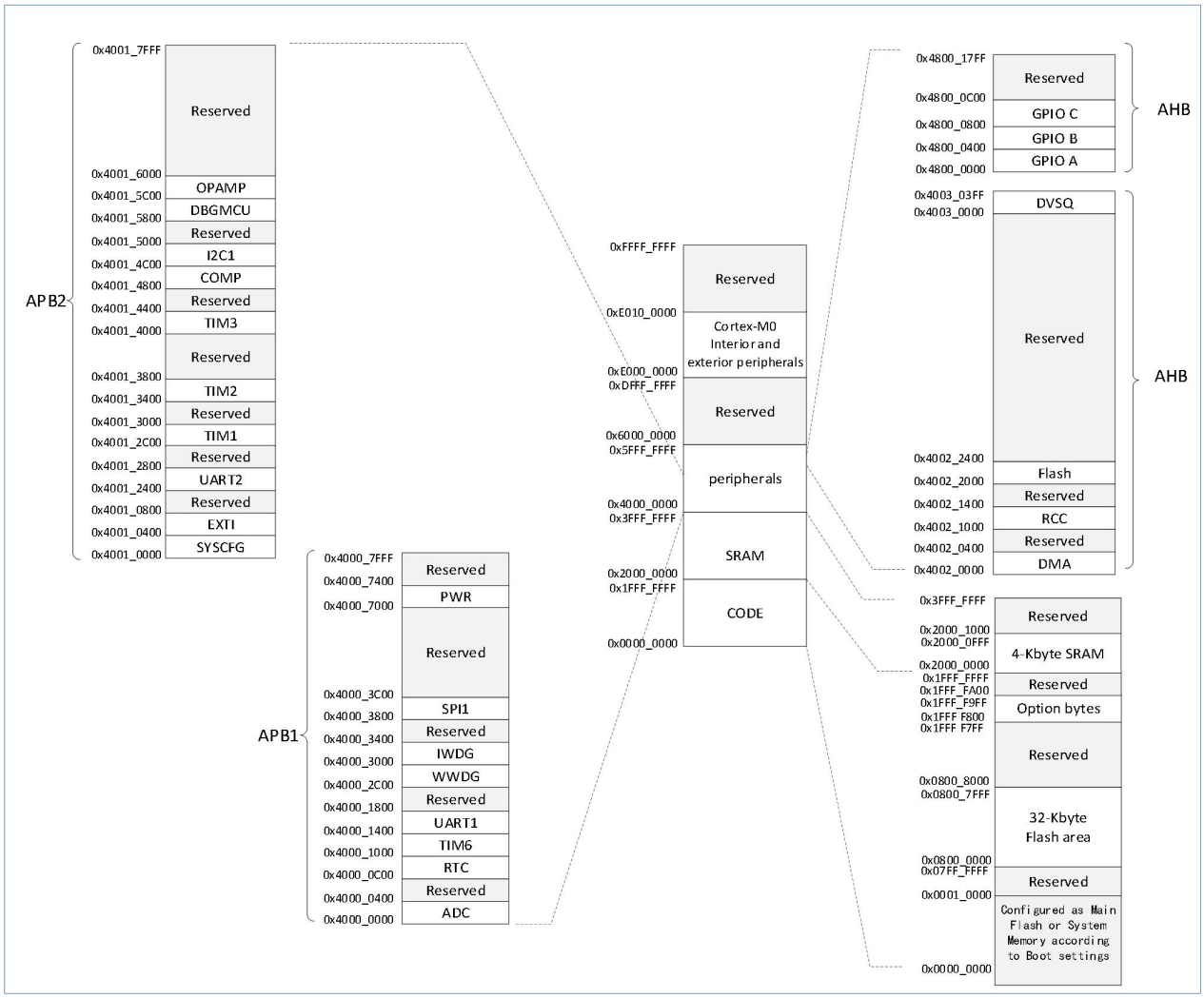

Figure 4- 2 PM10025PF Memory mapping

4.3 Memory

4.3.1 Flash

The series integrates a 32-Kbyte Flash memory for storing programs and data.

Through configuration of the Flash controller, remapping of interrupt vectors can be achieved within 32-Kbyte.

4.3.2 SRAM Integrated

The series features a 4-Kbyte SRAM, supports words, half-words, and bytes, with CPU access at zero wait states, accommodating a broad range of application.

4.4 Power Supply Schemes

V_{DD} =2.2 ~ 5.5V：External power supply (excluding V_{BAT}), V_{DD} pin provide power to the chip's digital circuitry, I/O pins, and internal voltage regulator.

V_{DDA} = 2.2 ~ 5.5V：V_{DDA} pin provides power to the analog circuitry, including the ADC, voltage comparators, and operational amplifiers.

Note：

V_{DD} and V_{DDA} are connected internally.

4.5 Power Supply Monitor

The MCUs feature POR/PDR/BOR circuitry. The MCU operates normally when the supply voltage reaches 2.2 V. If V_{DD}/V_{DDA} falls below the V_{POR}/V_{PDR} threshold, the MCU automatically resets without external circuits. During power-on, BOR ensures the MCU remains in reset until the supply voltage meets the V_{BOR} threshold. With BOR disabled, POR/PDR monitors the power supply.

4.6 Low-Power Mode

The series supports sleep and stop mode.

- Sleep Mode：Only the CPU stops operating, while all peripherals continue functioning. The CPU can be waken up when an interrupt or event occurs.
- Stop Mode：Enables the MCUs to achieve their lowest power consumption, preserving SRAM and register contents. In Stop Mode, all core domain clocks, including the PLL, HSI oscillator, and HSE oscillator, are disabled. The MCU can be awakened from Stop Mode by any EXTI (Extended Interrupt/Event Controller) line. EXTI sources can include any of the 16 external I/O pins. Additionally, I2C can revive the MCU from Stop Mode upon data reception.

4.7 Reset

4.7.1 System Reset

The system reset clears all registers except for the reset flags in the RCC_CSR control/status register. The source of the reset can be determined by examining the reset status flags in the RCC_CSR register.

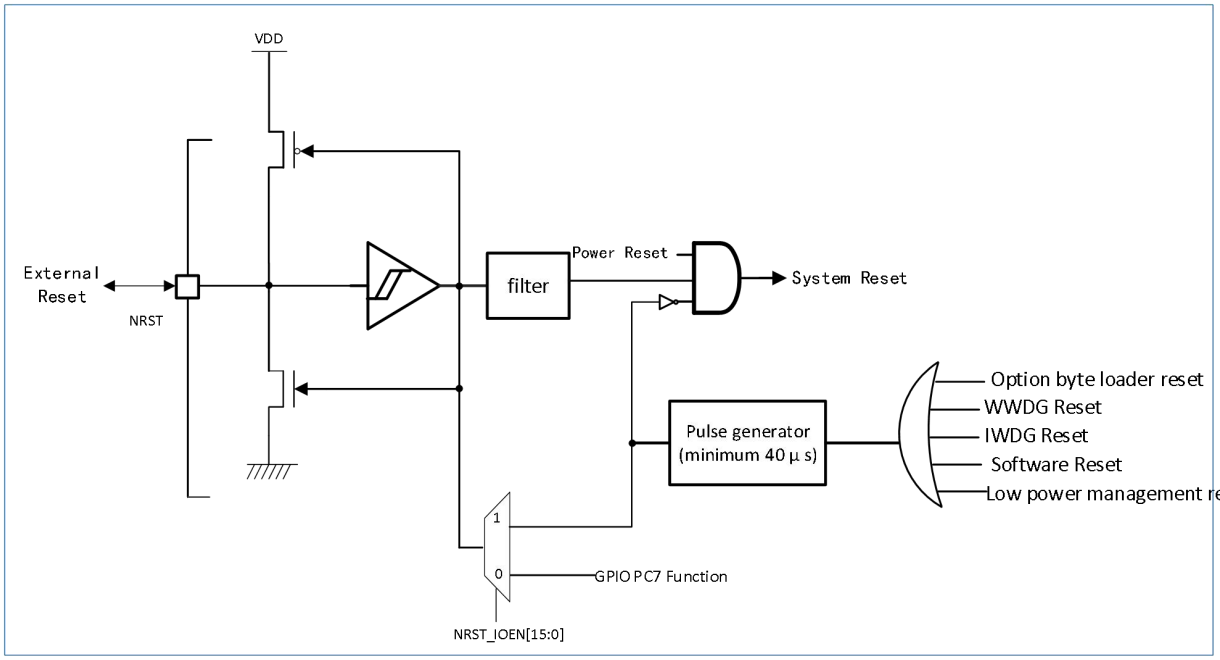

Figure 4- 3 Reset Signal

A system reset can be triggered by any of these events:

- **External reset due to a low level on the NRST pin**
- **Option byte loading (OBL) reset**
- **Window watchdog (WWDG) timeout**
- **Independent watchdog (IWDG) timeout**
- **Power reset, including POR (Power-On Reset), PDR (Power-Down Reset), and BOR (Brown-Out Reset).**
- **Software reset (SW reset), which requires setting the SYSRESETREQ bit in the Cortex®-M0 Application Interrupt and Reset Control Register to 1**
- **Low-power management reset**

Apart from the power reset, the triggers for all other resets ultimately affect the NRST pin, which maintains a low level during these resets. The reset entry vector is consistently located at address 0x00000004. Internal reset signals, excluding the power reset, are output through the NRST pin. A pulse generator ensures a minimum reset

pulse duration of 40 μs for each internal reset source. When the NRST pin is externally pulled low, generating an external reset, a reset pulse is produced.

4.7.2 Power Reset

A power reset can be triggered by any of these events:

- **Power-on reset (POR)/Power-down reset (PDR)**
- **Brown-out reset (BOR)**

The series' MCUs are equipped with POR (Power-On Reset) and PDR (Power-Down Reset) circuitry. This circuitry remains active to ensure proper system operation when the power supply exceeds 2.2 V. If V_{DD} falls below the POR/PDR threshold, the MCU automatically resets without needing an external circuit.

The series also incorporates a brown-out reset (BOR) feature, which is disabled by default. In this state, the power supply is monitored by POR/PDR. BOR can be enabled or disabled through the configuration of the option byte.

4.8 Clock and Clock Tree

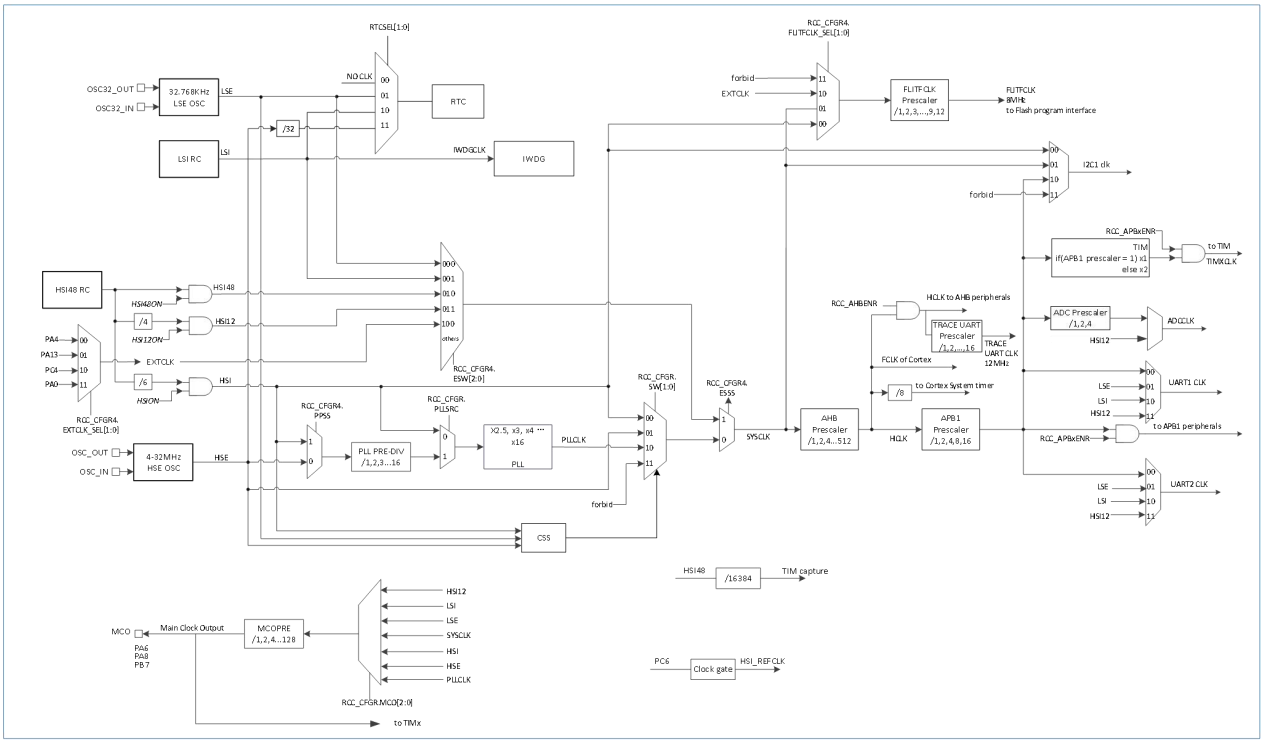

Figure 4- 4 Clock Tree

Note: Only LQFP48 and QFN48 packaging supports LSE.

As shown in the figure above, HSI48 and ADCCLK are derived from the same 48 MHz internal oscillator. Consequently, disabling one of these clocks does not lead to a reduction in power consumption when the other is in use.

Upon startup, the MCUs utilize SYSCLK as the CPU clock, sourced from an internal oscillator operating at 48 MHz. The default system clock, HSI, is a division of this 48 MHz clock and is automatically selected when the MCU powers on. Both HSI and HSE can serve as inputs for the phase-locked loop (PLL) pre-scaler, allowing the configuration of various system clock frequencies using HSI/HSE in conjunction with the PLL.

The series offers a range of clock sources for the system clock, providing customers with convenient, flexible, and diverse operating modes. The available options for the system clock include:

- **High-speed external clock (HSE): 4~32MHz**
- **Low-speed external clock (LSE): 32.768kHz**
- **High-speed internal clock (HIS): 8/12/48MHz**

- **Low-speed internal clock（LSI）：40kHz**
- **PLL clock：48MHz (Maximum)**
- **GPIO external input clock: 5~30MHz**

The clock frequencies of the AHB bus and APB domain can be configured through several frequency dividers. The maximum clock frequency of the AHB bus can reach up to 48MHz. The maximum clock frequency of the APB domain can also reach up to 48MHz.

The Clock Security System (CSS) monitors failures in the HSE (High Speed External) and LSE (Low Speed External) oscillators. Upon detecting a failure, the system automatically switches to an alternative clock source to maintain operational continuity.

4.9 GPIO

Each GPIO pin can be configured via software as an output pin (either push-pull or open-drain), an input pin (floating, with pull-up, or pull-down), or assigned to a peripheral's alternate function. Many GPIO pins support both digital and analog alternate functions. All GPIOs are capable of handling high currents. The configuration of I/O alternate functions can be locked through a specific operation to prevent unintended writes to the I/O registers.

4.10 SYSCFG

The MCU of this series features a set of system configuration registers that enable various functions, including:

- **Enabling or disabling Fast Mode Plus for I2C on selected I/O ports**
- **Remapping memory areas**
- **Managing external interrupts linked to the GPIOs**
- **Controlling the remapping of LSI, HSI, and LSE signals to TIM3_CH4**
- **Overseeing the switch to direct some internal analog signal outputs to I/Os**
- **Configuring the internal voltage divider (8-bit DAC)**

4.11 Boot Mode

Upon system startup, the boot pin is used to select one of the following boot modes:

- **Boot from Flash memory**
- **Boot from system memory**

The bootloader, stored in the system memory, can reprogram the Flash through the UART1 (PC8/PC9) interface.

4.12 DMA

The Direct Memory Access (DMA) controller facilitates high-speed data transfers between peripherals and memory, as well as memory-to-memory transfers. By operating without CPU intervention, DMA efficiently moves data to its destination, conserving CPU resources for other tasks.

The series incorporates a DMA controller designed to manage access requests from multiple peripherals. This controller includes an arbiter to prioritize different DMA requests.

- **DMA has five configurable, independent channels.**
- **Each channel is connected to dedicated hardware and can be triggered by either hardware or software.**
- **Support for circular buffer management.**
- **Compatibility with TIM1/2/3, SPI1, UART1/2, I2C1, and ADC for generating DMA requests.**

4.13 Interrupts and Events

4.13.1 NVIC

The PM10025 series embeds a nested vectored interrupt controller able to handle up to 22 maskable interrupts (not including the 16 interrupt line of Cortex®-M0) and four priority levels. This module provides flexible interrupt management capabilities with minimal interrupt latency.

- **Closely coupled NVIC gives low latency interrupt processing**
- **Interrupt entry vector table address passed directly to the core**

- **Allows early processing of interrupts**
- **Processing of late arriving higher priority interrupts**
- **Support for tail-chaining**
- **Processor state automatically saved**
- **Interrupt entry restored on interrupt exit with no instruction overhead**

4.13.2 EXTI

The Extended Interrupt/Event Controller (EXTI) in the series manages asynchronous interrupts and events. It routes event requests to the CPU, interrupt requests to the interrupt controller, and wakeup requests to the power supply management module.

EXTI is divided into two types: edge-configurable and edge-fixed. In the edge-fixed EXTI, only the rising edge serves as the trigger. This type of EXTI operates solely in Stop mode, primarily to awaken the core from this mode.

Up to 22 interrupt/event requests

- **22 configurable EXTI lines**
  - The trigger edge (rising or falling) is configurable.
  - Each line has a dedicated interrupt status bit flag.
  - Interrupts and events can be manually triggered via software.
- **1 fixed EXTI line**

Independent triggering and masking of each interrupt/event line.

Capability to detect external signals with pulse widths shorter than the APB2 clock period.

4.14 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

The IWDG (Independent Watchdog) can be configured to operate in window mode by setting the IWDG_WINR register.

4.15 System Window Watchdog(WWDG)

The System Window Watchdog (WWDG) is based on a 7-bit down counter, which can be configured as free-running. It's primarily used as a watchdog to reset the device in case of malfunctions. The WWDG is clocked by the APB clock (PCLK), not the main clock. It features an early warning interrupt capability, and its counter can be frozen in debug mode.

4.16 Timer

The series include up to one advanced timer, two general-purpose timers, and one basic timer. The following table provides a description of the features of these timers.

Table 4- 1 Timer Description

Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	DMA Request	Break Input	Capture/ Compare Channels	Complementary Outputs
Advanced timer	TIM1	16-bit	Up, down, up/down	1~65536	Yes	Yes	3	3
General- purpose timer	TIM2	32-bit	Up, down, up/down	1~65536	Yes	No	4	No

Type	Timer	Counter Resolution	Counter Type	Prescaler Factor	DMA Request	Break Input	Capture/ Compare Channels	Complementary Outputs
	TIM3	16-bit	Up, down, up/down	1~65536	Yes	No	4	No
Basic timer	TIM6	16-bit	Up	1~65536	No	No	No	No

4.16.1 Advanced Timer

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- **Input capture**
- **Output compare**
- **PWM generation (edge or center-aligned modes)**
- **One-pulse mode output**
- **The three channels have complementary PWM outputs with programmable inserted dead-zone.**

If TIM1 is configured as a 16-bit timer, it has the same functions as a basic timer. If TIM1 is configured as a 16-bit PWM generator, it has full modulation capability (0–100%). Many functions of TIM1 are the same as those of general-purpose timers. Therefore, the advanced timer can work together with general-purpose timers through the Timer Link feature for synchronization or event chaining.

The advanced timer provides the update event shifting function and simple data migration function which can be adopted in motor control.

In debug mode, the counter can be frozen

4.16.2 General-purpose Timer

The series integrates 2 general-purpose timer

- **TIM2 and TIM3**

TIM2 employs a 32-bit auto-reload up/down counter and a 16-bit prescaler, while TIM3 utilizes a 16-bit auto-reload up/down counter with a matching 16-bit prescaler. Both TIM2 and TIM3 feature four independent channels, each serving various purposes, including input capture, output comparison, PWM output, and one-pulse mode output.

TIM2 and TIM3 integrate with advanced timer TIM1 through the Timer Link feature, facilitating synchronization and event chaining. They possess the capability to independently generate DMA requests, process quadrature (incremental) encoder signals, and handle digital outputs from one to three hall-effect sensors. In debug mode, the counter's operation can be frozen.

4.16.3 Basic Timer

The series integrates a basic timer TIM6.

TIM6 is based on a 16-bit auto-reload upcounter and a 16-bit prescaler. In debug mode, the counter can be frozen.

4.16.4 System Tick Timer

The System Tick timer serves as a dedicated component within the operating system, designed as a standard down counter and designed with the following key features:

- **A 24-bit down counter**
- **The ability to auto-reload**
- **Generation of a maskable interrupt when the counter reaches the value of 0**
- **A programmable clock source**

4.17 ADC

The 12-bit analog to digital converter has up to 10 external channels and 6 internal channels. The ADC offers versatile operation modes, including single, continuous, scan, or discontinuous conversions. Key features include:

- **12-bit Resolution**
- **Support for a maximum ADC clock frequency of 24 MHz and a maximum ADC conversion frequency of 1 MSPS**
- **Two independent sample and hold units connected to the 14 analog input channels**
- **Compatibility with the DMA controller for efficient data transfer**
- **A flexible queue configuration with four independent regular queues and a test queue**
- **Queue operating modes, including single-sample and hold, dual-sample and hold, single-sample and hold scan, and BK modes**
- **A versatile arbitration mechanism, allowing priorities from 0 to 3 for each queue, with a higher number indicating a higher priority**
- **Independent registers for each channel to store the conversion results**
- **The ability to redirect the conversion request of a channel to another channel, facilitating testing and saving conversion results to different registers**
- **A data window comparison function that allows comparison of ADC conversion results with preset values**
- **Data averaging functionality for data pre-processing**
- **Support for trigger latency configuration, ensuring that ADC conversions start after a specified latency from the generation of a trigger signal**
- **The ability to connect events generated by advanced timer (TIM1) and general-purpose timers (TIM2/TIM3) to the ADC start trigger, enabling A/D conversions to be triggered by these timers internally**

4.17.1 Internal Reference Voltage

The internal reference voltage, VREFINT, serves as a reliable and stable voltage output, functioning as a bandgap voltage reference specifically designed for the ADC.

4.18 COMP

The series is integrated with four built-in voltage comparators (COMPs): COMP1, COMP2, COMP3, and COMP4. The four comparators can be used independently or used with timers:

The functions of the four comparators are:

- **To wake up the MCU from low-power modes after being triggered by the analog signal.**
- **For analog signal conditioning.**
- **Together with the timer PWM output to form the cycle-by-cycle current control loop**

4.19 OPAMP

The microcontroller incorporates three operational amplifiers (OPAMPs) capable of operating in Standalone, Follower, and PGA (Programmable Gain Amplifier) modes.

The outputs of these OPAMPs can be directed to external pins, internally connected to the inverting input node, or synchronized with the internal ADC for sampling purposes.

4.20 DVSQ

The features of the division and square root (DVSQ) calculation unit are listed below.

- **Support 32-bit signed integer division (SDIV), unsigned integer division (UDIV), as well as root calculation.**
  - Either division or root calculation can be supported at a given time.
  - In the case of 32-bit SDIV and UDIV, it updates the corresponding registers with the quotient and remainder.
  - The MOD operation is supported in division
- **High-precision root calculation can be opted for in the case of unsigned integer root calculations, with the option being available through software control.**
- **With a streamlined design, each clock period allows for a 2-bit calculation to be completed.**

- **The calculation time is variable and depends on the specific data being processed.**
- **The unit provides support for divide-by-zero interrupts and overflow interrupts, enhancing overall robustness and reliability.**

4.21 I2C Bus

The series features an I²C bus interface that supports both multimaster and slave modes. It operates at various speeds, including standard mode (up to 100 kHz), fast mode (up to 400 kHz), and fast mode plus (up to 1 MHz).

The I²C interface provides hardware support for SMBus 2.0 and PMBus 1.1, featuring capabilities like ARP, host notify protocol, hardware CRC (PEC) generation and verification, timeout verification, and ALERT protocol management.

The I²C interface operates independently of the CPU clock domain, enabling it to wake up the MCU from Stop mode when a matching address is detected, enhancing power efficiency and responsiveness.

Table 4-2 I2C Feature

I2C Features	I2C1
Master/Slave mode	Supported
Multimaster mode	Supported
Standard/Fast/Fast mode plus	Supported
7-bit/10-bit addressing mode	Supported
General call	Supported
Event management	Supported
Clock stretching	Supported
Software reset	Supported
DMA transmission	Supported
Analog and digital filter	Supported
SMBus2.0	Supported
PMBus1.1	Supported
Independent clock	Supported
Wakeup from Stop mode	Supported

4.22 Universal synchronous/asynchronous/receiver/transmitter(UART)

The MCU includes two UARTs (UART1 and UART2) capable of high-speed communication, with a maximum baud rate of up to 6 Mbit/s. These UARTs offer hardware management for RS485 DE signals, support multiprocessor communication mode, and facilitate single-wire half-duplex communication. Furthermore, they are compatible with DMA controller usage for efficient data transfer.

Table 4-3 UART Feature

UART Modes/ Features	UART1/UART2
Data word length	7/8/9-bit
DMA transmission	Supported
Multiprocessor communication	Supported
Single-wire half-duplex communication	Supported
RS232 hardware flow control	No supported
RS485 driver enable	Supported

4.23 Serial peripheral interface(SPI)

Each MCU is equipped with a single Serial Peripheral Interface (SPI). This SPI interface is versatile, supporting both full-duplex and half-duplex communication modes, and it can operate as either a master or a slave device.Additionally, the SPI interface features a 3-bit prescaler that allows for the generation of eight different master mode frequencies. Each data frame within the communication can be configured to be 4 to 16 bits in length, offering flexibility in data transmission.

Table 4-4 SPI Feature

SPI Features	SPI1
Hardware CRC calculation	Supported
RX/TX FIFO	Supported
NSS pulse mode	Supported
TI mode	Supported
DMA transmission	Supported

4.24 RTC

The Real-Time Clock (RTC) in the series comprises continuously running counters and provides clock functionality through software. Additionally, it offers alarm and seconds interrupts, serving as potential wakeup sources in Stop mode.

The RTC can be clocked using three sources: HSE/32, LSE, or LSI. It features a 32-bit programmable counter that works in conjunction with the alarm register, enabling long-term measurements and alarm event generation. The RTC also includes a 20-bit prescaler responsible for generating the time base clock. When the RTC is clocked by the 32.768 kHz crystal oscillator (LSE) and the prescaler register is set to 0x7FFF, it generates a 1-second time base.

4.25 96-bit UID

The 96-bit Unique Identifier (UID) serves as an exclusive reference number for each MCU and is inherently unalterable. The UID can be accessed in various formats, including bytes (8 bits), half-words (16 bits), or words (32 bits), making it adaptable for diverse applications. Here are some potential uses for the 96-bit UID:

- **Serial Number: It can function as a unique serial number, suitable for applications like USB string serial numbers or other terminal-based functionalities.**
- **Security Key: The UID can be employed as a security key. When programming the Flash memory, combining the UID with software encryption and decryption algorithms enhances the security of the code stored in the Flash memory.**
- **Boot Process Activation: The UID can play a role in initiating the boot process of security mechanisms, contributing to enhanced security protocols and processes.**

4.26 DBG

The integrated SWJ-DP in ARM allows for serial line SWDIO/SWCLK debugging interface.

5 Electrical Characteristics

5.1 Absolute Maximum Values

Stress test values represent the absolute maximum limits for short durations. Important guidelines include:

Warning：

- Avoid operating the device at or above these maximum values.
- Exceeding these limits, as detailed in Tables 5-1 to 5-3, could permanently damage the device.
- Prolonged operation near these maximum values may reduce the device's reliability.

5.1.1 Limit Voltage Characteristics

Table 5-1 Limit Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External main power supply voltage (including VDDA and VDD)	-0.3	5.5	V
V_{IN}	Input voltage on pins	-0.3	5.5	
$\|V_{SSX} - V_{SS}\|$	Variation between different ground pins	-	50	mV

5.1.2 Limit Current Characteristics

Table 5-2 Limit Current Characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into VDD/VDDA (source)(1)	105	mA
I_{VSS}	Total current from VSS (sink)(1)	105	
I_{IO}	Output current sunk by any I/O and control pin	60	
	Output current sourced by any I/O and control pin	60	
$I_{INJ(PIN)}$ (2)	Injected current on pins(3)	-5/+0	
$\Sigma I_{INJ(PIN)}$	Total injected current (all I/Os and control pins)(4)	-25/+0	

(1). All power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must continuously connect to the external power supply within the specified range.

(2). Negative current injection affects the device's analog performance.

(3). A positive injected current occurs when VIN exceeds VDD, and a negative one when VIN falls below VSS. Injected currents must stay within allowed limits.

(4). For multiple I/Os undergoing current injection, the maximum total IINJ (PIN) equals the combined absolute instant values of both positive and negative injected currents.

5.1.3 Limit Temperature Characteristics

Table 5-3 Limit Temperature Characteristics

Symbol	Description	Min	Max	Unit
T_{STG}	Storage Temperature Range	-55	130	°C
T_J	Maximum Junction Temperature	-55	130	°C

5.2 Operating Parameters

5.2.1 Recommended Operating Conditions

Table 5-4 Running Condition

Symbol	Description	Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	-	48	MHz
f_{PCLK1}	Internal APB1 clock frequency	-	48	
f_{PCLK2}	Internal APB2 clock frequency	-	48	
V_{DD}	Standard operating voltage	2.2	5.5	V
V_{REFP} (1)	Analog operating voltage	2.2	5.5	V
T	Operating temperature	-40	105	°C

(1). V_{REFP} can be lower than V_{DD}, For instance, V_{DD}=4.2V, V_{REFP}=3.3V; V_{DD}=3.3V, V_{REFP}=2.5V.

5.2.2 BOR Characteristics

Table 5-5 BOR Characteristics

Symbol	Parameter	Level	Minimum	Typical	Maximum	Unit
V_{BOR}(1)	BOR detection level selection (VDD rising edge) (–40°C to 105°C)	V_{BOR0}	2.34	2.42	2.46	V
		V_{BOR1}	2.75	2.83	2.91	
		V_{BOR2}	3.24	3.29	3.35	
		V_{BOR3}	3.66	3.72	3.81	
		V_{BOR4}	4.07	4.15	4.26	
		V_{BOR5}	4.45	4.58	4.71	
		V_{BOR6}	4.87	4.97	5.29	
		V_{BOR7}	5.25	5.44	5.58	
	BOR detection level selection (VDD falling edge) (–40°C to 105°C)	V_{BOR0}	2.11	2.24	2.31	
		V_{BOR1}	2.55	2.63	2.68	
		V_{BOR2}	2.91	3.05	3.09	
		V_{BOR3}	3.32	3.44	3.51	
		V_{BOR4}	3.68	3.83	3.91	
		V_{BOR5}	4.11	4.23	4.33	
		V_{BOR6}	4.51	4.61	4.71	
		V_{BOR7}	4.79	5.02	5.12	
$V_{BORhyst}$	BOR Hysteresis	-	150	-	400	mV
t_{BORRST}(2)	Time for BOR to take effect after reaching the threshold	-	-	10	-	μs

(1). Only V_{DD} is monitored for BOR

(2). The values are guaranteed with design.

5.2.3 POR/PDR Characteristics

Table 5-6 POR/PDR Characteristic

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
$V_{POR/PDR}$ (1)	POR/PDR threshold	Falling edge	1.67	1.92	2.16	V
		Rising edge	1.85	2.08	2.35	V
$V_{PDRhyst}$	PDR hysteresis	-	140	160	170	mV
$t_{RSTTEMPO}$ (2)	Reset duration	-	-	2	-	ms

(1). Only V_{DD} is monitored for PDR and POR.

(2). The values are guaranteed with design.

5.2.4 Internal Reference Voltage

Table 5-7 Internal Reference Voltage

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{REFINT}	Internal reference voltage	-40 ~ 105°C	-	0.8	-	V

5.2.5 Operating Current Characteristics

Table 5-8 Operating Current Characteristics

Symbol	Mode	Condition	VDD=5V			Unit
			-40°C	25°C	105°C	
I_{run}	Run mode	SYSCLK = 48 MHz; LSI enabled, other peripherals disabled; All I/Os configured in high impedance; Two wait states to access Flash.	7.35	7.63	7.89	mA
		SYSCLK = 8 MHz; LSI enabled, other peripherals disabled; All I/Os configured in high impedance; Zero wait states to access Flash.	1.9	2	3.7	mA
		SYSCLK= 40kHz; All I/Os configured in high impedance; LSI enabled, other peripherals disabled; Zero wait states to access Flash.	0.531	0.656	0.687	mA
I_{Sleep1}	Sleep mode 1	SYSCLK = 48 MHz; AHB/APB enabled; Core clock disabled, all peripherals disabled; All I/Os configured in high impedance; RAM and peripheral data retained.	4.48	4.68	5.21	mA
I_{Sleep2}	Sleep mode 2	SYSCLK = 8 MHz; AHB/APB enabled; Core clock disabled, all peripherals disabled; All I/Os configured in high impedance;	1.59	1.67	1.81	mA

Symbol	Mode	Condition	VDD=5V			Unit
		RAM and peripheral data retained.				
		Wakeup time	-	1.63	-	μs
I_{Sleep3}	Sleep mode 3	SYSCLK = 40 kHz; AHB/APB enabled; Core clock disabled, all peripherals disabled; All I/Os configured in high impedance; RAM and peripheral data retained.	753	808	938	μA
		Wakeup time	-	83	-	μs
I_{Stop}	Stop mode mode	All clocks stopped, HSI oscillator and HSE oscillator disabled, LSI oscillator enabled, all peripherals disabled; LDO operating in normal power mode; All I/Os configured in high impedance; Backup registers retained; CPU, RAM, and peripheral data retained.	300.5	353.2	487.8	μA
		Wakeup time	-	6.25	-	μs
I_{LPstop}	LowPower Stop mode	All clocks stopped, HSI oscillator and HSE oscillator disabled, LSI oscillator enabled, all peripherals disabled; LDO operating in low-power mode, all peripherals disabled; All I/Os configured in high impedance; Backup registers retained; CPU, RAM, and peripheral data retained.	5.9	8.83	54.3	μA
		Wakeup time	-	57	-	μs

5.2.6 HSE Clock Characteristics

Table 5-9 Clock Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{OSC_IN}	Oscillator frequency	-	4	-	32	MHz
R_F(1)	Feedback resistor	-	-	1.1	-	MΩ
$T_{stb\ (HSE)}$ (2)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	0.7	1.8	ms
C	Recommended load capacitance minus equivalent serial resistance of the crystal oscillator (RS)		-	12	-	pF
$I_{DD\ (HSE)}$ (1)	HSE oscillator power consumption	Normal operation: V_{DD}=3.3V, CL=12pF	-	400	-	μA

(1). The values are guaranteed with design;

(2). $T_{stb\ (HSE)}$ refers to the time from HSE startup to the time when it outputs stable frequency signals.

An HSE negative feedback circuit supplied with a crystal resonator in integrated. The following oscillator circuit outside the chip is recommended:

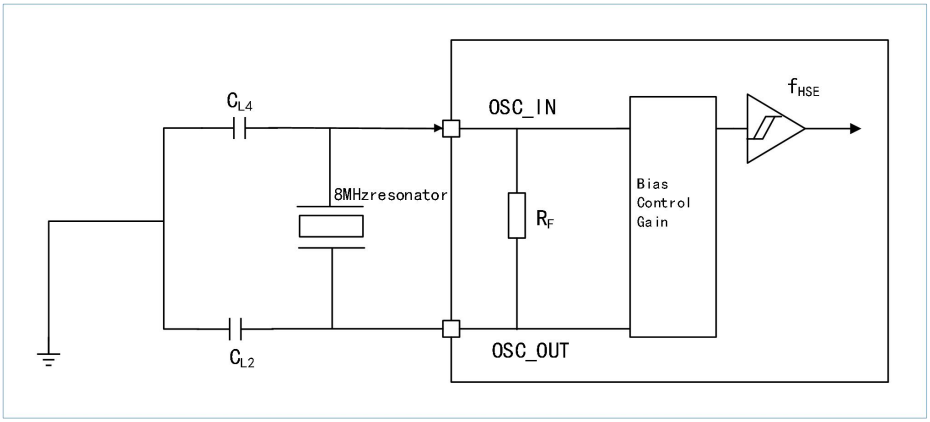

Figure 5-1 HSE Oscillator Circuit

Alternatively, it can be clocked from the OSC_IN pin. The following table lists the requirements for this clock signal:

Table 5-10 External Clock Input Features

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{HSE_ext}	External clock source frequency	-	4	-	32	MHz
$DuCy_{(HSE)}$ (1)	Duty cycle	-	45	-	55	%

(1). The values are guaranteed with design;

5.2.7 LSE Clock Characteristics

Table 5-11 LSE Clock Characteristics (fLSE=32.768 kHz)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
R_F(1)	Feedback resistor	-	-	10	-	MΩ
$T_{stb\ (LSE)}$ (2)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	2000	-	ms
C	Recommended load capacitance minus equivalent serial resistance of the crystal oscillator	-	-	12	-	pF
$I_{DD\ (LSE)}$ (1)	LSE oscillator power consumption	Normal operating conditions: V_{DD} = 3.3V with CL = 12pF (AGC disabled).	-	700	-	nA

(1). The values are guaranteed with design;

(2). $T_{stb\ (HSE)}$ refers to the time from HSE startup to the time when it outputs stable frequency signals.

An LSE (Low-Speed External) negative feedback circuit is integrated paired with a crystal resonator. It is recommended to use a specific external oscillator circuit with this chip:

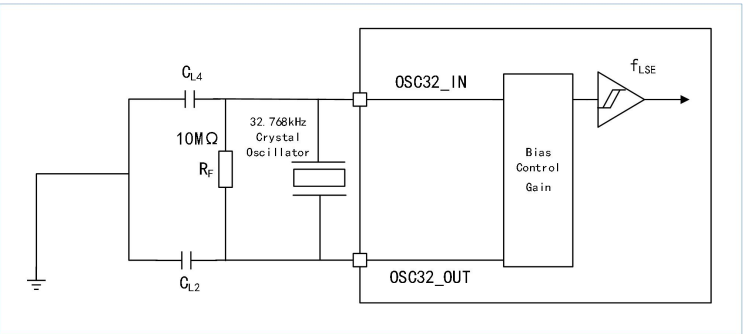

Figure 5-2 LSE negative feedback circuit

It can also be clocked from the OSC32_IN pin. The following table lists the requirements for this clock signal.

Table 5-12 Characteristics of the input LSE clock(1)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
fLSE_ext	External clock source frequency	-	-	32.768	-	kHz
DuCy $_{(LSE)}$	Duty cycle	-	45	-	55	%

(1). The values are guaranteed with design.

5.2.8 HIS Clock Characteristics

Table 5-13 HSI Clock Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{HSI}(1)	External clock source frequency	-	-	48	-	MHz
DuCy $_{(HSI)}$ (1)	Duty cycle	-	45	50	55	%
ACC $_{(HSI)}$	Oscillator accuracy	RCC_CR register calibration completed by the user	-1	-	1	%
		Factory calibration: T_A = –40°C to +105°C	-1.3	-	1.0	
$T_{stb\ (HSI)}$ (1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	8	11	µs
$I_{DD\ (HSI)}$ (1)	Oscillator power consumption	48 MHz, V_{DD} = 5 V	-	115	145	µA

(1). The values are guaranteed with design.

5.2.9 LSI Clock Characteristic

Table 5-14 LSI Clock Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{LSI}	Frequency	-	-	40	-	kHz
$T_{su\ (LSI)}$ (1)	Oscillator startup time	$V_{SS} \le V_{IN} \le V_{DD}$	-	50	150	µs
$I_{DD\ (LSI)}$ (1)	Oscillator power consumption	-	-	250	-	nA

(1). The values are guaranteed with design.

5.2.10 PLL Characteristics

Table 5-15 PLL Characteristics (1)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
f_{PLL_IN}	Input clock frequency	2	-	48	MHz
	Input clock duty cycle	45	50	55	%
f_{PLL_OUT}	Output clock frequency	6	-	48	MHz
t_{LOCK}	PLL lock time	-	60	150	μs

(1). The values are guaranteed with design.

5.2.11 Flash Memory Characteristics

Table 5-16 Flash Memory Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_{PROG}	One-word programming time	62	62	102	μs
T_{ERASE}	Page erase time	100	100	200	ms
	Mass erase time	100	100	200	ms
I_{DDPROG}	One-word programming current	-	-	8	mA
$I_{DDERASE}$	Page/Mass erase current	-	-	9	mA
I_{DDREAD}	Supply current@25 MHz (read mode)	-		3	mA
N_{END}	Erasure endurance	100	-	-	kcycles
t_{RET}	Data retention	10	-	-	year

5.2.12 IO Pin Input Characteristics

Table 5-17 IO pin input characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input high level voltage	V_{DD}=3.3V	0.65*V_{DD}	-	-	V
V_{IL}	Input low level voltage	V_{DD}=3.3V	-	-	0.2*V_{DD}	V
V_{IHhys}	Input high level voltage	V_{DD}=3.3V	0.65*V_{DD}	-	-	V
V_{ILhys}	Input low level voltage	V_{DD}=3.3V	-	-	0.2*V_{DD}	V
V_{hys}	Schmitt trigger voltage hysteresis	V_{DD}=3.3V	-	-	0.2*V_{DD}	mV

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
I_{lkg}	Input leakage current	V_{DD}=3.3V; 0<V_{IN}<3.3V	-	5	-	nA
		V_{DD}=3.3V; V_{IN}=5V	-	5	-	nA
R_{PU}	Pull-up resistor	V_{IN}=V_{SS}	-	33	-	kΩ
R_{PD}	Pull-down resistor	V_{IN}=V_{DD}	-	33	-	kΩ
C_{IO}(1)	I/O pin capacitance	-	-	-	10	pF

(1). The values are guaranteed with design.

5.2.13 IO Pin Output Characteristics

Table 5-18 IO Pin Output Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output high level voltage	2.4V ≤ V_{DD} ≤5.5 V	0.8*V_{DD}	-	-	V
V_{OL}	Output low level voltage	2.4V ≤ V_{DD} ≤5.5 V	-	-	0.2* V_{DD}	V

5.2.14 NRST Pin Characteristics

The NRST pin is internally integrated with a pull-up resistor. It can be either left floating (no external components required) or connected to an external RC circuit.

Table 5-19 NRST Pin Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_{Noise}	Low level values are disregarded	-	-	80	ns

5.2.15 TIM Timer Characteristics

Table 5-20 TIM1 Characteristics (1)

Symbol	Condition	Minimum	Maximum	Unit
F_{EXT}	Frequency of the timer's external clock on CH1 to CH3	-	$f_{TIMxCLK}$/2	MHz

(1). The values are guaranteed with design , $f_{TIMxCLK}$ = 48MHz.

Table 5-21 TIM2/3 Characteristics (1)

Symbol	Condition	Minimum	Maximum	Unit
F_{EXT}	Frequency of the timer's external clock on CH1 to CH4	-	$f_{TIMxCLK}$/2	MHz

(1). The values are guaranteed with design , $f_{TIMxCLK}$ = 48MHz.

5.2.16 ADC Characteristics

Table 5-22 ADC Characteristics

Program	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{DD}	Analog power supply voltage when ADC is	-	2.0	5	5.5	V

Program	Parameter	Condition	Minimum	Typical	Maximum	Unit
	enabled					
V_{REFP}	Positive reference voltage	-	2.0	5	5.5	V
V_{REFN}	Negative reference voltage	-	0	0	0	V
f_{ADC}	ADC clock frequency	-	0.3	12	24	MHz
f_S (1)	Sampling frequency	f_{ADC} = 12MHz	-	0.857	-	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 12 MHz	-	-	705	kHz
			17	-	-	Cycles
V_{AIN}	Conversion voltage range	-	V_{REFN}	-	V_{REFP}	V
R_{AIN} (1)	External input impedance	Refer to Table 5-25 for details				kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	2	kΩ
C_{ADC} (1)	Sample and hold capacitance	-	-	5	-	pF
JitterADC	Jitters triggered by ADC conversions	-	-	1	-	Cycles
t_S (1)	Sampling time	f_{ADC} = 12MHz	1.5	-	239.5	Cycles
t_{CONV} (1)	Total conversion time (including sampling time)	f_{ADC} = 12MHz; 12-bit resolution	14	-	252	Cycles

(1). The values are guaranteed with design

(2). The value is measured based on the ADC clock. The register access latency is not taken into account.

The calculation formula of the maximum input impedance R_{AIN}:

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The value of N (resolution) is 12

The allowable error can be lower than 1/4 least significant bit (LSB)

Table 5-23 Maximum input impedance values（fADC = 12 MHz）

Sampling Cycle Ts（Cycles）	Sampling Times（μs）	Maximum Input Impedance (kΩ)
1.5	0.125	0.577
7.5	1.6	10.8
13.5	1.125	21.1
28.5	2.375	46.9
41.5	3.458	69.3
55.5	4.625	93.3

Sampling Cycle Ts（Cycles）	Sampling Times（μs）	Maximum Input Impedance (kΩ)
71.5	5.958	120.8
239.5	19.958	409.5

Table 5-24 ADC Accuracy

Symbol	Parameter	Test Condition	Typical	Maximum	Unit
ET	Total unadjusted error(1)	V_{DD}=V_{REFP}=5V, f_{ADC} = 12 MHz,	-	13	LSB
EO	Offset error(2)		-	3	
EG	Gain error(3)		-	5	
ED	Differential linearity error(4)		-	2	
EL	Integral linearity error(5)		-	3	

(1). Total unadjusted error refers to the maximum deviation from the actual to the ideal transfer curve.

(2). Offset error is the difference between the first actual and the first ideal conversion.

(3). Gain error indicates the deviation between the last ideal conversion and the last actual conversion.

(4). Differential linearity error is the maximum deviation of the actual step from the ideal step.

(5). Integral linearity error represents the maximum deviation between any actual transition and the endpoint correlation line.

Note：

- To maintain ADC accuracy, avoid negative current injection on standard analog pins, as it significantly impairs conversion accuracy on other pins. Using a Schottky diode (pin to ground) on these pins is advisable.
- Enhanced ADC performance is achievable within specific VDDA, frequency, and temperature ranges.
- The data presented are based on characterization, not production testing.

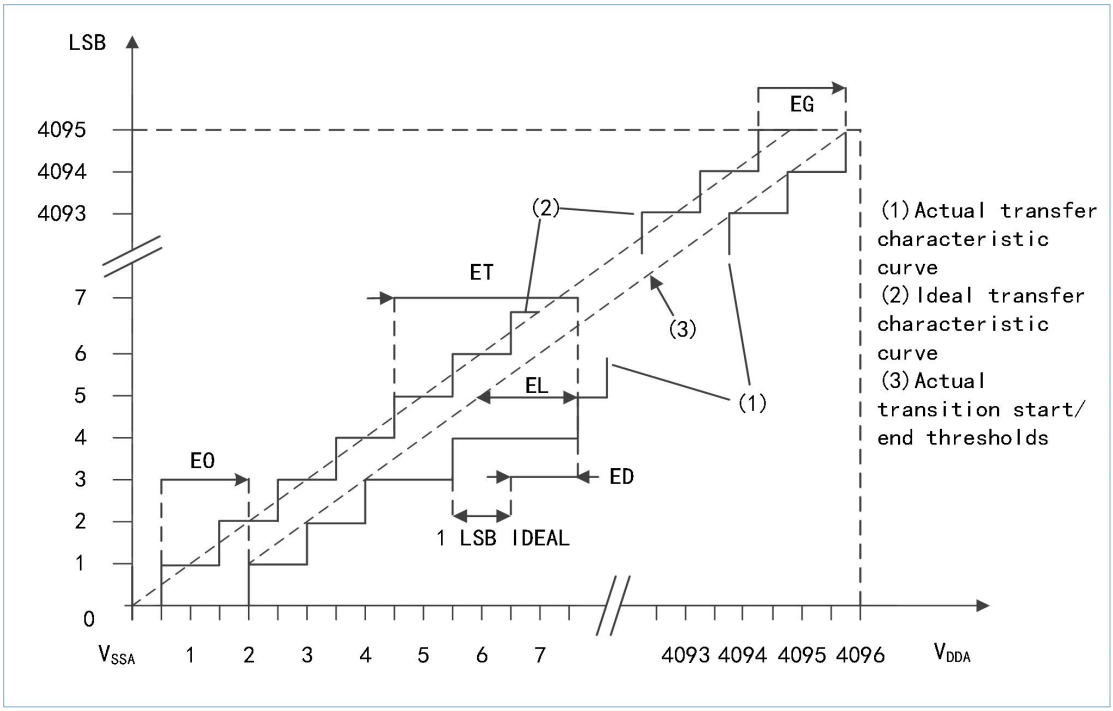

Figure 5-3 ADC Accuracy Characteristics

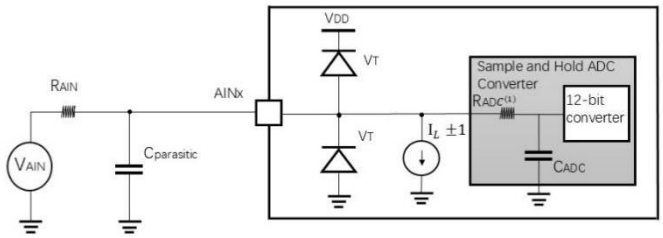

Figure 5-4 ADC

(1). For RADC and CADC ADC characteristics, refer toTable 5-24。

$C_{parasitic}$, combining PCB and pad capacitance, affects conversion accuracy. Higher $C_{parasitic}$ values necessitate lower fADC.

For ADC sampling PCB design, follow Figure 6-1 for power supply decoupling. Use ceramic 10 nF capacitors near the chip to ensure ADC conversion accuracy.

5.2.17 DAC Voltage Divider Characteristics

Table 5-25 DAC Voltage Divider Characteristics

Program	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{DD}	Analog power supply voltage when DAC is enabled	-		5	5.5	V
R_O	Output impedance	DAC buffer enabled	-	7	-	kΩ
I_{OUT}(1)	Output current	DAC buffer enabled	-	-	2	mA

(1). The values are guaranteed with design.

5.2.18 Voltage Comparator (COMP) Characteristics

Table 5-26 COMP Characteristics

Program	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{DD}	Analog power supply voltage	-	2.2	5	5.5	V
V_{com}	Input common mode Voltage	-	0.2	-	5.3	V
V_{diff}	Input differential mode voltage	Low-power (low-speed) mode	-	-	40	mV
		High-power (high-speed) mode	-	-	10.5	
V_{hy}	Hysteresis voltage	Level 1	-	0	-	mV
		Level 2	-	10	-	
		Level 3	-	20	-	
I_{OP}	Operating current (VDD = 5 V, static power consumption)	Low-power (low-speed) mode	1.405	2.81	3.74	μA
		High-power (high-speed) mode	22.2	38.55	42.42	
T_{dly}(1)	Output delay (no hysteresis)	High-power (high-speed) mode Rising edge	28.67	42.81	79	ns
		Low-power (low-speed) mode Rising edge	142.3	287.4	753.4	
		High-power (high-speed) mode Falling edge	30.62	57.8	72.13	
		Low-power (low-speed) mode Falling edge	206.5	597.2	849.8	

(1). The values are guaranteed with design.

5.2.19 Operational amplifier (OPAMP) characteristics

Table 5-27 OPAMP Characteristics

Program	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{DD}(1)	Analog power supply voltage	-	2.7	5	5.5	V
V_{OUT}	Output voltage	-	0.2	-	V_{DDA}-0.2	V
CMIR	Input common mode	-	0	-	5.5	V

Program	Parameter	Condition	Minimum	Typical	Maximum	Unit
	voltage					
I_{bias}(2)	Input bias current	-	0.8	1	1.2	μA
I_{load}	Output current	R_L=100Ω, V_{DD}=5V	-	6	-	mA
I_q	Operating current	Static mode	-	-	1100	μA
I_l(2)	Leakage current	OPAMP disabled	-	2.00	170.00	nA
V_{OS}	Input bias voltage	Before calibration	-	±15	-	mV
		After calibration	-	±2.5	-	mV
CMRR(2)	Common mode rejection ratio	-	51	-	145	dB
PSRR(2)	Power supply rejection ratio	-	41	70	109.4	dB
UGF	Unity-gain bandwidth	-	-	6	6.4	MHz
SR	Slew rate	(5%-95%) rising	5.213	6.251	8.061	V/μs
		(5%-95%) falling	5.278	6.571	8.679	
φ	Phase margin	-	47.09	70.93	84.58	Deg
PGA gain	PGA gain	Level 1	-	1	-	times
		Level 2	-	2	-	
		Level 3	-	5	-	
		Level 4	-	8	-	
		Level 5	-	10	-	
		Level 6	-	14	-	
		Level 7	-	16	-	
		Level 8	-	20	-	

(1). Ensure that the operating voltage of the OPAMP is from 2.7 V to 5.5 V. The operating voltage of other peripherals can be lower than 2.7 V.

(2). The values are guaranteed with design.

6 Typical Circuitry

6.1 Power Supply Scheme

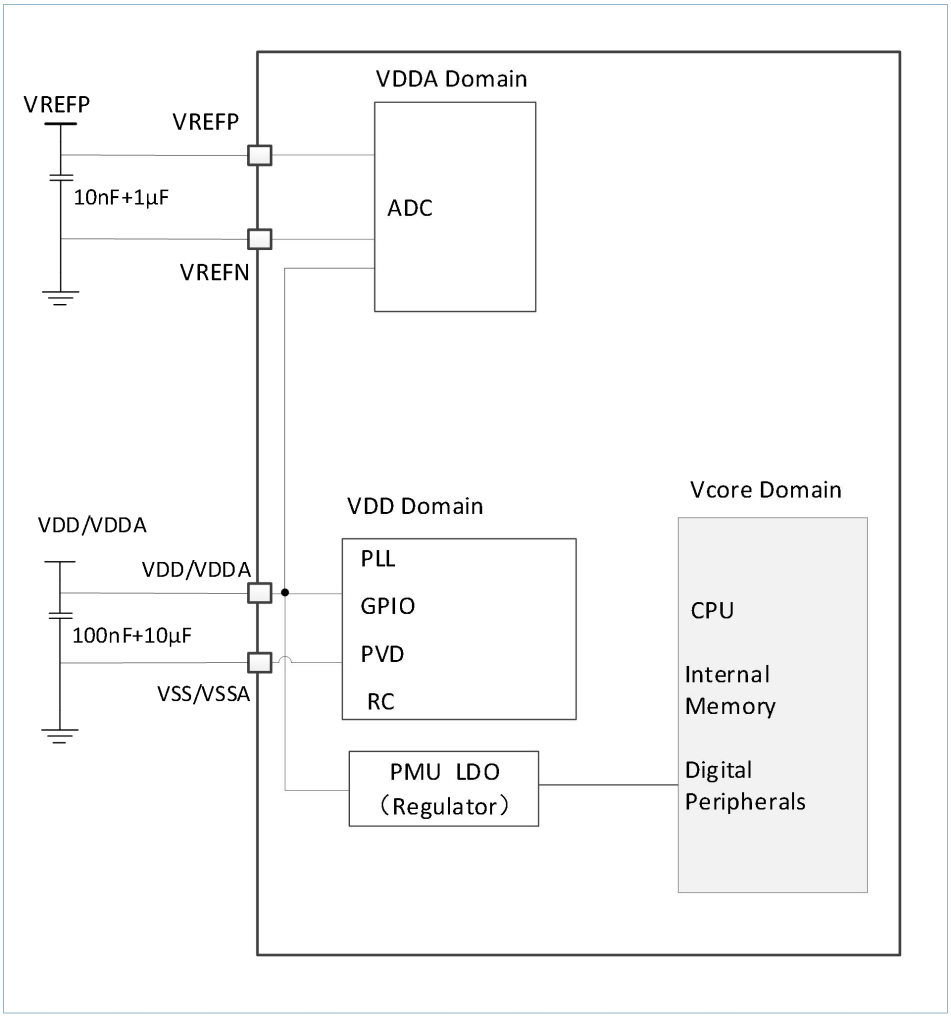

Figure 6-1 Power Supply Block Diagram

7 Pin Definition

The series contain TSSOP28、QFN32、LQFP32、QFN48 和 LQFP48 packages. This chapters defines each pin definition.

7.1 TSSOP28 Package

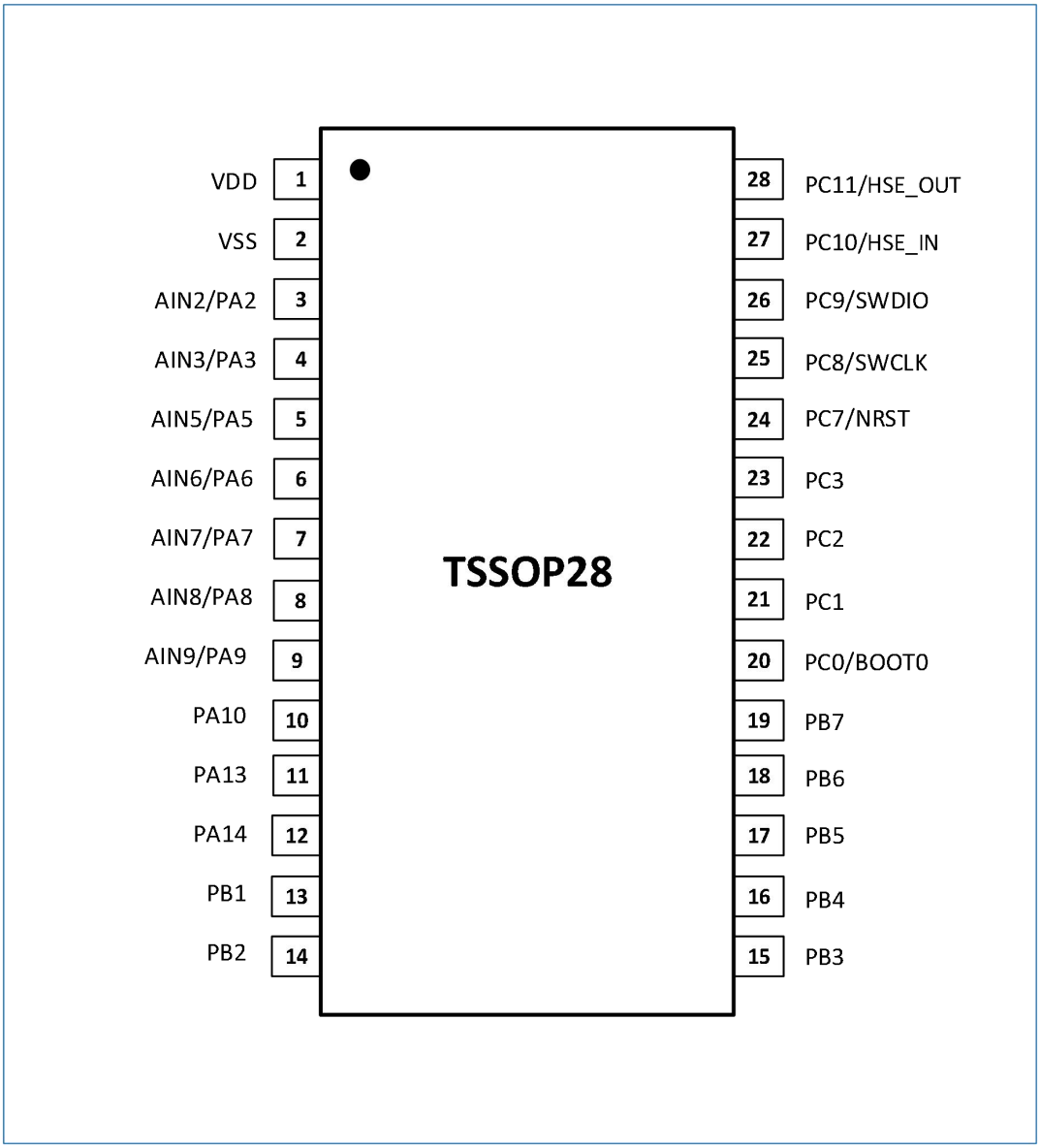

Figure 7-1 TSSOP28 Pins

7.2 QFN32 Package

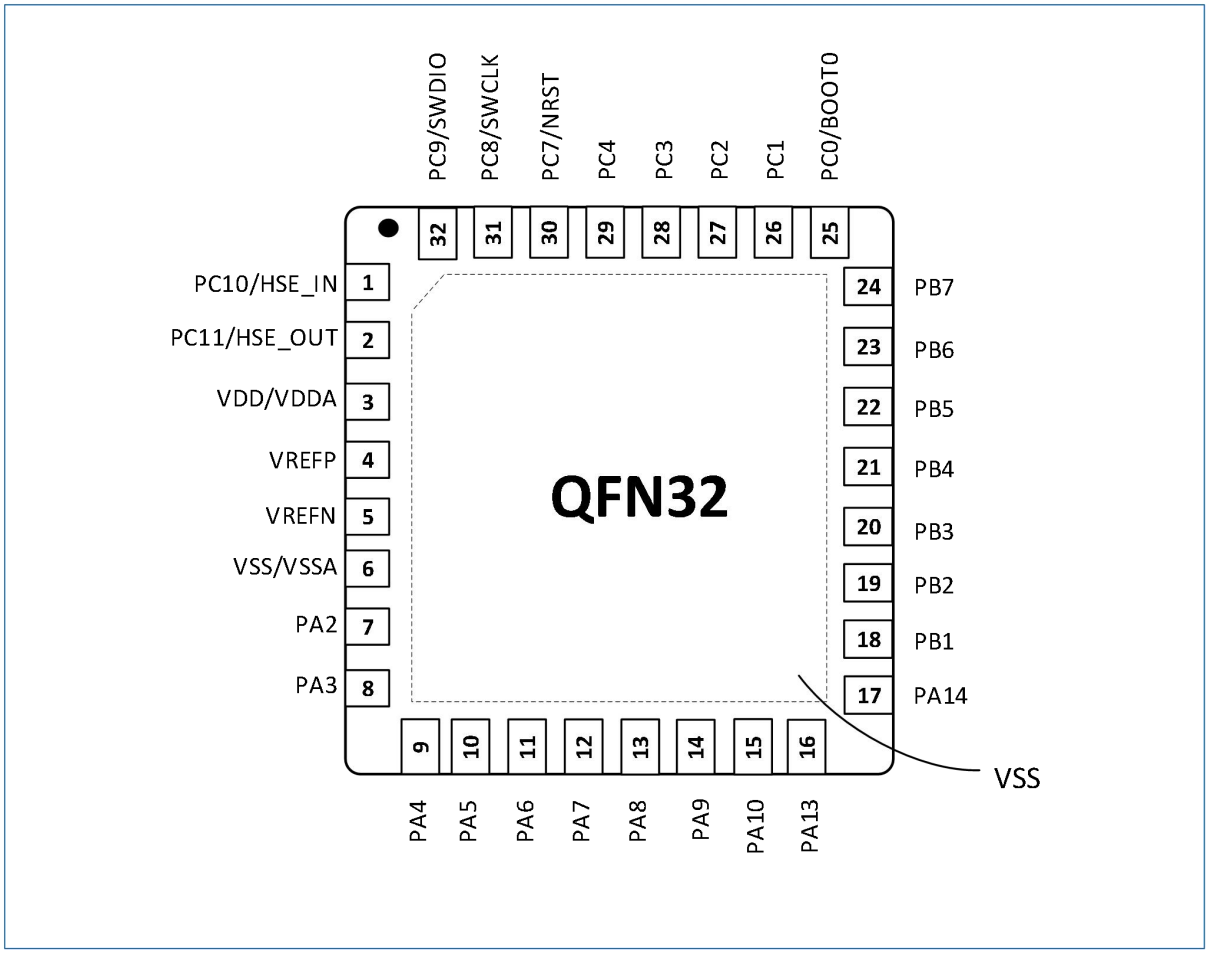

Figure 7- 2 QFN32 Pins

7.3 LQFP32 Package

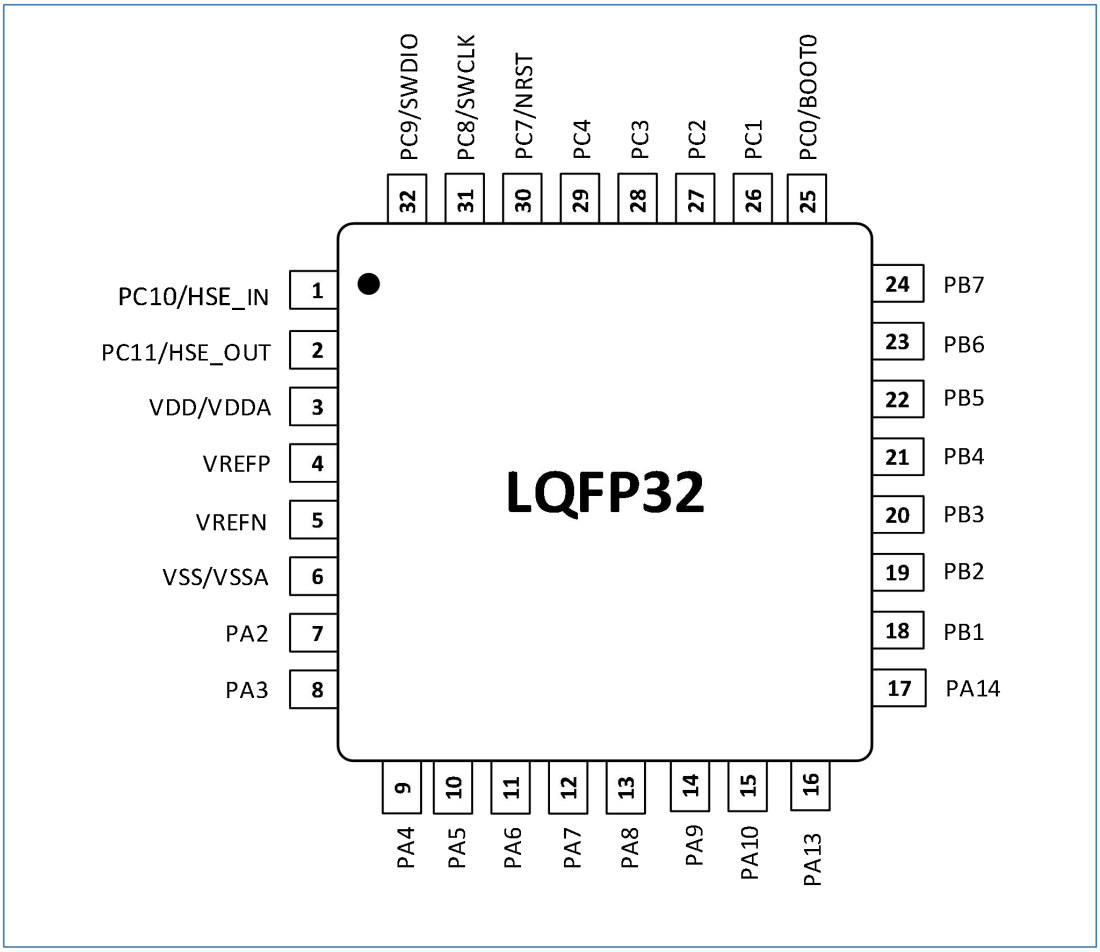

Figure 7- 3 LQFP32 Pin

7.4 QFN48 Package

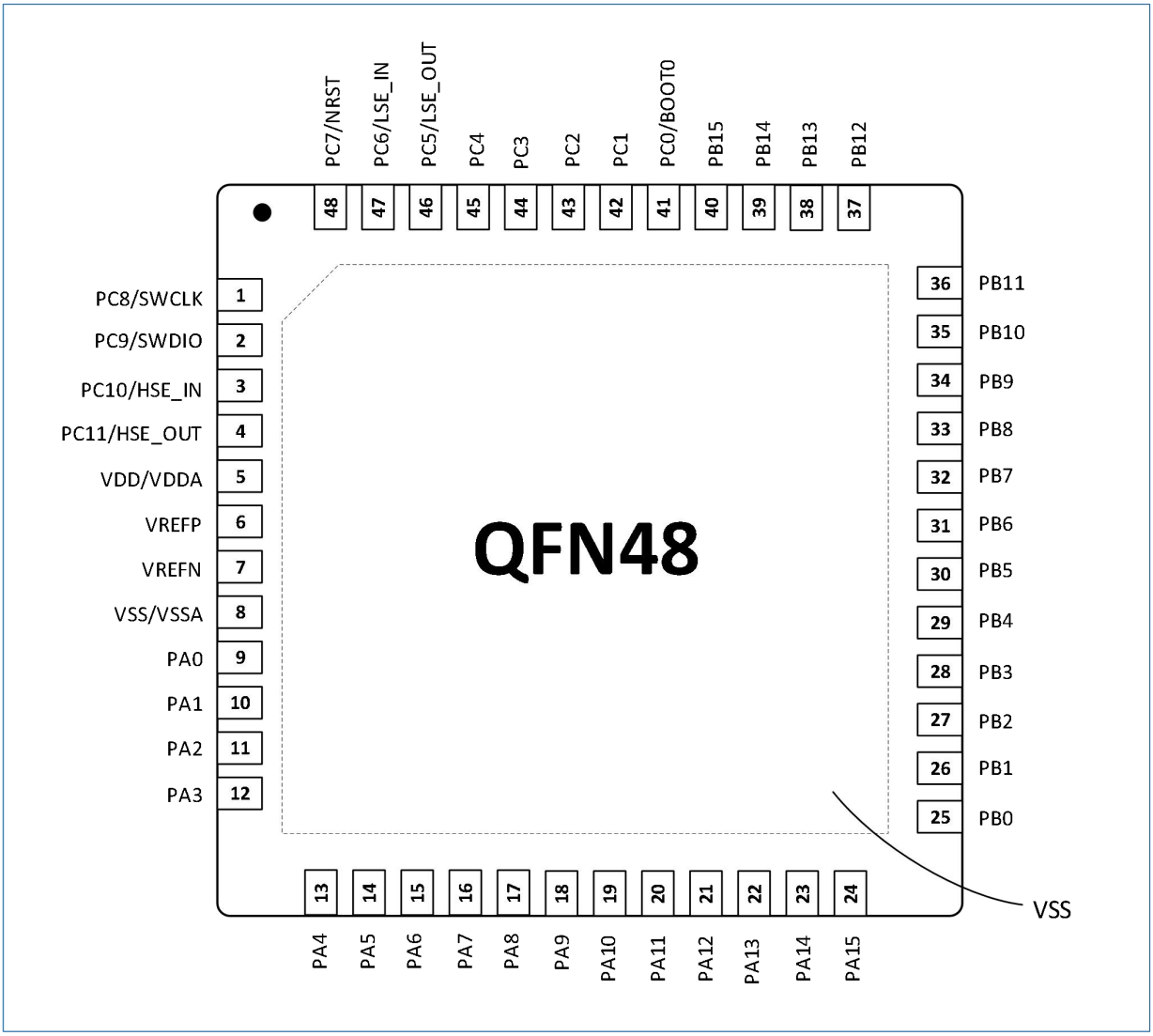

Figure 7-4 QFN48 Pin

7.5 LQFP48 Package

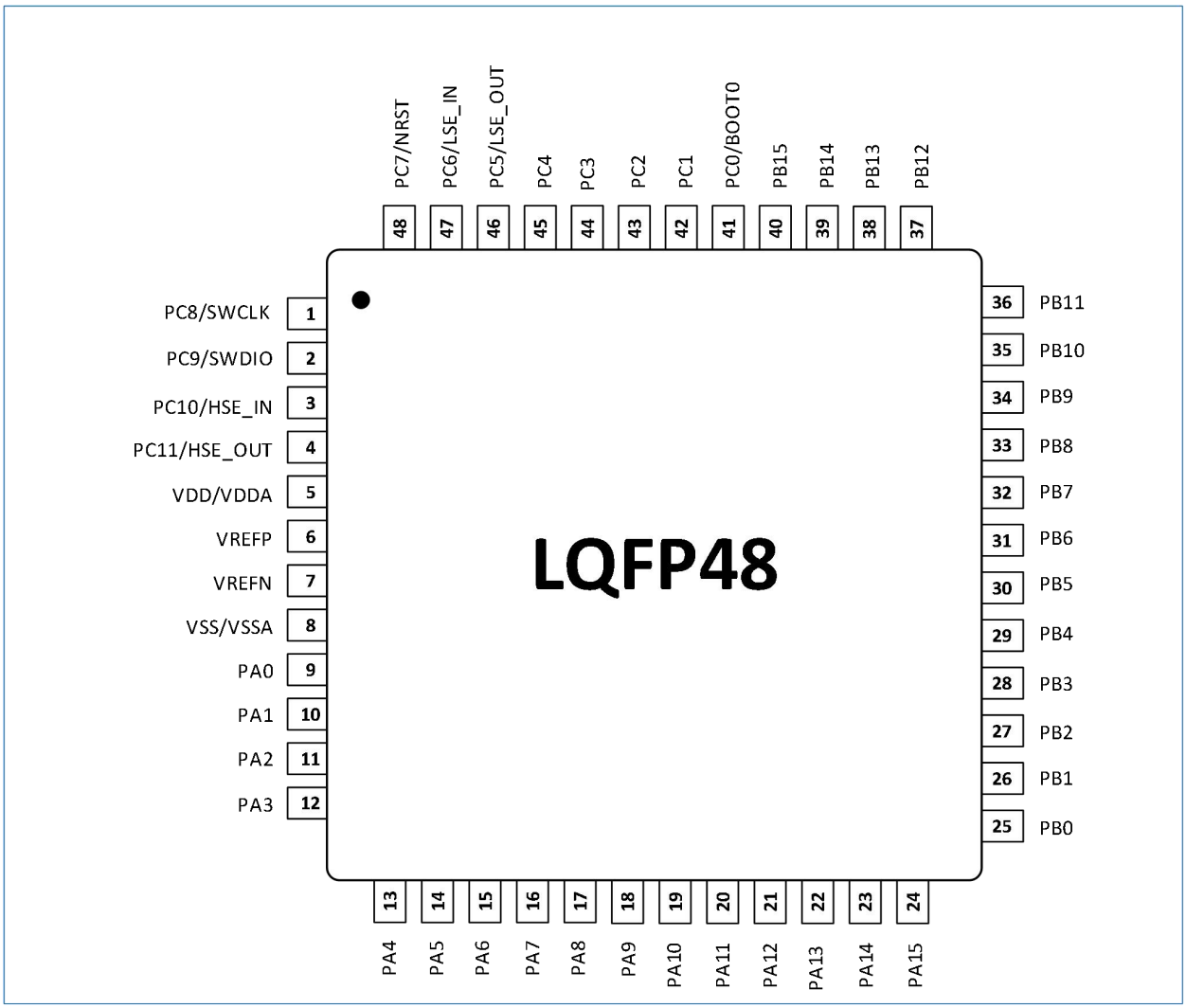

Figure 7-5 LQFP48 Pin

7.6 Pin Definition

Table 7-1 Pin Definition

LQFP48	QFN48	LQFP32	QFN32	TSSOP28	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
1	1	31	31	25	PC8/SWCLK (SWCLK)	I/O	FT	CM0_SWCLK UART1_TX/UART1_RX ADC_EXT_TRIG	COMP1_INN1 EXTIN8
2	2	32	32	26	PC9/SWDIO (SWDIO)	I/O	FT	CM0_SWDIO UART1_RX/UART1_TX ADC_EXT_TRIG	COMP2_INN1 EXTIN9
3	3	1	1	27	PC10/HSE_IN (PC10)	I/O	-	-	HSE_IN COMP3_INN1 OPA3_INN1 EXTIN10

LQFP48	QFN48	LQFP32	QFN32	TSSOP28	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
4	4	2	2	28	PC11/HSE_OUT (PC11)	I/O	-	-	HSE_OUT COMP4_INN1 OPA3_OUT2 EXTIN11
5	5	3	3	1	VDD/VDDA	S	-	Digital/Analog power supply	
6	6	4	4	1	VREFP	S	-	Reference power supply	
7	7	5	5	2	VREFN	S	-	Reference power supply ground	
8	8	6	6	2	VSS/VSSA	S	-	Digital/Analog ground	
-	0	-	0	2	VSS	S	-	Digital ground (Pin 0 is the thermal pad on the QFN package bottom.)	
9	9	-	-	-	PA0	I/O	FT	-	CKI_4 ADC_IN0 EXTIN0
10	10	-	-	-	PA1	I/O	FT	-	ADC_IN1 EXTIN1
11	11	7	7	3	PA2	I/O	FT	TIM3_CH1 COMP4_OUT	ADC_IN2 OPA2_OUT1 EXTIN2
12	12	8	8	4	PA3	I/O	FT	COMP3_OUT	ADC_IN3 OPA2_INN1 EXTIN3
13	13	9	9	-	PA4	I/O	FT	COMP1_OUT	CKI_1 ADC_IN4 EXTIN4
14	14	10	10	5	PA5	I/O	FT	COMP2_OUT TRACE_TX	ADC_IN5 DAC1_OUT EXTIN5
15	15	11	11	6	PA6	I/O	FT	RCC_MCO	ADC_IN6 COMP1_INP1 EXTIN6
16	16	12	12	7	PA7	I/O	FT	-	ADC_IN7 OPA1_OUT1 COMP2_INP1 EXTIN7
17	17	13	13	8	PA8	I/O	FT	RCC_MCO	ADC_IN8 OPA1_INN1 COMP3_INP1 EXTIN8

LQFP48	QFN48	LQFP32	QFN32	TSSOP28	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
18	18	14	14	9	PA9	I/O	FT	-	ADC_IN9 COMP4_INP1 OPA1_INP2 OPA2_INP2 EXTIN9
19	19	15	15	10	PA10	I/O	FT	-	COMP1_INN0 COMP2_INN0 COMP3_INN0 COMP4_INN0 OPA3_INP1 EXTIN10
20	20	-	-	-	PA11	I/O	FT	-	OPA2_OUT0 OPA3_OUT1 EXTIN11
21	21	-	-	-	PA12	I/O	FT	-	OPA2_INN0 EXTIN12
22	22	16	16	11	PA13	I/O	FT	-	OPA1_INP1 OPA2_INP1 EXTIN13
23	23	17	17	12	PA14	I/O	FT	-	OPA1_PGA_N OPA2_PGA_N COMP1_INP0 COMP2_INP0 COMP3_INP0 COMP4_INP0 OPA3_INP0 EXTIN14
24	24	-	-	-	PA15	I/O	FT	-	OPA1_OUT0 OPA3_OUT0 EXTIN15
25	25	-	-	-	PB0	I/O	FT	-	OPA1_INN0 OPA3_INN0 EXTIN0
26	26	18	18	13	PB1	I/O	FT	-	OPA1_INP0 OPA2_INP0 EXTIN1
27	27	19	19	14	PB2	I/O	FT	TIM1_CH3N TIM1_CH1 TIM1_CH1N	EXTIN2
28	28	20	20	15	PB3	I/O	FT	TIM1_CH3 TIM1_CH2 TIM1_CH2N	EXTIN3

LQFP48	QFN48	LQFP32	QFN32	TSSOP28	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
29	29	21	21	16	PB4	I/O	FT	TIM1_CH2N TIM1_CH3 TIM1_CH3N	EXTIN4
30	30	22	22	17	PB5	I/O	FT	TIM1_CH2 TIM1_CH1N TIM1_CH1	EXTIN5
31	31	23	23	18	PB6	I/O	FT	TIM1_CH1N TIM1_CH2N TIM1_CH2	EXTIN6
32	32	24	24	19	PB7	I/O	FT	TIM1_CH1 TIM1_CH3N TIM1_CH3 RCC_MCO	EXTIN7
33	33	-	-	-	PB8	I/O	FT	TIM1_ETR	EXTIN8
34	34	-	-	-	PB9	I/O	FT	TIM1_BKIN	EXTIN9
35	35	-	-	-	PB10	I/O	FT	TIM1_CH1 TIM1_CH3 ADC_EXT_TRIG SPI_CLK UART2_RX/UART2_TX	EXTIN10
36	36	-	-	-	PB11	I/O	FT	TIM1_CH2 ADC_EXT_TRIG SPI_CS UART2_TX/UART2_RX	EXTIN11
37	37	-	-	-	PB12	I/O	FT	TIM1_CH1 TIM1_CH3 I2C_SCL UART2_DE	EXTIN12
38	38	-	-	-	PB13	I/O	FT	TIM1_CH1N TIM1_CH3N SPI_MISO UART1_RX/UART1_TX	EXTIN13
39	39	-	-	-	PB14	I/O	FT	TIM1_CH2N SPI_MOSI UART1_TX/UART1_RX	EXTIN14
40	40	-	-	-	PB15	I/O	FT	TIM1_CH3N TIM1_CH1N I2C_SDA UART1_DE	EXTIN15
41	41	25	25	20	PC0/BOOT0	I/O	FT	TIM1_ETR	EXTIN0

LQFP48	QFN48	LQFP32	QFN32	TSSOP28	Pin Name (default function after resets)	Pin Type(1)	5 V-tolerant	Alternate Function	Additional Function
					(PC0)			ADC_EXT_TRIG TIM2_CH4	
42	42	26	26	21	PC1	I/O	FT	TIM2_CH3 SPI_CLK	EXTIN1
43	43	27	27	22	PC2	I/O	FT	TIM2_CH2 TIM3_CH3 SPI_CS	EXTIN2
44	44	28	28	23	PC3	I/O	FT	TIM2_CH1 TIM3_CH2 SPI_MISO	EXTIN3
45	45	29	29	-	PC4	I/O	FT	TIM3_CH1 SPI_MOSI TRACE_TX	CKI_3 OPA3_INP2 EXTIN4
46	46	-	-	-	PC5/LSE_OUT (PC5)	I/O	-	TIM3_CH2 I2C_SCL	LSE_OUT EXTIN5
47	47	-	-	-	PC6/LSE_IN (PC6)	I/O	-	TIM3_CH3 I2C_SDA	LSE_IN EXTIN6
48	48	30	30	30	PC7/NRST (PC7)	I/O	FT	TIM3_CH4	NRST EXTIN7

(1). I = input, O = output, I/O = input/output, S = power supply.

Note:

- Unless otherwise specified, all I/Os are configured in analog input mode during and after resets.
- For details on alternate functions, refer to “Alternative Function table”

7.7 Alternative Function Table

Table 7-2 Alternative Function Table

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PC8	SWCLK	ADC_EXT_TRIG	-	-	-	-	UART1_TX	-
PC9	SWDIO	ADC_EXT_TRIG	-	-	-	-	UART1_RX	-
PC10	-	-	-	-	-	-	-	-
PC11	-	-	-	-	-	-	-	-
PA0-AIN0	-	-	-	-	-	-	-	-
PA1-AIN1	-	-	-	-	-	-	-	-

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA2-AIN2	COMP4_OUT	-	-	-	-	TIM3_CH1	-	-
PA3-AIN3	COMP3_OUT	-	-	-	-	-	-	-
PA4-AIN4	COMP1_OUT	-	-	-	-	-	-	-
PA5-AIN5	COMP2_OUT	-	-	-	-	-	TRACE_TX	-
PA6-AIN6	RCC_MCO	-	-	-	-	-	-	-
PA7-AIN7	-	-	-	-	-	-	-	-
PA8-AIN8	RCC_MCO	-	-	-	-	-	-	-
PA9-AIN9	-	-	-	-	-	-	-	-
PA10	-	-	-	-	-	-	-	-
PA11	-	-	-	-	-	-	-	-
PA12	-	-	-	-	-	-	-	-
PA13	-	-	-	-	-	-	-	-
PA14	-	-	-	-	-	-	-	-
PA15	-	-	-	-	-	-	-	-
PB0	-	-	-	-	-	-	-	-
PB1	-	-	-	-	-	-	-	-
PB2	-	-	TIM1_CH3N	TIM1_CH1	TIM1_CH1N	-	-	-
PB3	-	-	TIM1_CH3	TIM1_CH2	TIM1_CH2N	-	-	-
PB4	-	-	TIM1_CH2N	TIM1_CH3	TIM1_CH3N	-	-	-
PB5	-	-	TIM1_CH2	TIM1_CH1N	TIM1_CH1	-	-	-
PB6	-	-	TIM1_CH1N	TIM1_CH2N	TIM1_CH2	-	-	-
PB7	RCC_MCO	-	TIM1_CH1	TIM1_CH3N	TIM1_CH3	-	-	-
PB8	-	-	TIM1_ETR	-	-	-	-	-
PB9	-	-	TIM1_BKIN	-	-	-	-	-

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PB10	-	ADC_EXT_TRIG	TIM1_CH3	TIM1_CH1	-	-	UART2_RX	SPI_CLK
PB11	-	ADC_EXT_TRIG	TIM1_CH2	TIM1_CH2	-	-	UART2_TX	SPI_CS
PB12	-	-	TIM1_CH1	TIM1_CH3	-	-	UART2_DE	I2C_SCL
PB13	-	-	TIM1_CH3N	TIM1_CH1N	-	-	UART1_RX	SPI_MISO
PB14	-	-	TIM1_CH2N	TIM1_CH2N	-	-	UART1_TX	SPI_MOSI
PB15	-	-	TIM1_CH1N	TIM1_CH3N	-	-	UART1_DE	I2C_SDA
PC0	-	ADC_EXT_TRIG	TIM1_ETR	-	TIM2_CH4	-	-	-
PC1	-	-	-	-	TIM2_CH3	-	-	SPI_CLK
PC2	-	-	-	-	TIM2_CH2	TIM3_CH3	-	SPI_CS
PC3	-	-	-	-	TIM2_CH1	TIM3_CH2	-	SPI_MISO
PC4	-	-	-	-	-	TIM3_CH1	TRACE_TX	SPI_MOSI
PC5	-	-	-	-	-	TIM3_CH2	-	I2C_SCL
PC6	-	-	-	-	-	TIM3_CH3	-	I2C_SDA
PC7-NRST	-	-	-	-	-	TIM3_CH4	-	-

8 Packages

8.1 Package Outline

8.1.1 TSSOP28 Package

TSSOP28 is a 9.70 mm x 4.40 mm,0.65 mm pitch package.

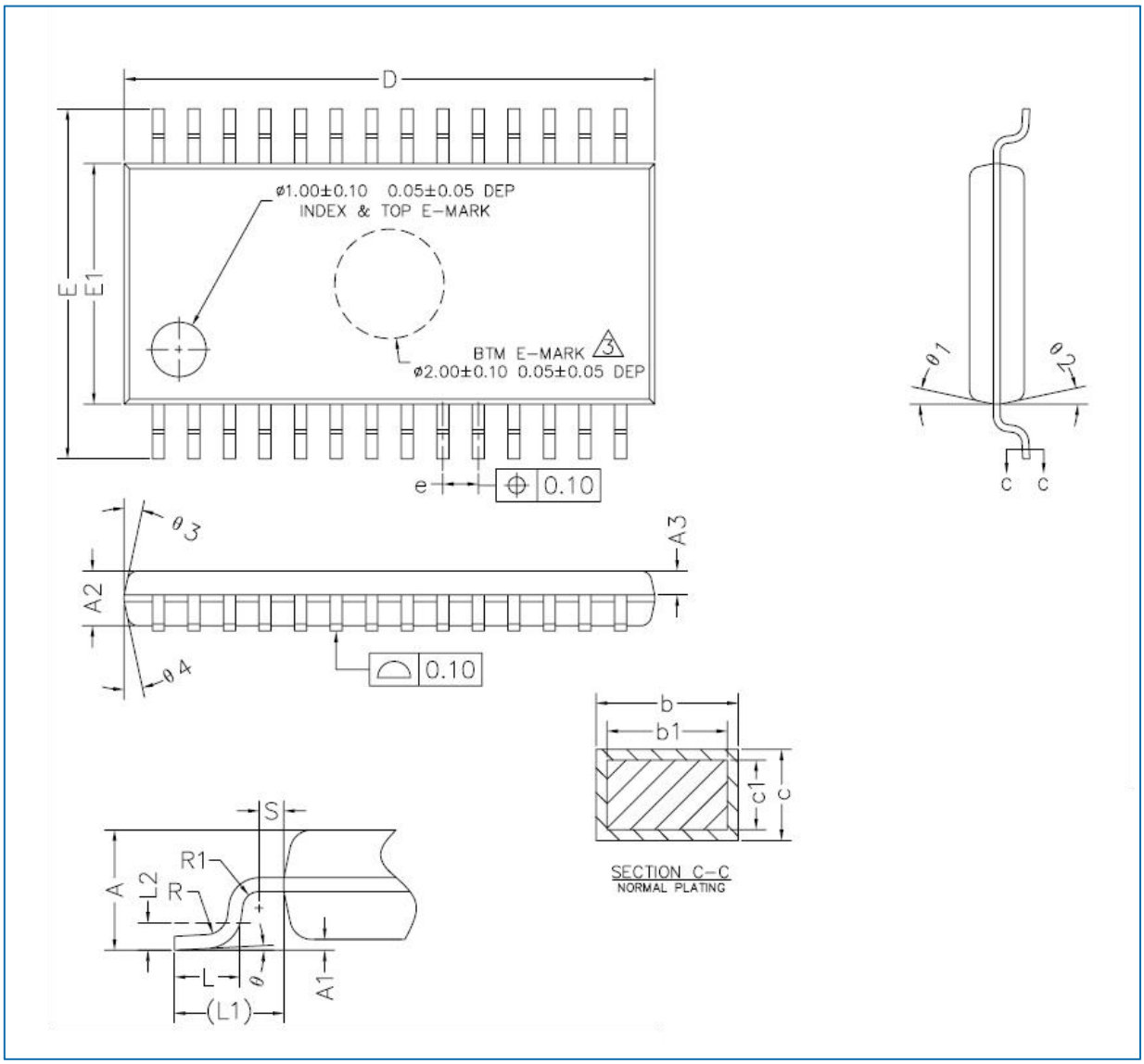

Figure 8-1 TSSOP28 Outline

Table 8-1 TSSOP28 mechanical data

Symbol	Min(mm)	Typ(mm)	Max(mm)
A	-	-	1.20
A1	0.03	0.08	0.12
A2	0.80	-	1.00
A3	0.39	0.44	0.49
b	0.20	-	0.29
b1	0.19	0.22	0.25
c	0.14	-	0.18

Symbol	Min(mm)	Typ(mm)	Max(mm)
c1	0.12	0.13	0.14
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
L2		0.25BSC	
R	0.09	-	-
R1	0.09	-	-
S	0.20	-	-
θ	0°	--	8°
θ1	10°	12°	14°
θ2	10°	12°	14°
θ3	10°	12°	14°
θ4	10°	12°	14°

8.1.2 QFN32 Package

QFN32 is a 5 mm x 5 mm, 0.5 mm pitch package.

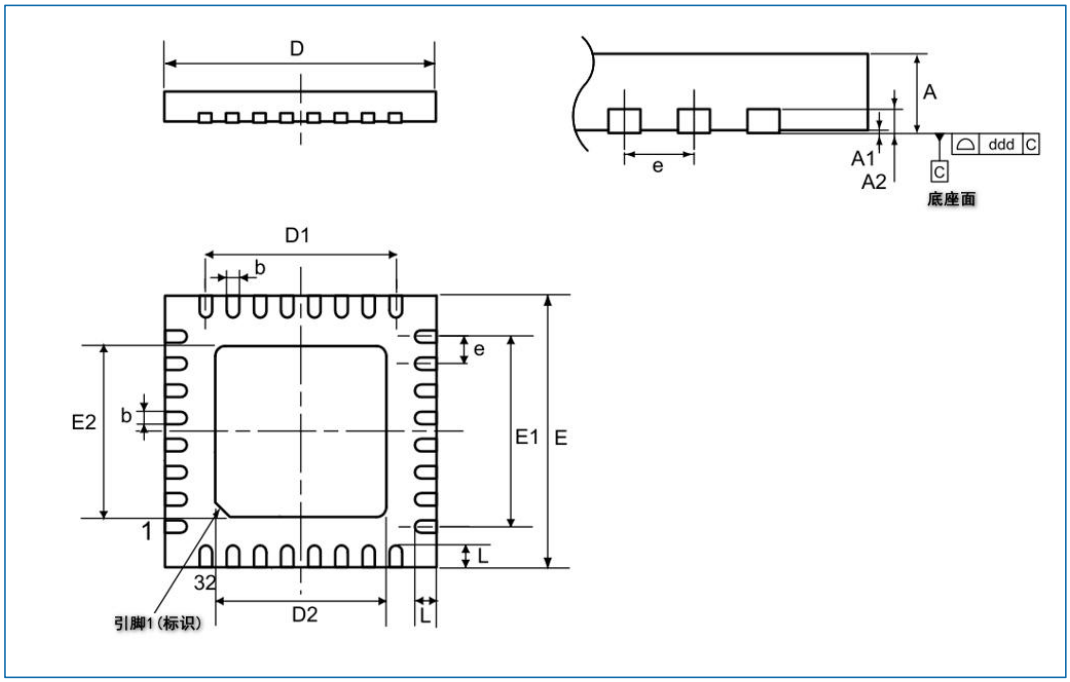

Figure 8-2 QFN32 Outline

Table 8-2 QFN32 mechanical data

Symbol	Min(mm)	Typ(mm)	Max(mm)	Min(inches) (1)	Typ(inches) (1)	Max(inches) (1)
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.500	0.550	0.600	0.0197	0.0217	0.0236

Symbol	Min(mm)	Typ(mm)	Max(mm)	Min(inches) (1)	Typ(inches) (1)	Max(inches) (1)
A2	0.000	0.020	0.050	0.0000	0.0008	0.0020
A3	-	0.152	-	-	0.0060	-
b	0.180	0.230	0.280	0.0071	0.0091	0.0110
D	4.900	5.000	5.100	0.1929	0.1969	0.2008
D1	3.400	3.500	3.600	0.1339	0.1378	0.1417
D2	3.400	3.500	3.600	0.1339	0.1378	0.1417
E	4.900	5.000	5.100	0.1929	0.1969	0.2008
E1	3.400	3.500	3.600	0.1339	0.1378	0.1417
E2	3.400	3.500	3.600	0.1339	0.1378	0.1417
e	-	0.500	-	-	0.0197	-
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
ddd	-	-	0.080	-	-	0.0031

(1). Values in inches are converted from mm and rounded to 4 decimal digits.

8.1.3 LQFP32 Package

LQFP32 is a 7mm x7mm, 0.8 mm pitch package.

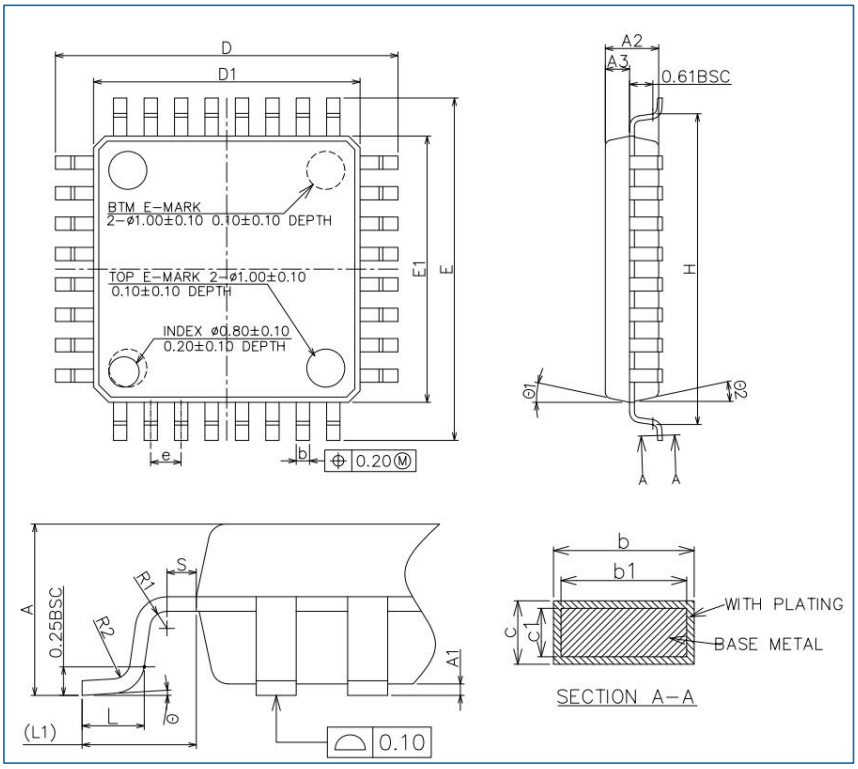

Figure 8-3 LQFP32 Outline

Table 8-3 LQFP32 mechanical data

Symbol	Min(mm)	Typ(mm)	Max(mm)	Min(inches) (1)	Typ(inches) (1)	Max(inches) (1)
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571

Symbol	Min(mm)	Typ(mm)	Max(mm)	Min(inches) (1)	Typ(inches) (1)	Max(inches) (1)
b	0.33	-	0.42	0.0130	-	0.0165
b1	0.32	0.35	0.38	0.0126	0.0138	0.0150
c	0.13	-	0.18	0.0051	-	0.0071
c1	0.117	0.127	0.137	0.0046	0.0050	0.0054
D	8.80	9.00	9.20	0.3465	0.3543	0.3622
D1	6.90	7.00	7.10	0.2717	0.2756	0.2795
E	8.80	9.00	9.20	0.3465	0.3543	0.3622
E1	6.90	7.00	7.10	0.2717	0.2756	0.2795
e	0.70	0.80	0.90	0.0276	0.0315	0.0354
H	8.14	8.17	8.20	0.3205	0.3217	0.3228
L	0.50	-	0.70	0.0197	-	0.0276
L1	-	1.00	-	-	0.0394	-
R1	0.08	-	-	0.0031	-	-
R2	0.08	-	0.20	0.0031	-	0.0079
S	0.20	-	-	0.0079	-	-
θ	0°	3.5°	7°	-	-	-
θ1	11°	12°	13°	-	-	-
θ2	11°	12°	13°	-	-	-

(1). Values in inches are converted from mm and rounded to 4 decimal digits.

8.1.4 QFN48 Package

QFN48 is a 7mm x7mm, 0.5 mm pitch package

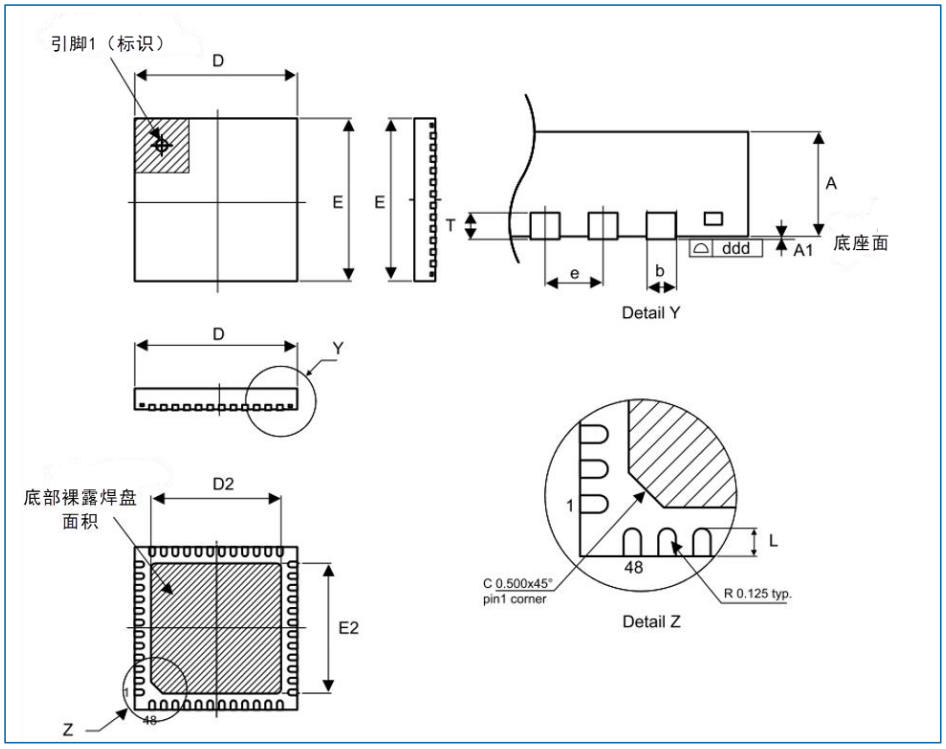

Figure 8-4 QFN48 Outline

Table 8-4 QFN48 mechanical data

Symbol	Min(mm)	Typ(mm)	Max(mm)	Min(inches) (1)	Typ(inches) (1)	Max(inches) (1)
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

(1). Values in inches are converted from mm and rounded to 4 decimal digits.

8.1.5 LQFP48 Package

LQFP48 is a 7mm x7mm, 0.5 mm pitch package.

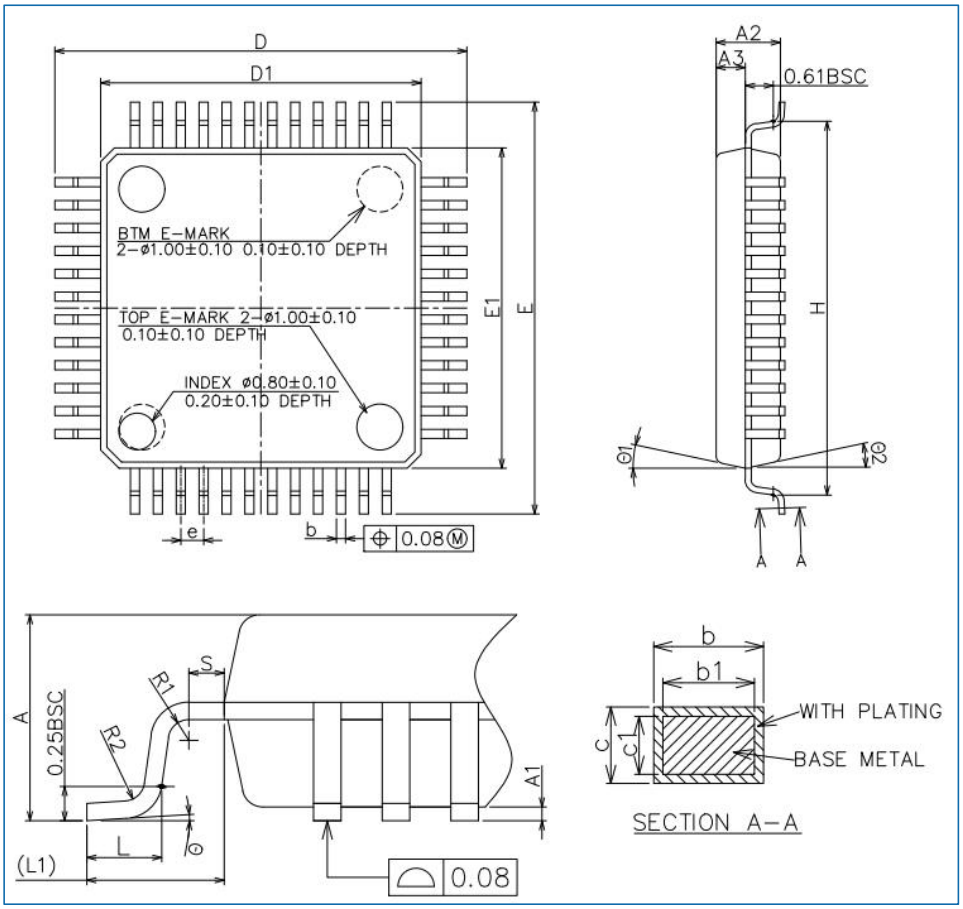

Figure 8-5 LQFP48 Outline

Table 8-5 LQFP48 mechanical data

Symbol	Min(mm)	Typ(mm)	Max(mm)
A	-	-	1.600
A1	0.050	-	0.150
A2	1.350	1.400	1.450
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50BSC		
H	8.14	8.17	8.20
L	0.40	-	0.65
L1	-	1.00REF	-
R1	0.08	-	-
R2	0.08	-	0.20
S	0.2	-	-
θ	0°	3.5°	8°
θ1	11°	12°	13°
θ2	11°	12°	13°

9 Acronyms

Abbreviation	Full Name
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-Wakeup
CSS	Clock Security System
CTS	Clear to Send
DMA	Direct Memory Access
EXTI	Extended Interrupts and Events Controller
GPIO	General Purpose Input Output
HSE	High Speed External（Clock Signal）
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-Speed Internal（Clock Signal）
MCU	Microcontroller Unit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-Down Reset
PGA	Programmable Gain Amplifier
PLL	Phase Locked Loop
POR	Power-On Reset
PPM	Parts per Million
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computing
RTS	Request to Send
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver Transmitter
WWDG	Window Watchdog

10 Version History

Version	Date	Changes
Rev.1.0	2025-07-03	Initial release

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