PMC1302A Datasheet

36V, 1.5A Synchronous Step-Down Regulator with 30μA Quiescent Current

Version：Preliminary Datasheet

Release Date：2025-06-25

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GENERAL DESCRIPTION

The PMC1302A is a high efficiency synchronous monolithic step-down switching regulator with integrated internal high-side and low-side MOSFETs. It provides up to 1.5A output current with peak current mode control for fast loop response.

The PMC1302A operates over a wide input voltage range from 3.0V to 36V with only 30µA low quiescent current.

Standard features include thermal shutdown, UVLO, enable (EN) control and power good (PG) indicator. During the overload or output short circuit, the cycle by cycle current limit and hiccup protection are provided. Thermal shutdown provides reliable and fault-tolerant operation.

FEATURES

- Wide Input Voltage Range: 3.0V to 36V
- 2.1MHz Switching Frequency
- 1.5A Output Current Capability
- Low Operating Quiescent Current: 30µA (Typ.) from $12V_{IN}$ to $3.3V_{OUT}$
- 1.5% 1V Reference Over -40°C~125°C
- Peak Eff. >93% (Typ.) From $12V_{IN}$ to $5V_{OUT}$
- Minimum On Time: 40ns (Typ.)
- Internal Compensation
- Precision Enable
- Cycle by Cycle Current Limit and Hiccup When Overload or Short Circuit
- Thermal Shutdown and Auto Recovery

APPLICATIONS

- Consumer systems: Robotic Vacuum Cleaner, Drone.
- Battery Powered System: Power Tools, Home Appliance, GPS Tracker etc.
- Industrial and Medical Power Supplies

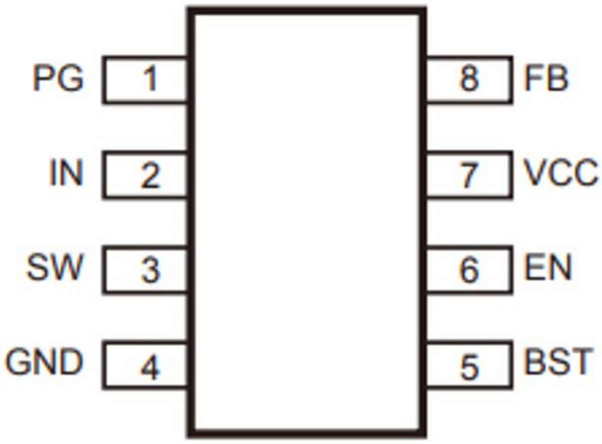
ORDERING INFORMATION

ORDER NUMBER	Marking ID	Package	Description
PMC1302AJA8	A1DNN	TSOT23-8	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel

MARKING INFORMATION

Marking	Package	Definition
A1DNN	TSOT23-8	A1: Product code;D:Date code ;NN: Serial number

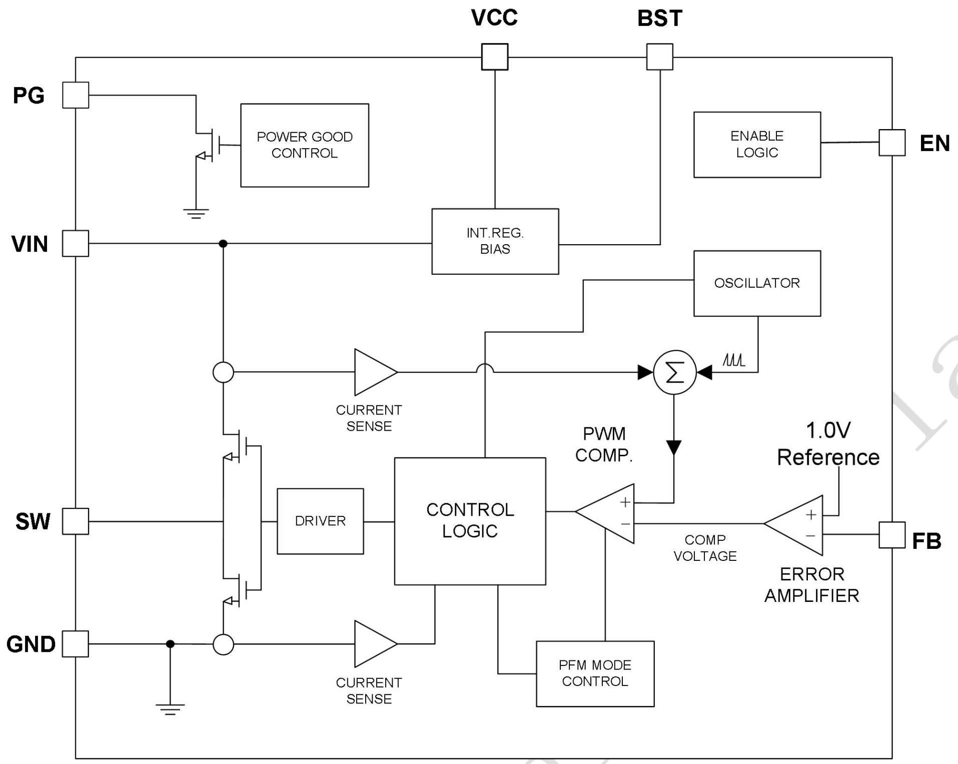
PIN CONFIGURATION



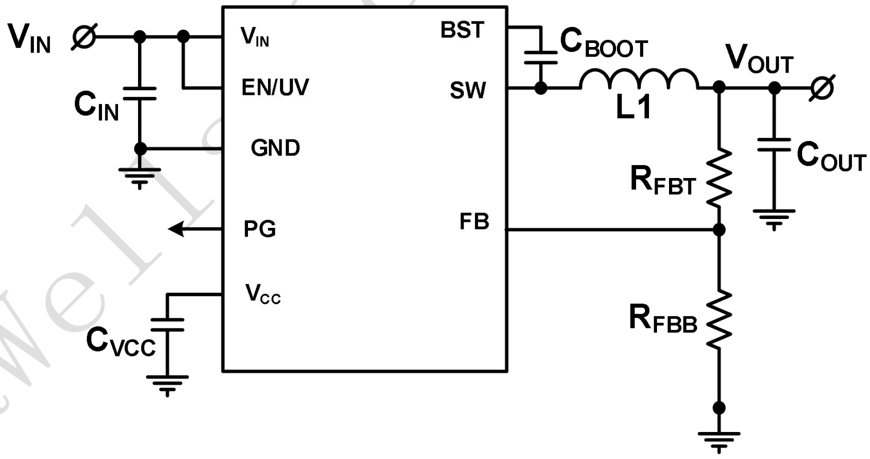
TSOT23-8 (TOP VIEW)

Terminal		Description
Pin No.	Name	
1	PG	Power Good Signal
2	IN	Input Voltage
3	SW	Switching Node Output
4	GND	Power Ground
5	BST	Bootstrap Supply Voltage
6	EN	Enable Input
7	VCC	Internal Supply for Control Circuits
8	FB	Feedback Voltage

FUNCTION BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
VIN, EN to GND	Input	-0.3 to 42	V
FB to GND		-0.3 to 5.5	
PG to GND		-0.3 to 6	
BST to SW		-0.3 to 5.5	
VCC to GND	Output	-0.3 to 6	V
SW to GND		-0.3 to 42	
T_J	Junction temperature	-40 to 150	°C
T_S	Storage temperature	-55 to 150	

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	RATING	UNIT
VIN	Buck Regulator	3.0 to 36	V
SW		0 to 36	
FB		0 to 5	
EN	Control	0 to 36	V
PG		0 to 5	
V_{OUT}	Output	0 to 24	V
T_J	Junction temperature	-40 to 125	°C

HANDLING RATINGS

SYMBOL	PARAMETER	VALUE	UNIT
V_{ESD}	Human Body Model (HBM) ESD stress voltage	±2000	V
	Charged Device Model (CDM) ESD stress voltage	±750	

ELECTRICAL CHARACTERISTICS

Limits apply over the recommended operating junction temperature 25°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12 V. V_{OUT} is converter output voltage.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SD}	Shutdown Supply Current	V_{EN}=0V			8	µA
I_Q	Non-Switching Quiescent Current	V_{FB}=1.05V			20	µA
R_{DSON_H}	High Side MOSFET ON Resistance			105	190	mΩ
R_{DSON_L}	Low Side MOSFET ON Resistance			65	135	mΩ
I_{LKG_SW}	Switch Leakage	V_{EN}=0V, V_{SW}=12V			1	µA
I_{LIMIT_H}	High Side MOSFET Current Limit (1)		2.5	3.5	4.8	A
I_{LIMIT_L}	Low Side MOSFET Current Limit (1)		2			A
f_{SW}	Switching Frequency		1.8	2.1	2.4	MHz
f_{FB}	Fold-Back Frequency	V_{FB}<700mV		1.5		MHz
D_{MAX}	Maximum Duty Cycle	V_{IN}=V_{OUT}=12V, I_{OUT}=1A	96	98.5		%
T_{ON_MIN}	Min. Turn On Time			40		ns
V_{FB}	Feedback voltage		0.985	1.00	1.015	V
I_{FB}	Current into FB pin	V_{FB}=1V	-100		100	nA
V_{EN_H}	Enable High Threshold		1.185	1.235	1.285	V
V_{EN_L}	Enable Low Threshold		0.95	1.03	1.09	V
V_{EN_HYS}	Enable Hysteresis Threshold			205		mV
V_{EN_LKG}	Enable Pin Leakage Current	V_{EN}=2V		-0.6		nA
V_{IN_UV}	Under Voltage Lockout Thresholds	Rising Threshold		2.85	3	V
		Falling Threshold	2.2	2.65		V
		Hysteresis		200		mV
V_{CC}	Internal Power Supply	4V≤V_{IN}, Iload=0mA	3.32	3.5	3.68	V
	VCC Load Regulation	4V≤V_{IN}, Iload=5mA		1.5	3	%
Tss	Internal Soft-Start Time		2	5	9	ms
T_{SD}	Thermal Shutdown			165		°C
T_{SD_HYS}				15		°C
V_{PG_R}	Power Good Threshold Rising	% of V_{FB}	91	94	97	%
V_{PG_F}	Power Good Threshold Falling	% of V_{FB}	89	92	95	%
PG_{Vth_HYS}	PG Threshold Hysteresis	% of V_{FB}		2		%
t_{PG}	Power Good Glitch Filter Delay		40	130	160	µs
R_{PG}	PG Pull-Down Resistance	V_{EN}=4V		95	250	Ω
		V_{EN}=0V		85	200	
I_{LKG_PG}	PG Leakage Current				100	nA

Note:

(1) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.

TYPICAL CHARACTERISTICS

Unless otherwise specified the following conditions apply: V_{IN} = 12V, f_{SW} = 2.1MHz, L=2.2uH, C_{OUT} =22uF, T_J =25° C

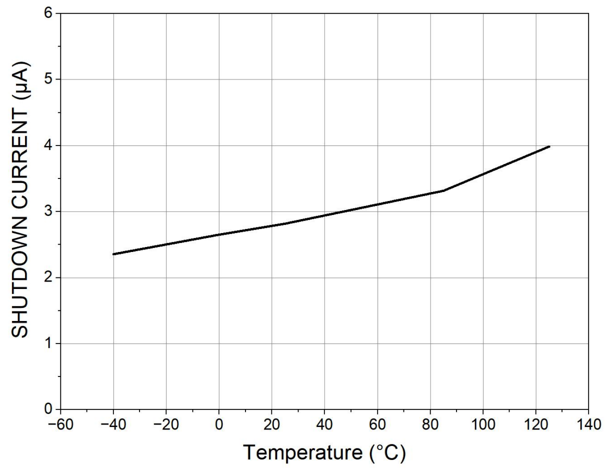


Figure 1. Shutdown Current VS. Junction Temperature

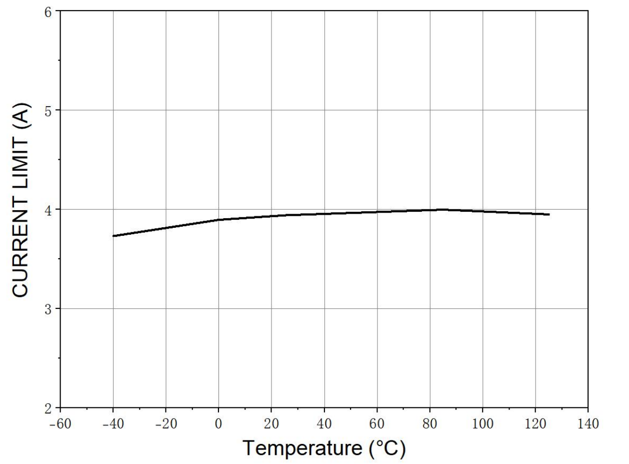


Figure 2. Current Limit VS. Junction Temperature at Duty = 40%

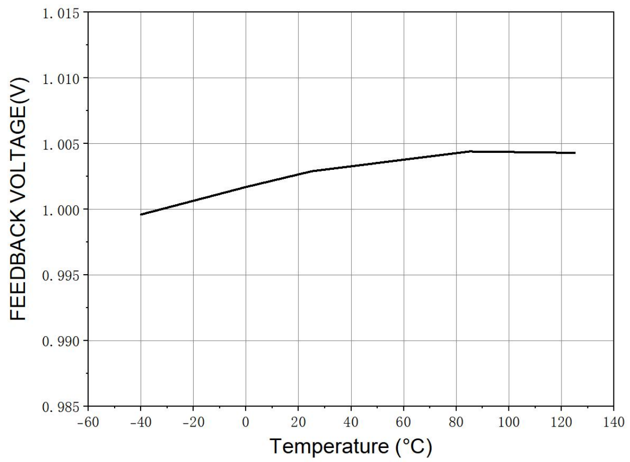


Figure 3. Feedback Voltage VS. Junction Temperature

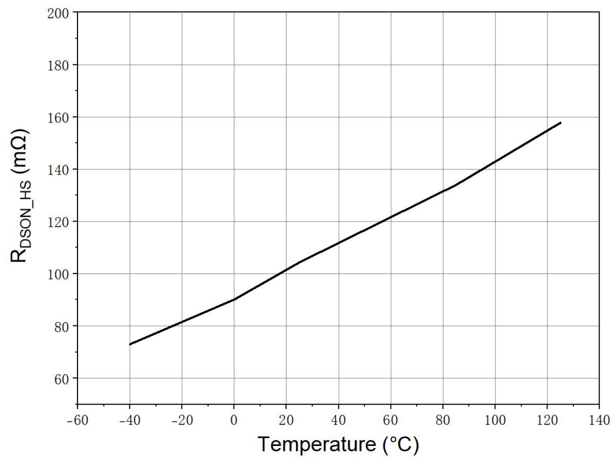


Figure 4. R_{DSON_HS} VS. Junction Temperature

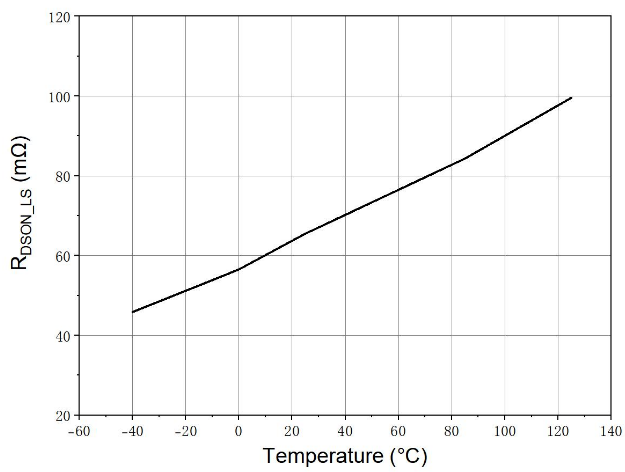


Figure 5. R_{DSON_LS} VS. Junction Temperature

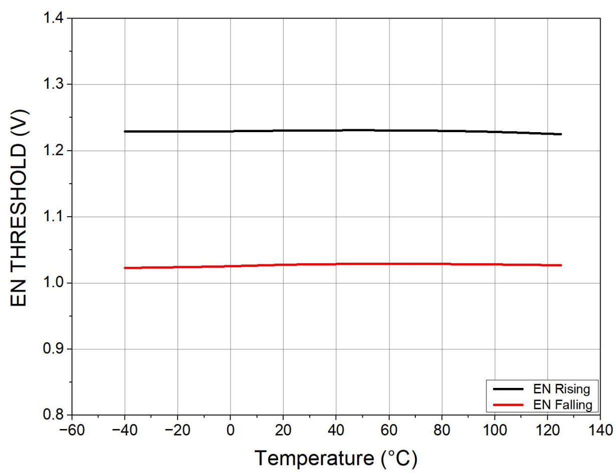


Figure 6. EN Threshold VS. Junction Temperature

TYPICAL CHARACTERISTICS (Continued)

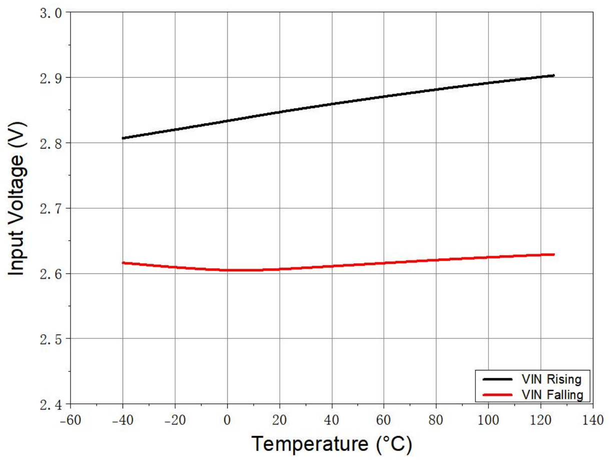


Figure 7. V_{IN} UVLO VS. Junction Temperature

FUNCTION DESCRIPTION

Overview

The PMC1302A is a synchronous, step-down,switching regulator with integrated high-side and low-side power MOSFETs. The PMC1302A can provide 1.5A of output current with very high efficiency from light load to full load. The PMC1302A features a wide input voltage from 3.0V to 36V, switching frequency 2.1 MHz. The internal soft start limits inrush current during power on. The PMC1302A also integrated compensation circuit inside the chip to simplify the loop design. Another highlighted feature is Its very low operational quiescent current which makes it suitable for battery powered applications.

Light Load Operation

The PMC1302A utilizes advanced Pulse Frequency Modulation (PFM) control to improve efficiency in light load working condition. When the loading current decreases, the device approaches discontinuous conduction mode first and the COMP voltage decreases accordingly. The low-side power switch is turned off when the zero current detection is triggered to improve system efficiency. When the COMP voltage drops to the low clamped threshold voltage, the device will skip pulse and decrease switching frequency by extend the non switching period. During this period, the output voltage decreases due to load current or capacitor discharge. The high-side power switch will resume to turn on once the COMP voltage is higher than the threshold. The device will try to obtain few switching pulses with minimum peak inductor current to reduce the output ripple and the COMP voltage will drop to the clamped value again and trigger another non-switching period.

Soft-Start with Pre-Biased Capability

The PMC1302A implements a soft-start circuits to prevent the inrush current during start up. The soft start time is fixed internally. When the start-up period begins, the output voltage slowly ramps up. The PMC1302A also supports a monotonic start-up with pre-biased loads. If output voltage is pre-biased to a certain value during start-up, the device disables switching for both high-side and low-side power switches until soft-start reference voltage exceeds the feedback voltage.

Over-Current Protection and Hiccup Mode

The PMC1302A has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. If, during current limit, the voltage on the FB input falls below about 0.5 V due to a short circuit, the device enters into hiccup mode. In this mode, the device stops switching for about 30 ms and then goes through a normal re-start with soft start. If the short-circuit condition remains, the device runs in current limit for about 5 ms (typical) and then shuts down again. This cycle repeats as long as the short circuit-condition persists. This mode of operation helps reduce the temperature rise of the device during a hard short on the output. The output current is greatly reduced during hiccup mode. Once the output short is removed and the hiccup delay is passed, the output voltage recovers normally.

Low Drop-out Mode

As the duty cycle is increasing, where the input voltage approaches the output voltage level, the required off time of high-side power switch will approach its minimum off time. When the minimum off time is reached, the PMC1302A will automatically extend the high-side on time and reduce the switching frequency. The device can realize 98.5% max duty cycle in drop-out condition. In this condition, the dropout voltage difference between input and output is influenced by the on-resistance of power switch, the DCR of power inductor, and the maximum duty cycle achieved.

Minimum On Time

As the duty cycle is decreasing, where the conversion ratio is very low, the required on time of high-side power switch will approach its minimum on time. The PMC1302A features typical 40ns ultra-low minimum on time and can support smaller duty cycle for high frequency power systems. Also, the device can automatically reduce the switching frequency, when the minimum on time is reached.

Power Good

The device employs an open-drain output PGOOD signal to check whether the output voltage is operating within the normal range. The external pull up voltage resource is recommended to be less than 5V (such as V_{CC}) with a 100kΩ resistor. Once the feedback voltage is within the 92% and 107% of internal reference voltage, the PGOOD pull-down will be disabled and pulled up by the externally resistor. Once the feedback voltage is lower than 92% or greater than 107% of internal reference voltage, the PGOOD will be pulled low. To prevent glitching both the upper and lower thresholds include about 2% of hysteresis. Also, if UVLO, over temperature protection or EN pin is pulled low, the PGOOD will be pulled low accordingly.

APPLICATION

Figure 8. shows a typical application circuit for the PMC1302A. Thanks to the high integration in the PMC1302A, the application circuit based on PMC1302A only need input capacitor, output capacitor, output inductor and feedback resistors which are needed to be selected based on applications specifications. "Table.1"shows some typical external component values.

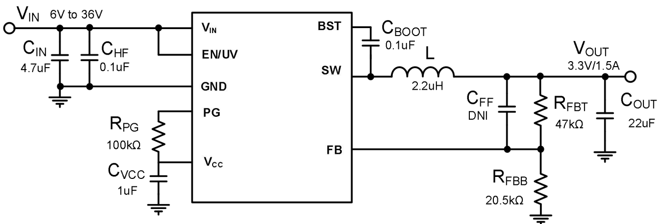


Figure 8. Typical Application Circuit (2.1MHz)

Setting Output Voltage

The external feedback resistors connected to FB sets the output voltage. The feedback resistors value can be calculated with the below equation.

$$R_{FBB} = \frac{V_{REF} R_{FBT}}{V_{OUT} - V_{REF}}$$

While R_{FBT}=47kΩ, V_{REF}=1V, V_{OUT}=3.3V

Calculate R_{FBB}≈20.5kΩ

Inductor Selection

For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 20% to 40% of the maximum load current. The minimum inductance value can be calculated with the below equation.

$$L = \frac{V_{OUT}(1 - D)}{f_{SW} \times \Delta I_L}$$

While V_{OUT}=3.3V, f_{SW}=2.1MHz, ΔI_L=30%×1.5A=0.45A, D=3.3V/12V=0.275

Calculate L≈2.2uH.

Output Capacitor Selection

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with equation. Generally, required the output voltage ripple is less than 1% of the output voltage.

$$\Delta V_{OUT} = \frac{V_{OUT} \times (1 - D)}{8 \times {f_{SW}}^2 \times L \times C_{OUT}}$$

Input Capacitor Selection

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (like X7R,C0G etc.) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. From the below equation, can easily calculate the input voltage ripple. Generally, required the input voltage ripple is less than 10% of the input voltage.

$$\Delta V_{IN} = \frac{I_O \times D \times (1 - D)}{f_{SW} \times C_{IN}}$$

Table.1 Typical External Component Values

f_{SW}(MHz)	V_{OUT}(V)	L(μH)	C_{OUT}(RATED CAPACITANCE)	R_{FBT} (kΩ)	R_{FBB} (kΩ)	C_{IN}+C_{HF}	C_{BOOT}	C_{VCC}	C_{FF}
2.1	3.3	2.2	22μF	47	20.5	4.7μF+100nF	100nF	1μF	DNI
2.1	5	2.2	22μF	47	11.8	4.7μF+100nF	100nF	1μF	DNI

C_{FF} Capacitor Selection

When some cases need improvement of load transient response or the margin of loop-phase, a feedforward capacitor can be used across R_{FBT}, especially when values of R_{FBT} > 1000kΩ are used. The minimum capacitation value can be calculated with the below equation.

$$C_{FF} \leq \frac{C_{OUT} \times V_{OUT}}{110 \times R_{FBT} \times \sqrt{\frac{R_{FBB}}{R_{FBT} + R_{FBB}}}}$$

Bootstrap Capacitor Selection

A bootstrap capacitor connected between the BST pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the internal MOSFETs. A ceramic capacitor of 0.1uF and 16V voltage rating is required.

VCC Capacitor Selection

The VCC pin is the output of the internal LDO used to supply the control circuits of the converter. This output requires a ceramic capacitor connected from VCC to GND for proper operation. It is highly recommended placing a ceramic capacitor of 1uF and 16V voltage rating. In general, avoid loading this output with any external circuitry. However, this output can be used to supply the pullup for the PGOOD function. The nominal output voltage on VCC is 3.5V. Do not short this output to ground or any other external voltage. Also, if over temperature protection or EN pin is pulled low, the VCC pin output will be low.

EN Resistor Selection

The PMC1302A has undervoltage lockout feature with default rising threshold of 2.85 V. It can be adjusted by using EN pin with external resistor divider. The UVLO threshold integrates a 200mV hysteresis to make a desired hysteresis for input voltage.

V_{UVLO_R} is the desired system level undervoltage protection rising threshold voltage, V_{UVLO_F} is the desired system level undervoltage protection falling threshold voltage. The R_{ENT} and R_{ENB} value can be calculated with the below equation.

$$V_{UVLO\_R} = \left(\frac{R_{ENT}}{R_{ENT} + R_{ENB}}\right) \times V_{ENR}$$

$$V_{UVLO\_F} = \left(\frac{R_{ENT}}{R_{ENT} + R_{ENB}}\right) \times (V_{ENR} - 0.2)$$

APPLICATION WAVEFORMS

Unless otherwise specified the following conditions apply: V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 2.1MHz, L=2.2uH, C_{OUT}=22uF, T_J =25°C.

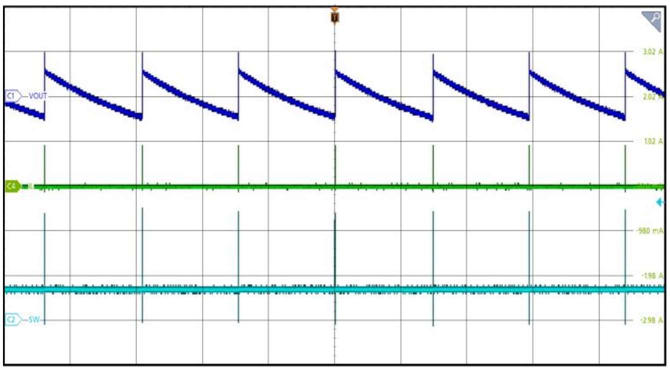


Figure 9. Steady State at V_{OUT}=3.3V, I_{LOAD}=0A

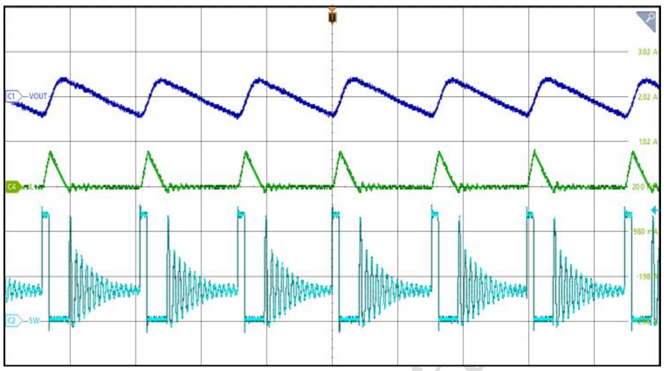


Figure 10. Steady State at V_{OUT}=3.3V, I_{LOAD}=100mA

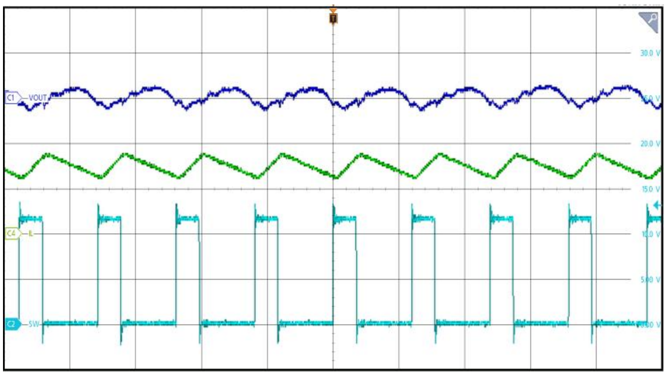


Figure 11. Steady State at V_{OUT}=3.3V, I_{LOAD}=1.5A

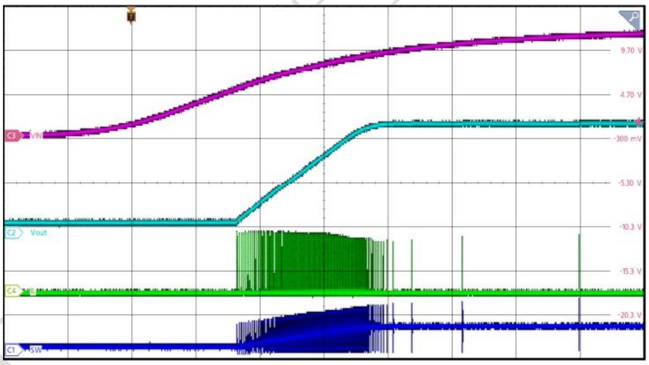


Figure 12. Startup through V_{IN} at I_{LOAD}=0A

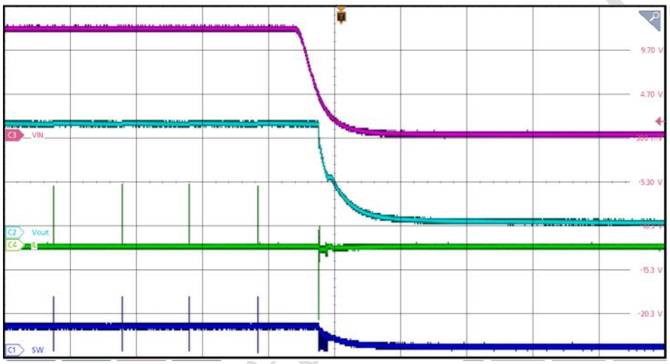


Figure 13. Startup through V_{IN} at I_{LOAD}=0A

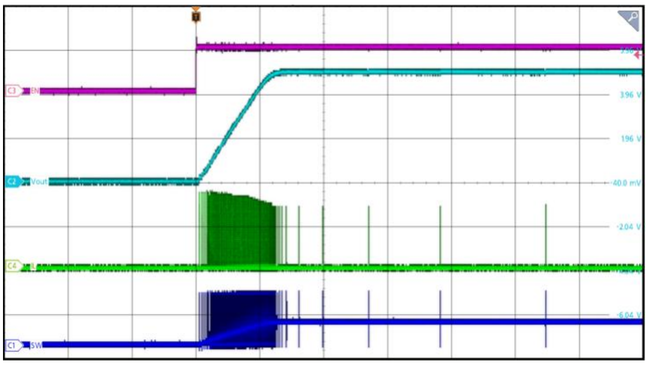


Figure 14. Startup through EN at I_{LOAD}=0A

APPLICATION WAVEFORMS (Continued)

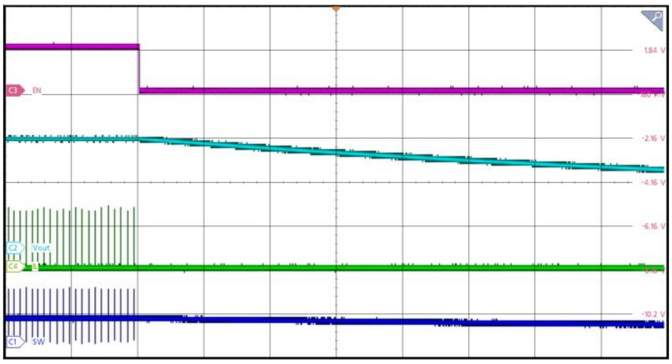


Figure 15. Shutdown through V_{IN} at I_{LOAD}=0A

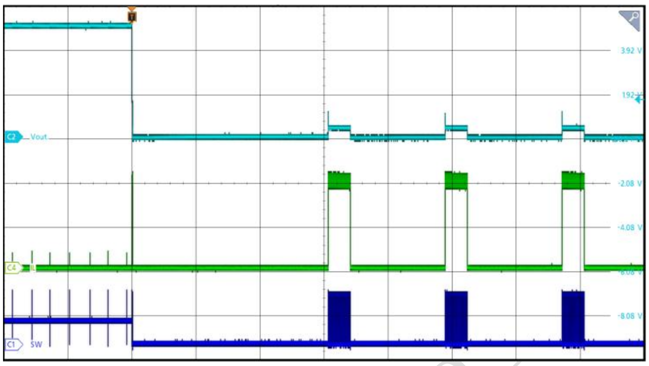


Figure 16. Short Circuit Protection at I_{LOAD}=0A

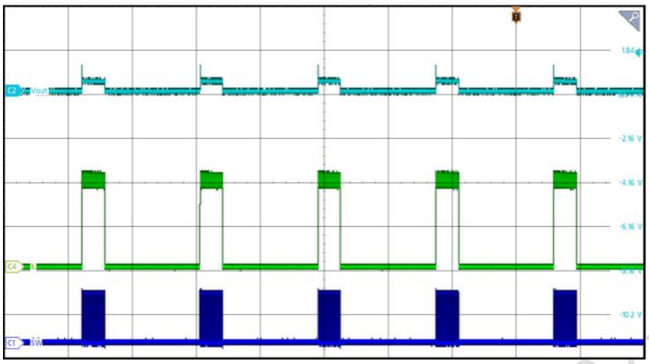


Figure 17. Short Circuit Steady

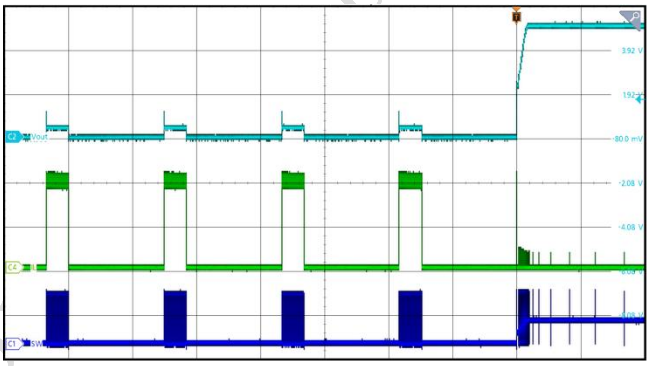


Figure 18. Short Circuit Recovery at I_{LOAD}=0A

PCB LAYOUT GUIDELINES

PCB layout is critical for stable operation of switching regulator PMC1302A, especially for thermal design and EMI design.

1. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible.

2. Make sure top switching loop with power have lowest impendence of grounding.

3. Use a large ground plane to connect to GND directly. And add vias near GND.

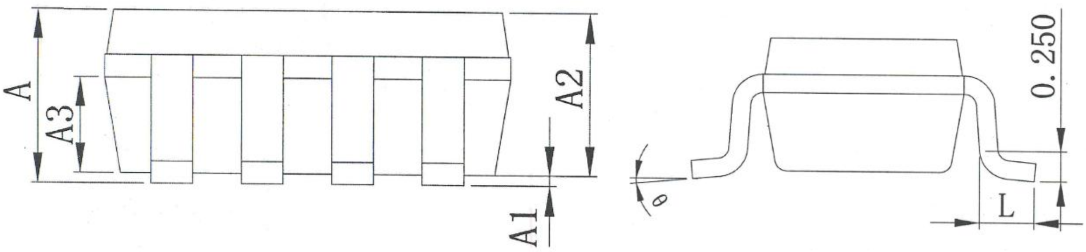
4. Output inductor should be placed close to the SW pin to minimize the SW area.

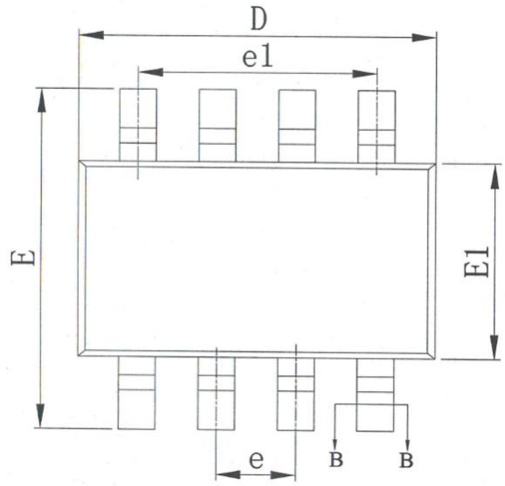
5. The FB terminal is sensitive to noise so the feedback resistor should be located as close as possible to the IC.

6. Keep the connection of the input capacitor and VIN as short and wide as possible.

PHYSICAL DIMENSIONS-TSOT23-8

Unit:mm





Symbol	Dimensions In Millimeters		
	MIN	NOM	MAX
A			0.95
A1	0.00	—	0.10
A2	0.75	0.80	0.85
A3	0.35	0.40	0.45
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.65BSC		
e1	1.95BSC		
L	0.30	0.40	0.50
θ	0	—	8°

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