PJ75230 Datasheet

Current and Power Monitor with I²C Compatible Interface

Version：Rev.1.1

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1 Product Description

The PJ75230 is a current shunt and power monitor with an I²C interface.

The PJ75230 monitors both shunt voltage drop and bus supply voltage. The device can directly read current in amperes and power in watts, with programmable calibration value, conversion times, and averaging options, combined with an internal multiplier. It supports up to 16 programmable addresses on I²C interface.

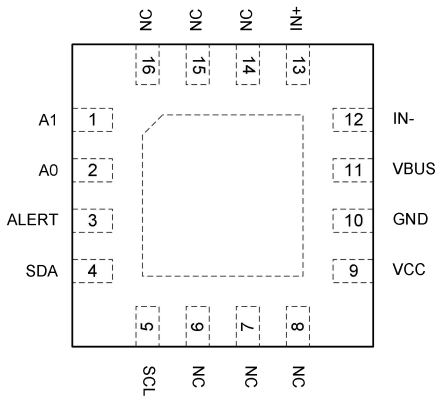
Applications

- **Server**
- **Telecom equipment**
- **Notebook Computers**
- **Power Management**
- **Battery Chargers**
- **Power Supplies**
- **Test Equipment**

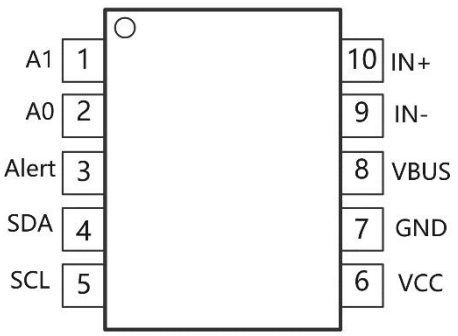
1.1 Product Features

- **Operating Voltage: 2.7V to 5.5V**
- **Bus Voltage (Input Voltage): 0V to 36 V**
- **16-Bit Delta-Sigma ADC**
- **Reports Current, Voltage, and Power**
- **Programmable Calibration Value, Conversion times, and Averaging Options**
- **High Accuracy:**
  - **0.3 % Gain Error (Max.)**
  - **25 μV Offset (Max.)**
- **Compatible with SMBus and I²C interface**
- **I²C Speed up to 2.94MHz (High-Speed Mode)**
- **Noise Filter on SCL/SDA inputs**
- **16 Programmable Addresses**
- **Operating temperature Range: -40°C to 125°C**
- **Available Package: QFN3X3-16, MSOP-10P**

1.2 PIN Configurations (Top View)



QFN3X3-16



MSOP-10P

1.3 Typical Application

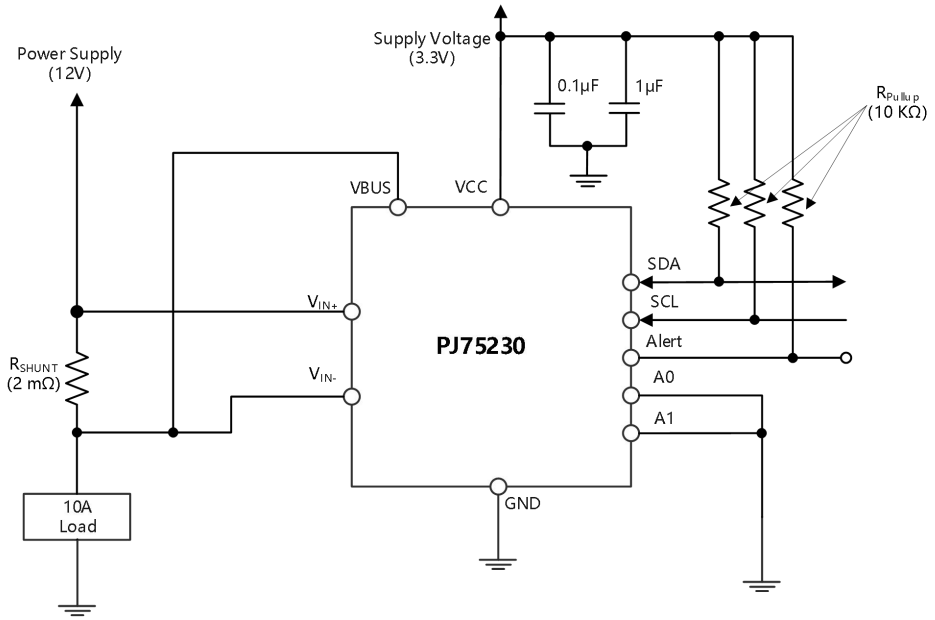


Figure 1-1 Typical Application of PJ75230

1.4 Pin Description

Pin Name	PIN No.		Type	Description
	QFN	MSOP		
A1	1	1	Digital Input	Address pin. Connect to GND, SCL, SDA, or VCC.
A0	2	2	Digital Input	Address pin. Connect to GND, SCL, SDA, or VCC.
Alert	3	3	Digital Output	Multi-functional alert, open-drain output. Can be floated.
SDA	4	4	Digital I/O	Serial bus data line, open-drain output & input.
SCL	5	5	Digital Input	Serial bus clock line.
NC	6	/	/	Not connected.
NC	7	/	/	Not connected.
NC	8	/	/	Not connected.
VCC	9	6	Power	Power supply, 2.7V to 5.5 V.
GND	10	7	Ground	Ground.
VBUS	11	8	Analog Input	Bus voltage input.
IN-	12	9	Analog Input	Connect to load side if shunt resistor.
IN+	13	10	Analog Input	Connect to supply side of shunt resistor.
NC	14	/	/	Not connected.
NC	15	/	/	Not connected.
NC	16	/	/	Not connected.

1.5 Function Block

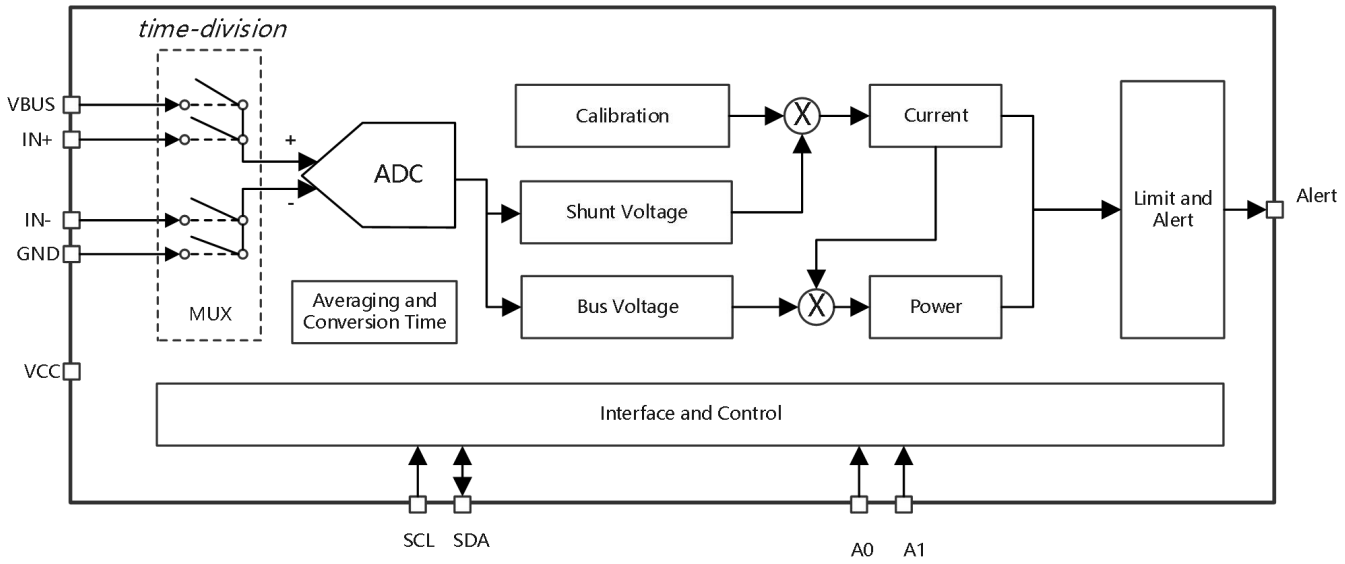


Figure 1-2 Function Block Diagram

2 Ordering Information

2.1 Ordering Information

Order number	Marking ID	Package	MSL	Description
PJ75230M	A2 YM DNN	MSOP-10P	Level-3	Halogen Free RoHS compliant in T&R, 3000pcs/R
PJ75230QW	A1 YM DNN	QFN3X3-16	Level-3	Halogen Free RoHS compliant in T&R, 3000pcs/R

2.2 Marking Information

Marking	Package	Definition
A2 YM DNN	MSOP-10P	A2: Product code,Y: Year code M: Month code D: Day code, NN: Serial Number
A1 YM DNN	QFN3X3-16	A1: Product code,Y: Year code M: Month code D: Day code, NN: Serial Number

3 Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	6	V
Differential	V_{DIFF}	-40 to 40	V
Common Mode	V_{CM}	-0.3 to 40	V
Bus Voltage	V_{VBUS}	-0.3 to 40	V
SDA Voltage	V_{SDA}	(GND-0.3) to 6	V
SCL Voltage	V_{SCL}	(GND-0.3) to (V_{CC} + 0.3)	V
Input current into any pin	I_{IN}	5	mA
Open-drain digital output current	I_{OUT}	10	mA
Junction temperature	T_{JMAX}	150	°C
Storage temperature range	Tstg	-65 to 150	°C
ESD HBM	ESD_{HBM}	±3000	V
ESD CDM	ESD_{CDM}	±1000	V

4 Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Common-mode input voltage	V_{CM}	12	V
Operating supply voltage	V_{CC}	3.3	V
Operating free-air temperature	T_A	-40 to 125	°C

5 Electrical Characteristics

T_A = 25°C, V_{CC} = 3.3 V, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV and V_{VBUS} = 12 V, unless otherwise noted

Parameter	Symbol	Test Conditions	MIN	TYP	MAX	Unit
Shunt voltage input range			-81.9175		81.92	mV
Bus voltage input range			0		36	V
Common-mode rejection	CMRR	0V ≤ V_{IN+} ≤ 36V	126	140		dB
Shunt offset voltage,RTI	V_{OS}			±9.8	±25	μV
Shunt offset voltage,RTI vs temperature		–40°C ≤T_A ≤ 125°C		0.05	0.1	μV/°C
Shunt offset voltage,RTI vs Power supply	PSRR	2.7 V ≤ VS ≤ 5.5 V		3		μV/V
Bus offset voltage,RTI	V_{OS}			±2.3	±15	mV
Bus offset voltage,RTI vs temperature		–40°C ≤T_A ≤ 125°C		10	40	μV/°C
Bus offset voltage,RTI vs Power supply	PSRR			0.4		mV/V
Input bias current(I_{IN+}, I_{IN-} pins)	I_B			8		μA
VBUS input impedance				870		kΩ
Input leakage		(IN+ pin) + (IN– pin), Power-down mode		0.1	0.5	μA
ADC native resolution				16		Bits
1 LSB step size		Shunt voltage		2.5		μV
		Bus voltage		1.25		mV
Shunt voltage gain error				±0.02%	±0.3%	
Shunt voltage gain error vs temperature		–40°C ≤T_A ≤ 125°C		10	50	ppm/°C
Bus voltage gain error				±0.02%	±0.3%	
Bus voltage gain error vs temperature		–40°C ≤T_A ≤ 125°C		18	50	ppm/°C
Differential nonlinearity	DNL			±0.1		LSB
ADC conversion time	t_{CT}	CT bit = 000		140	154	μs
		CT bit = 001		204	224	
		CT bit = 010		332	365	
		CT bit = 011		588	646	
		CT bit = 100		1100	1210	
		CT bit = 101		2116	2328	
		CT bit = 110		4156	4572	
		CT bit = 111		8244	9068	
SMBus timeout				28	35	ms
Input capacitance	C_{Input}			3		pF

Leakage input current		$0\ V \le V_{SCL} \le V_{CC}$, $0\ V \le V_{SDA} \le V_{CC}$, $0\ V \le V_{Alert} \le V_{CC}$, $0\ V \le V_{A0} \le V_{CC}$, $0\ V \le V_{A1} \le V_{CC}$		0.1	1	µA
High-level input voltage	V_{IH}		0.7 * VCC		6	V
Low-level input voltage	V_{IL}		-0.5		0.3 * VCC	V
Low-level output voltage, SDA, Alert	V_{OL}	I_{OL} = 3mA	0		0.4	V
Hysteresis				300		mV
Operating supply range			2.7		5.5	V
Quiescent current	I_Q			330	420	µA
Quiescent current, power-down(shutdown) mode				0.5	2	µA
Power-on reset threshold	V_{POR}			2		V

6 Timing Requirements

T_A = 25°C, V_{CC} = 3.3 V, unless otherwise noted.

Parameter		FAST MODE		HIGH-SPEED MODE		Unit
		MIN	MAX	MIN	MAX	
SCL operating frequency	f_{SCL}	0.001	0.4	0.001	2.94	MHz
Bus free time between stop and start conditions	t_{BUF}	600		160		ns
Hold time after repeated STAT condition. After this period, the first clock is generated.	$t_{HD:STA}$	100		100		ns
Repeated start condition setup time	$t_{SU:STA}$	100		100		ns
STOP condition setup time	$t_{SU:STO}$	100		100		ns
Data hold time	$t_{HD:DAT}$	10	900	10	100	ns
Data setup time	$t_{SU:DAT}$	100		20		ns
SCL clock low period	t_{LOW}	1300		200		ns
SCL clock high period	t_{HIGH}	600		60		ns
Data fall time	t_F		300		80	ns
Clock fall time	t_F		300		40	ns
Clock rise time	t_R		300		40	ns
Clock/data rise time for SCL ≤ 100KHz	t_R		1000			ns

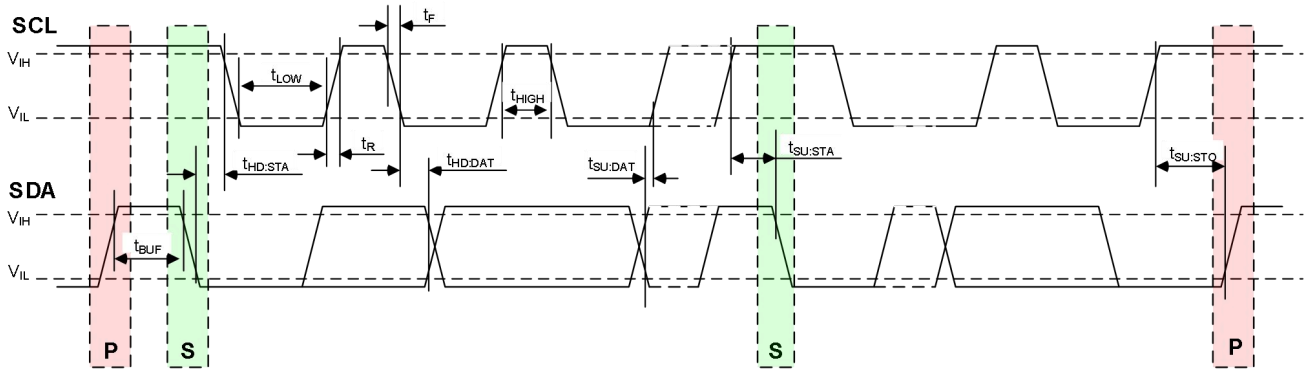


Figure 6-1 I²C Timing Diagram

7 Typical Characteristics

T_A = 25°C, V_{CC} = 3.3 V, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV and V_{VBUS} = 12 V, unless otherwise noted .

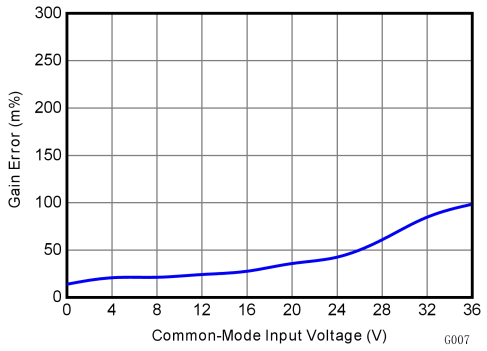


Figure 7-1 Shunt Input Gain Error vs Common-Mode Voltage

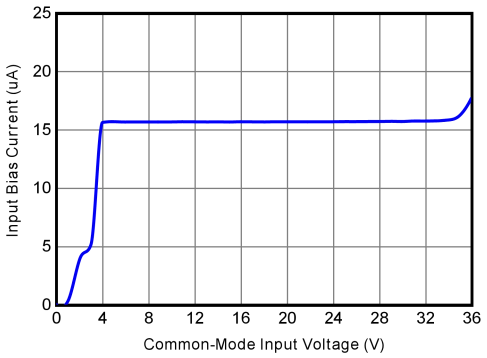


Figure 7-2 Input Bias Current vs Common-Mode Voltage

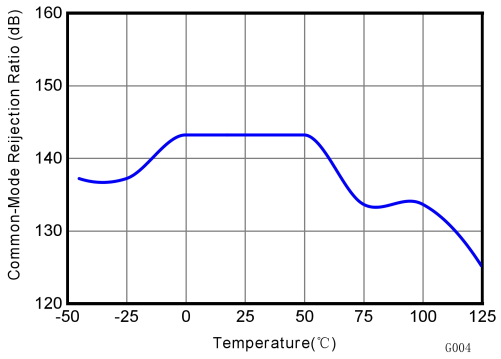


Figure 7-3 Shunt Input CMRR vs Temperature

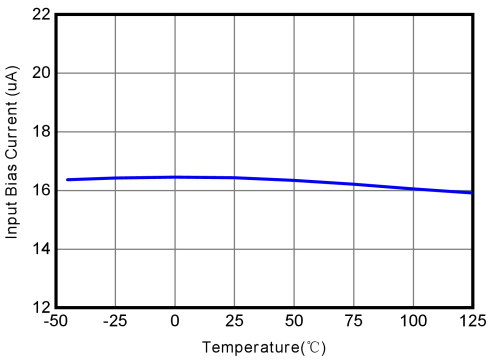


Figure 7-4 Input Bias Current vs Temperature

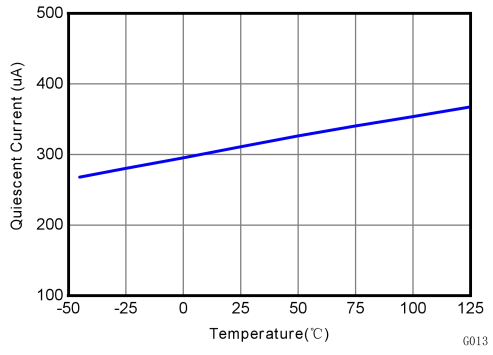


Figure 7-5 Active IQ vs Temperature

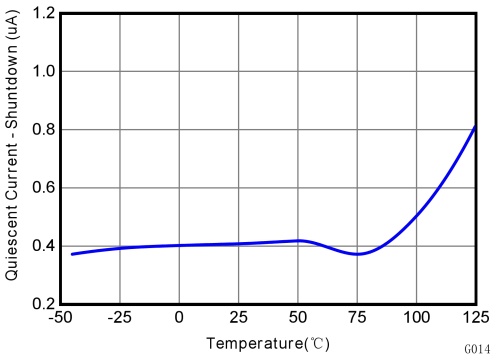


Figure 7-6 Shutdown IQ vs Temperature

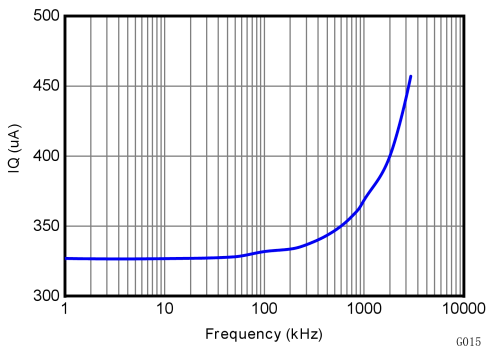


Figure 7-8 Active IQ vs I²C Clock Frequency

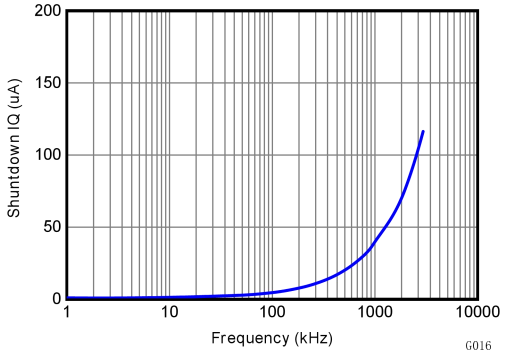


Figure 7-9 Shutdown IQ vs I²C Clock Frequency

8 Detailed Description

8.1 Operating Mode

The device has two operating modes, continuous and trigger. When the device is in the normal operating mode (that is, MODE bits of the Configuration Register (00h) are set to '111'), it continuously converts a shunt voltage reading followed by a bus voltage reading. After the shunt voltage reading, the current value is calculated. This current value is then used to calculate the power result. These values are subsequently stored in an accumulator, and the measurement/calculation sequence repeats until the number of averages set in the Configuration Register (00h) is reached. Following every sequence, the present set of values measured and calculated are appended to previously collected values. After all of the averaging has been completed, the final values for shunt voltage, bus voltage, current, and power are updated in the corresponding registers that can then be read. These values remain in the data output registers until they are replaced by the next fully completed conversion results. Reading the data output registers does not affect a conversion in progress. All current and power calculations are performed in the background and do not contribute to conversion time.

The mode control in the Conversion Register (00h) also permits selecting modes to convert only the shunt voltage or the bus voltage in order to further allow the user to configure the monitoring function to fit the specific application requirements.

In triggered mode, writing any of the triggered convert modes into the Configuration Register (00h) (that is, MODE bits of the Configuration Register (00h) are set to ‘001’, ‘010’, or ‘011’) triggers a single-shot conversion. This action produces a single set of measurements; thus, to trigger another single-shot conversion, the Configuration Register (00h) must be written to a second time, even if the mode does not change.

In addition to the two operating modes (continuous and triggered), the device also has a power-down mode that reduces the quiescent current and turns off current into the device inputs, reducing the impact of supply drain when the device is not being used. Full recovery from power-down mode requires 40μs. The registers of the device can be written to and read from while the device is in power-down mode. The device remains in power down mode until one of the active modes settings are written into the Configuration Register (00h).

8.2 Power Calculation

The Current is calculated following a shunt voltage measurement based on the value set in the Calibration Register. If there is no value loaded into the Calibration Register, the current value stored is zero. Power is calculated following the bus voltage measurement based on the previous current calculation and bus voltage measurement. If there is no value loaded in the Calibration Register, the power value stored is also zero. These current and power values are considered intermediate results (unless the averaging is set to 1) and are stored in an internal accumulation register, not the corresponding output registers. Following every measured sample, the newly-calculated values for current and power are appended to this accumulation register until all of the samples have been measured and averaged based on the number of averages set in the Configuration Register (00h).

8.3 Alert Pin

The PJ75230 has a single Alert Limit Register (07h), that allows the Alert pin to be programmed to respond to a single user-defined event or to a Conversion Ready notification if desired. The Mask/Enable Register allows the user to select from one of the five available functions to monitor and/or set the Conversion Ready bit to control the response of the Alert pin. Based on the function being monitored, the user would then enter a value into the Alert Limit Register to set the corresponding threshold value that asserts the Alert pin.

The Alert pin allows for one of several available alert functions to be monitored to determine if a user-defined threshold has been exceeded. The five alert functions that can be monitored are:

- **Shunt Voltage Over-Limit (SOL)**
- **Shunt Voltage Under-Limit (SUL)**
- **Bus Voltage Over-Limit (BOL)**
- **Bus Voltage Under-Limit (BUL)**
- **Power Over-Limit (POL)**

Only one of these alert functions can be enabled and monitored at a time. If multiple alert functions are enabled, the selected function in the highest significant bit position takes priority and responds to the Alert Limit Register value. For example, if the Shunt Voltage Over-Limit function and the Shunt Voltage Under-Limit function are both selected, the Alert pin asserts when the Shunt Voltage Register exceeds the value in the Alert Limit Register.

Conversion Ready can be monitored at the Alert pin along with one of the alert functions. By reading the Conversion Ready Flag (CVRF, bit 3), and the Alert Function Flag (AFF, bit 4) in the Mask/Enable Register, the source of the alert can be determined.

In addition to the AFF being asserted, the Alert pin is asserted based on the Alert Polarity Bit (APOL, bit 1 of the Mask/Enable Register). If the Alert Latch is enabled, the AFF and Alert pin remain asserted until either the Configuration Register (00h) is written to or the Mask/Enable Register is read.

8.4 Averaging and Conversion Time Considerations

The PJ75230 device offers programmable conversion times (t_{CT}) for both shunt voltage and bus voltage measurements. The conversion times for these measurements can be selected from as fast 140μs to as long as 8.224ms.The conversion time settings, along with the programmable averaging mode, allow the device to be configured to optimize the available timing requirements in a given application. The device could also be configured with a different conversion time setting for the shunt and bus voltage measurements.

There are trade-offs associated with the settings for conversion time and the averaging mode used. The averaging feature can significantly improve the measurement accuracy by effectively filtering the signal.

8.5 Filtering and input Considerations

The internal ADC is based on a delta-sigma (ΔΣ) front-end with a 500 kHz (±30%) typical sampling rate. This architecture has good inherent noise rejection; however, transients that occur at or very close to the sampling rate harmonics can cause problems. Because these signals are at 1MHz and higher, they can be manager by incorporating filtering at the input of the device. The high frequency enables the use if low-value sense resistors on the filter with negligible effects on measurement accuracy. In general, filtering the device input is only necessary if there are transients at exact harmonics of the 500KHz(±30%) sampling rate(greater than 1 MHz). Filter using the lowest possible series resistance (typically 10 Ω or less) and a ceramic capacitor. Recommended values for this capacitor are between 0.1 μF and 1 μF.

Overload conditions are another consideration for the device inputs. The device inputs are specified to tolerate 40 V across the inputs. A large differential scenario might be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long the power supply or energy storage capacitors support it). Removing a short to ground can result in inductive kickbacks that could exceed the 40-V differential and common-mode rating of the device. Inductive kickback voltages are best controlled by Zener-type transient-absorbing devices (commonly called transzorbs) combined with sufficient energy storage capacitance.

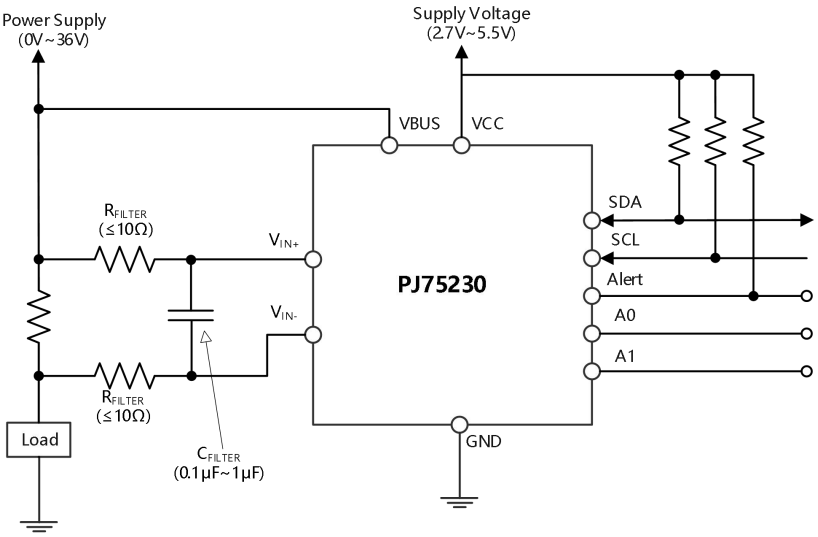


Figure 8-1 Input Filter Circuit

8.6 Programming

An important aspect of the PJ75230 device is that it does not necessarily measure current or power. The device measures both different voltage applied between the IN+ and IN- input pins and voltage applied to V_{BUS} pin. In order for the device to report both current and power values, the user must program the resolution of the Current Register(04h) and the value of the shunt resistor present in the application to develop the differential voltage applied between the input pins. The Power Register (03h) is internally set to be 25 times the programmed Current_LSB. Both the Current_LSB and shunt resistor value are used in the calculation of the Calibration Register value the device uses to calculate the corresponding current and power values based on the measured shunt and bus voltages.

The Calibration Register is calculation based on Equation (1). This equation includes the term Current_LSB, which is the programmed value for the LSB for the Current Register (04h). The user uses this value to convert the value in the Current Register (04h) to the actual current in amperes. The highest resolution for the Current Register (04h) can be obtained by using the smallest allowable Current_LSB based on the maximum expected current as shown in Equation (2). While this value yields the highest resolution, it is common to select a value for the Current_LSB to the nearest round number above this value to simplify the conversion of the Current Register (04h) and Power Register (03h) to amperes and watts respectively. The RSHUNT term is the value of the external shunt used to develop the differential voltage across the input pins.

$$\mathrm{CAL} = \frac{0.00512}{\mathrm{Current\_LSB} \cdot \mathrm{R_{SHUNT}}} \quad (1)$$

Where 0.00512 is an internal fixed value used to ensure scaling is maintained properly

$$\mathrm{Current\_LSB} = \frac{\mathrm{Maximum\ Expected\ Current}}{2^{15}} \quad (2)$$

After programming the Calibration Register, the Current Register (04h) and Power Register (03h) update accordingly based on the corresponding shunt voltage and bus voltage measurements. Until the Calibration Register is programmed, the Current Register (04h) and Power Register (03h) remain at zero.

8.6.1 Programming and Calibration Register

Take application for example with nominal 10-A load that creates a differential voltage of 20 mV across a 2-mΩ shunt resistor. The bus voltage for the PJ75230 is measured at the external V_{BUS} input pin, which in this example is connected to the IN– pin to measure the voltage level delivered to the load. For this example, the V_{BUS} pin measures less than 12 V because the voltage at the IN– pin is 11.98 V as a result of the voltage drop across the shunt resistor.

For this example, assuming a maximum expected current of 15 A, the Current_LSB is calculated to be 457.7 μA/bit using Equation (2). Using a Value for current of 500 μA/bit or 1mA/bit would significantly simplify the conversion from the Current Register(04h) and Power Register(03h) to amperes and watts. For this example, a value of 1mA/bit was chosen for the Current_LSB. Using this value for the Current_LSB does trade a small amount of resolution for having a simpler conversion process on the user side. Using Equation (1) in this example with a Current_LSB value of 1 mA/bit and a shunt resistor of 2 mΩ results in a Calibration Register value of 2560, or A00h.

The Current Register (04h) is then calculated by multiplying the decimal value of the Shunt Voltage Register (01h) contents by the decimal value of the Calibration Register and then dividing by 2048, as shown in Equation (3). For this example, the Shunt Voltage Register contains a value of 8,000 (representing 20 mV), which is multiplied by the Calibration Register value of 2560 and then divided by 2048 to yield a decimal value for the Current Register (04h) of 10000, or 2710h. Multiplying this value by 1 mA/bit results in the original 10-A level stated in the example.

$$\text{Current} = \frac{\text{ShuntVoltage} \cdot \text{CalibrationRegister}}{2048} \tag{3}$$

The LSB of the Bus Voltage Register(02h) is fixed 1.25 mV/bit, which means that the 11.98 V present at the V_{BUS} pin results in a register value of 2570h, or a decimal equivalent of 9584. Note that the MSB of the Bus Voltage Register(02h) is always zero because the V_{BUS} pin is only able to measure positive voltages.

The Power Register(03h) is then be calculated by multiplying the decimal value of the Current Register, 1000, by the decimal value of the Bus Voltage Register(02h), 9854, and the dividing by 20,000, as defined in Multiplying this result by power LSB(25 times the[1 x 10-3 Current_LSB]) result in a power calculation of (4792 x 25 mW/bit), or 119.82 W. The power LSB has a fixed ratio to the Current_LSB of 25. For this example, a programmed 1 mA/bit Current_LSB results in a power LSB of 25 mW/bit. This ratio is internally programmed to ensure that the scaling of the power calculation is within an acceptable range. A manual calculation for the power being delivered to the load would use a bus voltage of 11.98 V (12 VCM – 20 mV shunt drop) multiplied by the load current of 10 A to give a result of 119.8 W.

$$\text{Power} = \frac{\text{Current} \cdot \text{BusVoltage}}{20000} \tag{4}$$

lists the steps for configuring, measuring, and calculating the values for current and power for this device.

Table 8-1 Calculating Current and Power

STEP	REGISTER NAME	ADDRESS	CONTENTS	DEC	LSB	VALUE
Step1	Configuration register	00h	4127h	-	-	-
Step2	Shunt Register	01h	1F40h	8000	2.5uV	20mV
Step3	Bus Register	02h	2570h	9584	1.25mV	11.98V
Step4	Calibration Register	05h	A00h	2560	-	-
Step5	Current Register	04h	2710	10000	1mA	10A
Step6	Power Register	03h	12B8h	4792	25mW	119.82W

8.6.2 Calibration Register and Scaling

The Calibration Register enables the user to scale the Current Register (04h) and Power Register (03h) to the most useful value for a given application. For example, set the Calibration Register such that the largest possible number is generated in the Current Register (04h) or Power Register (03h) at the expected full-scale point. This approach yields the highest resolution using the previously calculated minimum Current_LSB in the equation for the Calibration Register. The Calibration Register can also be selected to provide values in the Current Register (04h) and Power Register (03h) that either provide direct decimal equivalents of the values being measured, or yield a round LSB value for each corresponding register. After these choices have been made, the Calibration Register also offers possibilities for end user system-level calibration. After determining the exact current by using an external ammeter, the value of the Calibration Register can then be adjusted based on the measured current result of the PJ75230 to cancel the total system error as shown in Equation (5).

$$\text{Corrected\_Full\_Scale\_Cal} = \text{trunc}\left(\frac{\text{Cal} \cdot \text{MeasShuntCurrent}}{\text{PJ75230\_Current}}\right) \quad (5)$$

8.7 Bus Overview

8.7.1 Serial Bus Address

Below lists the pin logic levels for each of the 16 possible addresses. The device samples the state of pins A0 and A1 on every bus communication. Establish the pin states before any activity on the interface occurs.

Table 8-2 Address Pins and Slave Addresses

A1	A0	Slave Address
GND	GND	1000000
GND	VCC	1000001
GND	SDA	1000010
GND	SCL	1000011
VCC	GND	1000100
VCC	VCC	1000101
VCC	SDA	1000110
VCC	SCL	1000111
SDA	GND	1001000
SDA	VCC	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	VCC	1001101
SCL	SDA	1001110
SCL	SCL	1001111

8.7.2 Writing to PJ75230

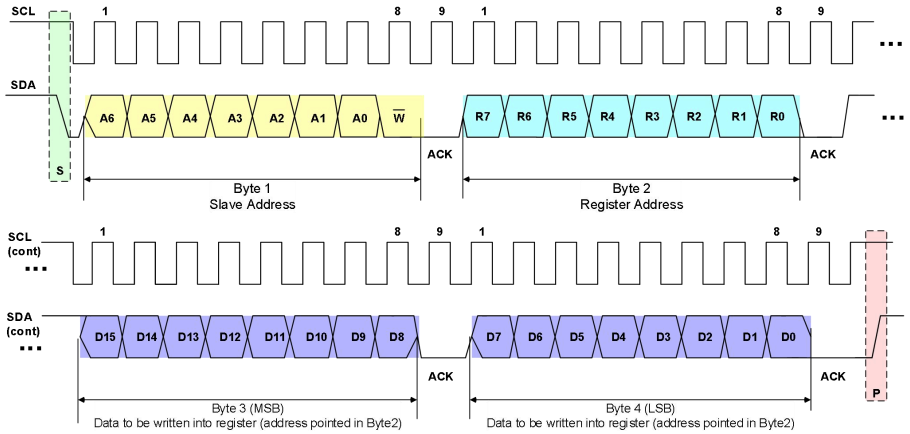


Figure 8-2 Timing Diagram for Write Word Format

8.7.3 Reading from PJ75230

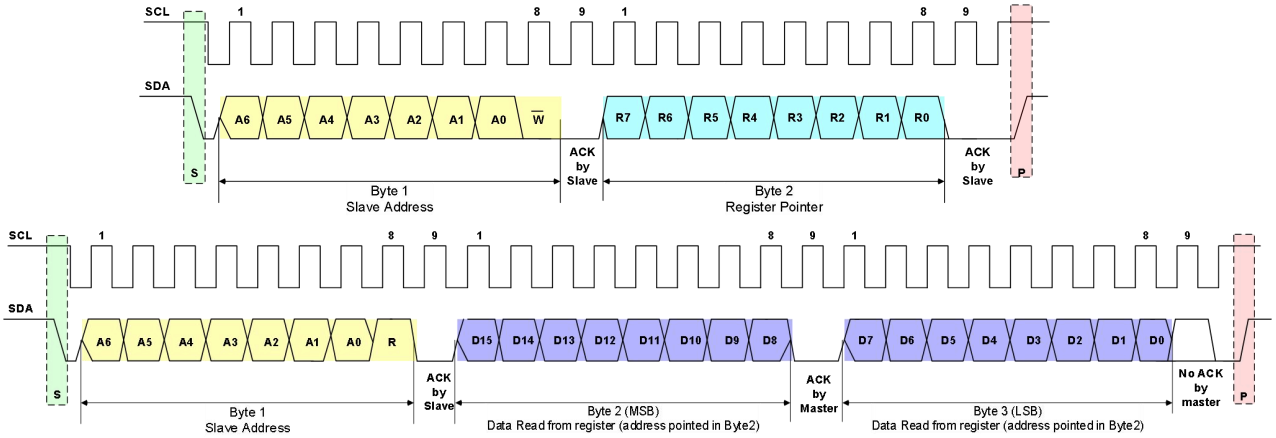


Figure 8-3 Timing Diagram for Read Word Format

8.7.4 ARA (Alert Response Address)

The PJ75230 is designed to respond to the SMBus Alert Response address. The SMBus Alert Response provides a quick fault identification for simple slave devices. When an Alert occurs, the master can broadcast the Alert Response slave address (0001 100) with the Read/Write bit set high. Following this Alert Response, and slave device that generates an alert identifies itself by acknowledging the Alert Response and sending its address on the bus.

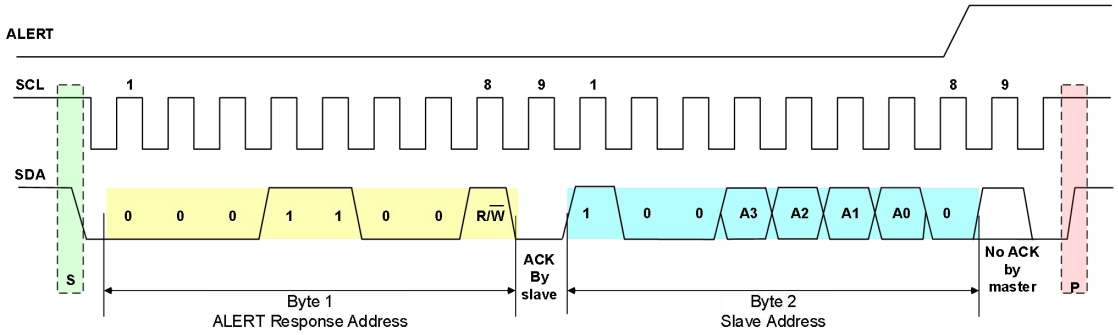


Figure 8-4 Timing Diagram for SMBus ALERT

8.7.5 High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pullup resistors. The master generates a start condition followed by a valid serial byte containing high-speed(HS) master code 00001XXX. This transmission is made in fast (400KHz) or standard (100KHz) (F/S) mode at no more than 400 KHz. The device does not acknowledge the HS master code, but does recognize it and switches its internal filters to support 2.94MHz operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speed up to 2.94MHz are allowed. Instead of using a stop condition, use repeated start conditions to secure the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the device to support the F/S mode.

9 Register Maps

Table 9-1 Register Set Summary

Address	Register Name	Description	Default		Type
			Binary	Hex	
00h	Configuration Register	All-register reset, shunt voltage and bus voltage ADC conversion times and averaging, operating mode.	0100000100100111	4127	R/W
01h	Shunt Voltage Register	Shunt voltage measurement data.	0000000000000000	0000	R
02h	Bus Voltage Register	Bus voltage measurement data.	0000000000000000	0000	R
03h	Power Register	Contains the value of the calculated power being delivered to the load.	0000000000000000	0000	R
04h	Current Register	Contains the value of the calculated current flowing through the shunt resistor.	0000000000000000	0000	R
05h	Calibration Register	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	0000000000000000	0000	R/W
06h	Mask/Enable Register	Alert configuration and Conversion Ready flag.	0000000000000000	0000	R/W
07h	Alert Limit Register	Contains the limit value to compare to the selected Alert function.	0000000000000000	0000	R/W
FFh	Die ID Register	Contains unique die identification number.	0010011100100110	2726	R

9.1 Configuration Register (00h) (Read/Write)

The Configuration Register settings setting control the operating modes for the device. This register controls the conversion time settings for both the shunt and bus voltage measurement as well as the averaging mode used. The operating mode that controls what signals are selected to be measured is also programmed in the Configuration Register.

The Configuration Register can be read from at any time without impacting or affecting the device settings or a conversion in progress. Writing to the Configuration Register halts any conversion in progress until the write sequence is completed resulting in a new conversion starting based on the new contents of the configuration Register (00h). This halt prevents any uncertainty in the conditions used for the next completed conversion.

Table 9-2 Configuration Register (00h) (Read/Write) Descriptions

BIT NO.	D15	D14	D13	D12	D11	D10	D9	D8
BIT NAME	RST	—	—	—	AVG2	AVG1	AVG0	VBUSCT2
VALUE	0	1	0	0	0	0	0	1
BIT NO.	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	VBUSCT1	VBUSCT0	VSHCT2	VSHCT1	VSHCT0	MODE3	MODE2	MODE1
VALUE	0	0	1	0	0	1	1	1

BIT	Name	Attribution	Default	Definition
15	RST	W	1'b0	System Reset: 1: Resets all registers to default values; this bit self-clears.
11:9	AVG[2:0]	R/W	3'b000	Number of Averages setting: 3b'000: 1 (default) 3b'001: 4 3b'010: 16 3b'011: 64 3b'100: 128 3b'101: 256 3b'110: 512 3b'111: 1024
8:6	VBUSCT[2:0]	R/W	3'b100	Bus Voltage Conversion Time setting: 3b'000: 140 μs 3b'001: 204 μs 3b'010: 332 μs 3b'011: 588 μs 3b'100: 1.1 ms (default) 3b'101: 2.116 ms 3b'110: 4.156 ms 3b'111: 8.224 ms
5:3	VSHCT[2:0]	R/W	3'b100	Shunt Voltage Conversion Time setting: 3b'000: 140 μs 3b'001: 204 μs 3b'010: 332 μs 3b'011: 588 μs 3b'100: 1.1 ms (default) 3b'101: 2.116 ms 3b'110: 4.156 ms 3b'111: 8.224 ms
2:0	MODE[2:0]	R/W	3'b111	Operating Mode: 3b'000: Power-Down (or Shunt-Down) 3b'001: Shunt Voltage, Triggered 3b'010: Bus Voltage, Triggered 3b'011: Shunt and Bus, Triggered 3b'100: Power-Down (or Shunt-Down) 3b'101: Shunt Voltage, Continue 3b'110: Bus Voltage, Continue 3b'111: Shunt and Bus Voltage, Continue (default)

9.2 Shunt Voltage Register (01h) (Read-Only)

The Shunt Voltage Register stores the current shunt voltage reading, VSHUNT. Negative numbers are repeated in two's complement format. Generate the two's complement of negative number by complementing the absolute value binary number and adding 1. An MSB = '1' denotes a negative number.

Example: For a value of VSHUNT = -80 mV:

1. Take the absolute value: 80 mV

2. Translate this number to a whole decimal number (80 mV ÷ 2.5 μV) = 32000

3. Convert this number to binary = 0111 1101 0000 0000

4. Complement the binary result = 1000 0010 1111 1111

5. Add '1' to the complement to create the two's complement result = 1000 0011 0000 0000 = 8300h

If averaging is enabled, this register displays the averaged value.

Full-scale range = 81.92 mV (decimal = 7FFF); LSB: 2.5 μV.

Table 9-3 Shunt Voltage Register (01h) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8
BIT NAME	SIGN	SD14	SD13	SD12	SD11	SD10	SD9	SD8
VALUE	0	0	0	0	0	0	0	0
BIT #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
VALUE	0	0	0	0	0	0	0	0

BIT	Name	Attribution	Default	Definition
15	SIGN	R	1'b0	Sign Bit: 1'b0: Denote a positive number 1'b1: Denote a negative number.
14:0	SD[14:0]	R	15'b0	Shunt Voltage Data. Negative numbers are repeated in two's complement format while The Bit15 = 1'b1.

9.3 Bus Voltage Register (02h) (Read-Only)

The Bus Voltage Register stores the most recent bus voltage reading, V_{BUS}.

If averaging is enabled, this register displays the averaged value.

Full-scale range = 40.96 V (decimal = 7FFF); LSB = 1.25 mV.

Table 9-4 Bus Voltage Register (02h) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8
BIT NAME	-	BD14	BD13	BD12	BD11	BD10	BD9	BD8
VALUE	0	0	0	0	0	0	0	0
BIT #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0
VALUE	0	0	0	0	0	0	0	0

9.4 Power Register (03h) (Read-Only)

If averaging is enabled, this register displays the averaged value.

The Power Register LSB is internally programmed to equal 25 times the programmed value of the Current_LSB.

The Power Register records power in Watts by multiplying the decimal values of the Current Register with the decimal value of the Bus Voltage Register according to Equation (4).

Table 9-5 Power Register (03h) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8
BIT NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8
VALUE	0	0	0	0	0	0	0	0
BIT #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
VALUE	0	0	0	0	0	0	0	0

9.5 Current Register (04h) (Read-Only)

If averaging is enabled, this register displays the averaged value.

The value of the Current Register is calculated by multiplying the decimal value in the Shunt Voltage Register with the decimal value of the Calibration Register, according to Equation (3).

Table 9-6 Current Register (04h) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8
BIT NAME	CSIGN	FS14	FS13	FS12	FS11	FS10	FS9	FS8
VALUE	0	0	0	0	0	0	0	0
BIT #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
VALUE	0	0	0	0	0	0	0	0

9.6 Calibration Register (05h) (Read/Write)

This register provides the device with the value of the shunt resistor that was present to create the measured differential voltage. It also sets the resolution of the Current Register. Programming this register sets the Current_LSB and the Power_LSB. This register is also suitable for use in overall system calibration.

Table 9-7 Calibration Register (05h) (Read/Write) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8
BIT NAME	—	FS14	FS13	FS12	FS11	FS10	FS9	FS8
VALUE	0	0	0	0	0	0	0	0
BIT #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
VALUE	0	0	0	0	0	0	0	0

BIT	Name	Attribution	Default	Definition
15	—	R/W	1'b0	Reserved.
14:0	FS[14:0]	R/W	15'b0	Calibration Register.

9.7 Mask/Enable Register (06h) (Read/Write)

The Mask/Enable Register selects the function that is enabled to control the Alert pin as well as how that pin functions. If multiple functions are enabled, the highest significant bit position Alert Function (D15-D11) takes priority and responds to the Alert Limit Register.

Table 9-8 Mask/Enable Register (06h) (Read/Write) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8
BIT NAME	SOL	SUL	BOL	BUL	POL	CNVR	—	—
VALUE	0	0	0	0	0	0	0	0
BIT #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	—	—	—	AFF	CVRF	OVF	APOL	LEN
VALUE	0	0	0	0	0	0	0	0

BIT	Name	Attribution	Default	Definition
15	SOL	R/W	1’b0	Shunt Voltage Over-Limit : 1'b0: Disable Shunt Voltage Over-Limit assert. 1'b1: Enable Shunt Voltage Over-Limit assert.
14	SUL	R/W	1’b0	Shunt Voltage Under-Limit: 1'b0: Disable Shunt Voltage Under-Limit assert. 1'b1: Enable Shunt Voltage Under-Limit assert.
13	BOL	R/W	1’b0	Bus Voltage Over-Limit : 1'b0: Disable Bus Voltage Over-Limit assert. 1'b1: Enable Bus Voltage Over-Limit assert.
12	BUL	R/W	1’b0	Bus Voltage Under-Limit: 1'b0: Disable Bus Voltage Under-Limit assert. 1'b1: Enable Bus Voltage Under-Limit assert.
11	POL	R/W	1’b0	Power Over-Limit: 1'b0: Disable Power Over-Limit assert. 1'b1: Enable Power Over-Limit assert. T
10	CNVR	R/W	1’b0	Conversion Ready: 1'b0: Disable Conversion Ready assert. 1'b1: Enable Conversion Ready assert.
9:5	—	R/W	5’b0	Reserved.
4	AFF	R	1’b0	Alert Function Flag: 1’b1: Determine the Alert source From Alert Function. While only one Alert Function can be monitored at the Alert pin at a time, the Conversion Ready can also be enabled to assert the Alert pin. Alert Function Flag bit clears under the following conditions: 1) When the Alert Latch Enable bit is set to Latch mode, the Alert Function Flag bit clears only when the Mask/Enable Register is read. 2) When the Alert Latch Enable bit is set to Transparent mode, the Alert Function Flag bit is cleared following the next conversion that does not result in an Alert condition.
3	CVRF	R	1’b0	Conversion Ready Flag: 1’b1: Determine the Alert source From Conversion Ready. The Conversion Ready Flag bit is provided to help coordinate one-shot or triggered conversions. The Conversion Ready Flag bit is set after all conversions, averaging, and multiplications are complete. Conversion Ready Flag bit clears under the following conditions: 3) Writing to the Configuration Register (except for Power-Down

				selection) 4) Reading the Mask/Enable Register
2	OVF	R	1'b0	Math Overflow Flag: 1'b1: The arithmetic operation resulted in an overflow error. It indicates that current and power data may be invalid.
1	APOL	R/W	1'b0	Alert Polarity bit: Sets the Alert pin polarity 1'b0: Inverted (active-high open collector) 1'b1: Normal (active-low open collector) (default)
0	LEN	R/W	1'b0	Alert Latch Enable: Configures the latching feature of the Alert pin and Alert Flag bits. 1'b0 = Transparent (default). The Alert pin and Flag bit resets to the idle states when the fault has been cleared. 1'b1 = Latch enabled. The Alert pin and Alert Flag bit remains active following a fault until the Mask/Enable Register has been read.

9.8 Alert Limit Register (07h) (Read/Write)

The Alert Limit Register contains the value used to compare to the register selected in the Mask/Enable Register to determine if a limit has been exceeded.

Table 9-9 Alert Limit Register (07h) (Read/Write) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8
BIT NAME	AUL15	AUL14	AUL13	AUL12	AUL11	AUL10	AUL9	AUL8
VALUE	0	0	0	0	0	0	0	0
BIT #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	AUL7	AUL6	AUL5	AUL4	AUL3	AUL2	AUL1	AUL0
VALUE	0	0	0	0	0	0	0	0

9.9 Die ID Register (FFh) (Read-Only)

The Die ID Register stores a unique identification number and the revision ID for the die.

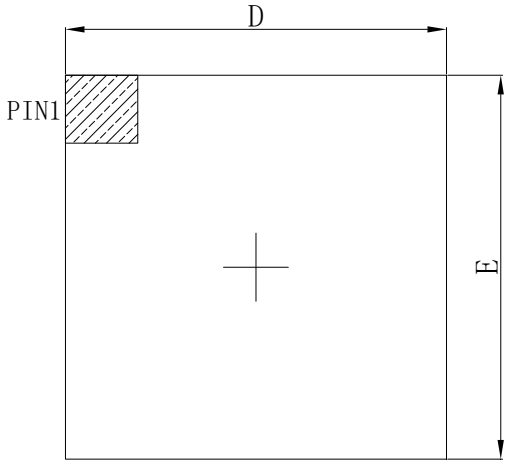
Table 9-10 Die ID Register (FFh) (Read-Only) Description

BIT #	D15	D14	D13	D12	D11	D10	D9	D8
BIT NAME	DID11	DID10	DID9	DID8	DID7	DID6	DID5	DID4
VALUE	0	0	1	0	0	1	1	1
BIT #	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
BIT NAME	DID3	DID2	DID1	DID0	RID3	RID2	RID1	RID0
VALUE	0	0	1	0	0	1	1	0

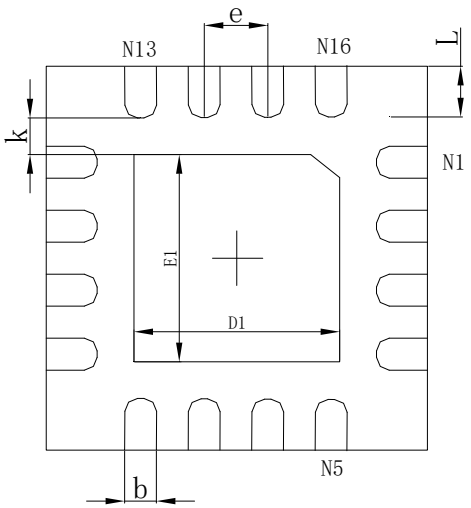
10 Package Outline Dimension and Recommended Land Pattern Layout

10.1 Package Outline Dimension (QFN3X3-16)

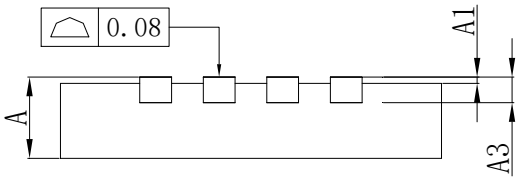
QFN3X3-16 Unit (mm)



Top View



Bottom View



Side View

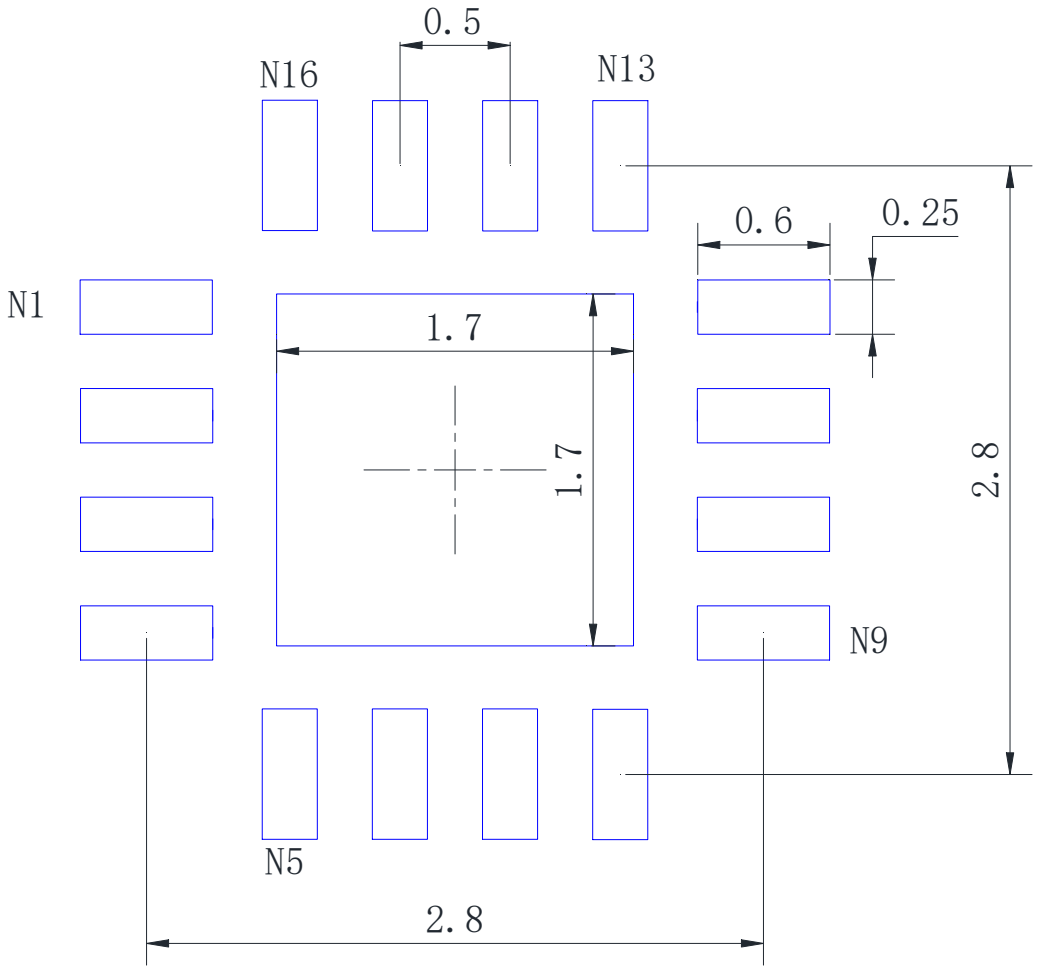
Table 10-1 Package Outline Dimension(QFN3x3-16)

Symbol	Dimensions in Millimeter		Dimensions in Inches	
	Min.	Max	Mn.	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.203REF		0.008REF	
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E1	1.600	1.800	0.063	0.071
k	0200MN.		0.008REF	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP	
L	0.300	0.500	0.012	0.020

Note：Pin1 shape on backside is not limited to bevel, it can be a notch or arch

10.2 Recommend Land Pattern Layout(QFN3X3-16)

QFN3X3-16 **Unit (mm)**



Note:

1. All dimensions are in millimeter
2. Recommend tolerance is within ±0.1mm
3. If the thermal pad is not necessary, designer can leave the land pattern area blank
4. Change without notice

10.3 Package Outline Dimensions (MSOP-10P)

MSOP-10P **Unit (mm)**

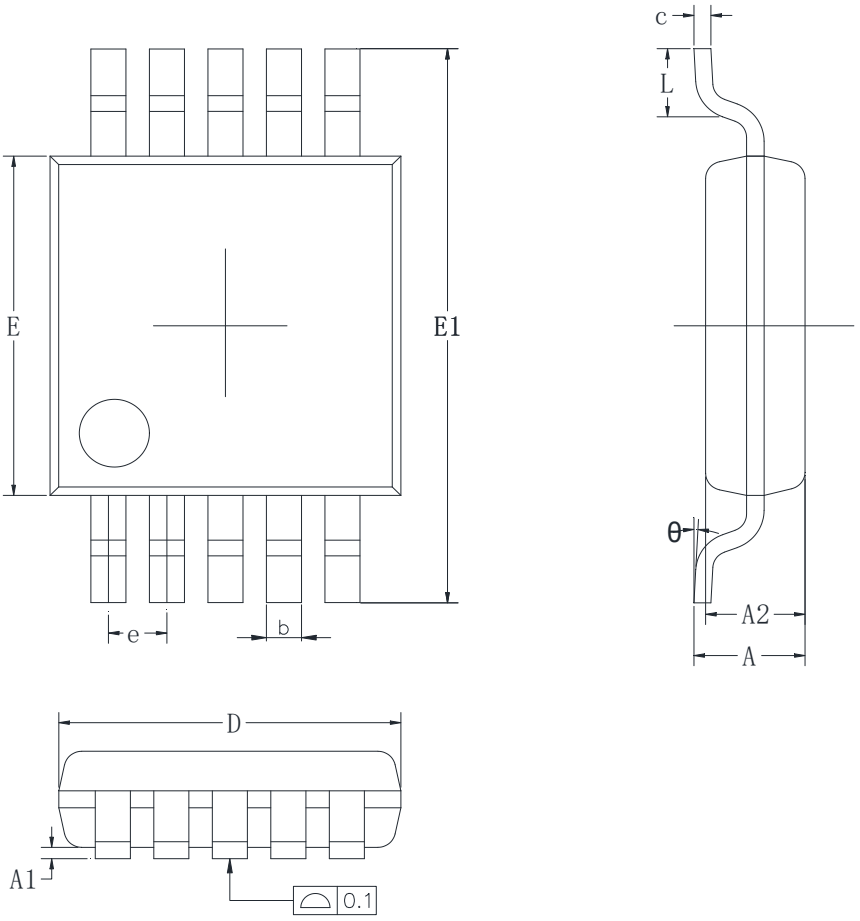
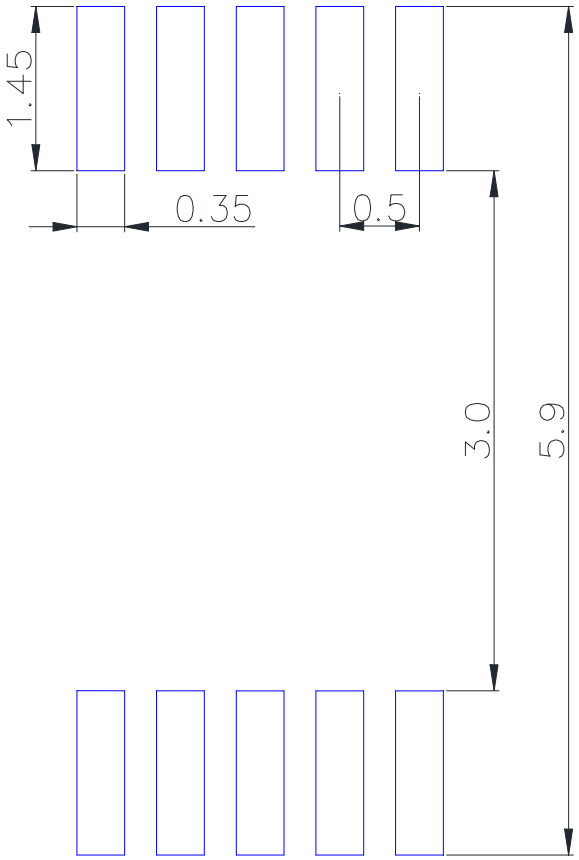


Table 10-2 Package Outline Dimension(MSOP-10P)

Symbol	Dimensions in Millimeter		Dimensions in Inches	
	Min.	Max	Mn.	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
C	0.090	0.250	0.004	0.010
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
e	0.500(BSC)		0.020(BSC)	
L	0.400	0.800	0.016	0.031
θ	0°	8°	0°	8°

10.4 Recommend Land Pattern Layout (MSOP-10P)

MSOP-10P **Unit (mm)**



Note:

1. All dimensions are in millimeter

2. Recommend tolerance is within ±0.1mm

3. Change without notice

11 Packing Information

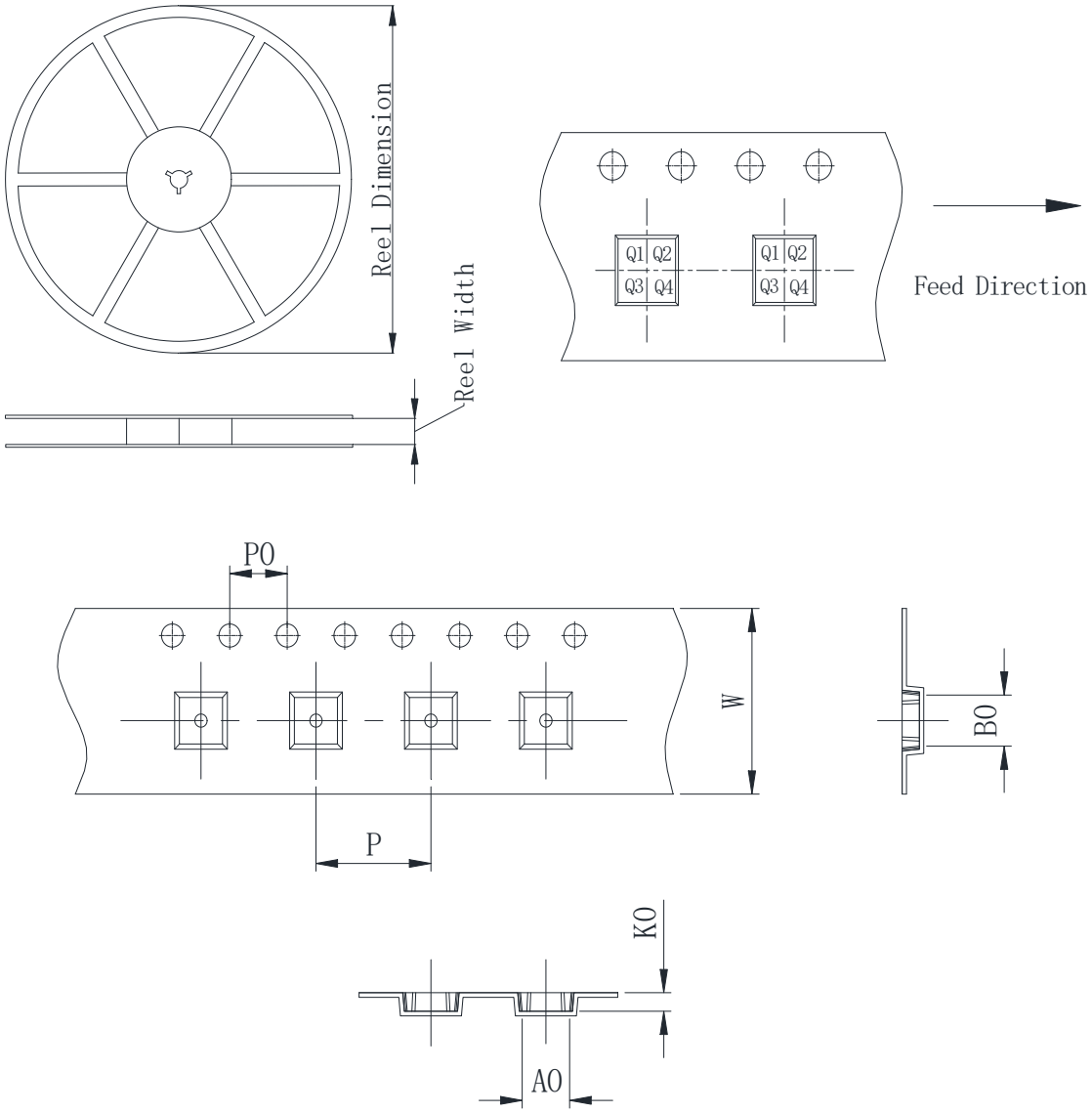


Table 11-1 Package Information

Package type	Reel size	Reel dimension (±3.0mm)	Reel width (±1.0mm)	A0 (±0.1mm)	B0 (±0.1mm)	K0 (±0.1mm)	P (±0.1mm)	P0 (±0.1mm)	W (±0.3mm)	Pin1
QFN3x3-16	13'	330	12.4	3.3/3.35	3.3/3.35	1.1/1.13	8.0	4.0	12.0	Q2
MSOP-10P	13'	330	12.4	5.2/5.4	3.3/3.4	1.5/1.4	8.0	4.0	12.0	Q1

12 Version History

Version	Date	Changes
Rev.1.0	2025-05-28	Initial release
Rev.1.1	2025-08-22	Added: MSL ratings to ordering table (Sect. 2.1). Added: Section 12 "Version History"

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