PM10225A Datasheet

Motor MCU with 64MHz ARM Cortex-M0

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MetaWells Co., Ltd.

www.metawells.com

Contents

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1 Introduction

This document is the datasheet for the PM10225A series of chips. The PM10225A series comprises motor-dedicated MCU chips developed by MetaWells Co., Ltd., and includes the following models:

- **PM10225A (QFN3X3-20 package)**

Users can refer to the PM10225 User Manual for further details on the functionality of this chip series.

2 Product Description

The PM10225A series is a motor-dedicated chip based on the ARM® Cortex®-M0 core, with a maximum operating frequency of 64 MHz. It integrates 32 Kbytes of Flash and 4 Kbytes of SRAM.

The PM10225A includes one 16-bit advanced timer, one 32-bit general-purpose timer, one 16-bit general-purpose timer, and one 24-bit hall-sensor dedicated timer.

The analog circuitry embedded in the PM10225A comprises: one 12-bit ADC (supporting 14 external analog input channels and 6 internal input channels), two programmable operational amplifiers (with PGA1 supporting two-phase current polling amplification), two analog comparators (featuring built-in BEMF neutral-point real-time detection), one power-on/power-down reset circuit (POR/PDR), one programmable voltage detector/brown-out reset circuit (PVD/BOR), one internal temperature sensor, one internal voltage reference (accessible via the on-chip ADC), and an internal analog supply circuit providing 2.4 V/3.6 V outputs.

All pins of the PM10225A, except for power and ground, can be used as GPIOs, peripheral I/Os, or external interrupt inputs.

The PM10225A supports traditional Flash read/write protection.

The PM10225A incorporates multiple communication interfaces: two UARTs, one high-speed SPI, and one I²C.

It also integrates a hardware division and square-root arithmetic unit (DVSQ), enhancing software processing capability and enabling fast response to external events.

The PM10225A supports Sleep and Stop low-power modes, making it suitable for applications requiring low power consumption.

Thanks to its rich set of peripherals, the PM10225A is particularly well-suited for BLDC/PMSM motor control applications, such as trapezoidal and FOC drives, in:

- **Power tools**
- **Industrial fans**
- **Compressors**
- **Electric vehicles**
- **Range hoods**
- **Vacuum cleaners**
- **Pumps**
- **Ceiling fans**
- **Air conditioners**

2.1 Product Features

- **CPU Core**
  - **ARM® Cortex®-M0**
  - **Maximum clock frequency: 64 MHz**
  - **24-bit System Tick timer**
- **Operating Voltage Range**
  - **Single power domain (main supply VDD): 2.2 V to 5.5 V**
- **Operating Temperature Range: –40 °C to +105 °C**
- **Typical Operating Current**
  - **Sleep mode**
    - 1.16 mA @ 5 V @ 40 kHz
    - 2.01 mA @ 5 V @ 8 MHz
    - 2.13 mA @ 5 V @ 64 MHz
  - **Stop mode**

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- Normal Stop: 0.19 mA @ 5 V @ 40 kHz
- Low-Power Stop: 0.04 mA @ 5 V @ 40 kHz

◆ **Memory**

- **32 Kbyte Flash**
  - Zero-wait-state access to Flash when CPU frequency ≤ 24 MHz
  - Flash data security protection with configurable read and write protection
- **4 Kbyte SRAM**

◆ **Clock**

- **Internal high-speed clock (HSI): 8/64 MHz**
- **Internal low-speed clock (LSI): 40 kHz**
- **GPIO external input clock: ≤ 32 MHz**

◆ **Reset**

- **External pin reset (NRST pin)**
- **Option-byte loader reset**
- **Window watchdog reset (WWDG reset)**
- **Independent watchdog reset (IWDG reset)**
- **Power reset (POR/PDR/BOR)**
- **Software reset (SW reset)**

◆ **GPIO Ports**

- **Up to 30 GPIO ports**

◆ **Data Communication Interfaces**

- **2 UARTs**
  - LIN mode supported
- **1 I²C**
  - 1 MHz / 400 kHz / 100 kHz transfer modes
- **1 high-speed SPI**
  - Maximum transfer rate: 18 Mbps

◆ **Timers**

- **1 advanced motor-dedicated 16-bit timer (ATU)**
  - 3 complementary PWM outputs with asymmetrical dead-time insertion
  - Supports 6 independent PWM outputs
  - Brake input from external pin or internal comparator output
  - Two independent trigger signals for synchronous ADC sampling
  - Supports ADC dual-group sampling trigger
- **2 general-purpose timers (UTU1: 32-bit, UTU2: 16-bit)**
  - Supports 2 independent PWM output modes
  - Supports 1 complementary PWM output mode
  - Supports single-trigger of ATU or the other UTU
  - Supports periodic ADC sampling trigger
- **1 24-bit hall timer (HTU)**
  - Supports three hall-signal inputs
  - Hall phase-sequence detection
  - Commutation averaging function (2, 4, or 8 commutations)
  - HTU linked counting with comparators CMPx

◆ **Division and Square-Root Unit (DVSQ)**

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- 32-bit fixed-point division, providing both quotient and remainder
- 32-bit fixed-point high-precision square-root

◆ **On-Chip Analog Circuits**

- **1 12-bit SAR ADC (up to 14 external analog input channels, corresponding to 16 external pins)**
  - 12-bit resolution
  - Maximum conversion rate: 2.285 MSPS
  - Programmable sampling time, independently configurable per channel
  - Left- and right-aligned data output
  - Supports sampling of internal analog circuits (PGA1_OUTA, PGA1_OUTB, PGA2_OUT, VDIV_OUT, internal temperature sensor, internal voltage reference)
  - Supports two sampling groups (customizable channels)
  - Trigger sources: software and multiple hardware triggers (ATU TRG0/TRG1, UTU1/2, CMP, etc.)
  - Analog window comparison function
  - Independent data result registers for each sampling group
  - Oversampling and averaging function
  - VREFP internal supply selection: 2.4 V, 3.6 V, or VDDA as ADC reference voltage
- **Internal voltage reference VREFINT (BGV)**
  - Output connected to a dedicated ADC channel
- **2 voltage comparators**
  - Reference voltage can come from external signal input or internal voltage divider VDIV
  - Comparator output can be used as ATU brake input
  - Supports BEMF internal neutral-point detection
  - Supports PWM blanking signal masking from ATU
- **2 programmable operational amplifiers**
  - Programmable gain (×1, ×4, ×8, ×12, ×20, ×40)
  - Built-in bias voltage on P-input
  - PGA1 supports two-input signal polling amplification
  - Output directly connected to ADC for sampling

◆ **96-Bit Chip Unique ID (UID)**

- **Used as serial number and security key**
- **Activates secure boot process**

◆ **CPU Trace and Debug**

- **SWD debug interface**
- **ARM® CoreSight™ debug components (ROM Table, DWT, BPU)**
- **Custom DBGMCU debug controller (low-power mode simulation control, peripheral clock control for debugging, debug and trace interface allocation)**

◆ **Reliability**

- **CDM 2000 V / HBM 6000 V qualified (LU data to be added)**

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2.2 Device Overview

Table 2-1 PM10225A Series Feature

Feature		PM10225A
GPIO		18
Package		QFN3X3-20
Operating Voltage		2.2V~5.5V
Operating Temperature		-40°C ~ +105°C
Memory	Flash (Kbyte)	32
	SRAM (Kbyte)	4
CPU	Core	Cortex®-M0
	Operating Frequency	64 MHz
Division/Square-Root Unit (DVSQ)		1
Clock	Internal LSI	40 kHz
	Internal HSI	8 MHz /64 MHz
	External Clock Input	0~32MHz
Timers	Advanced Timer (ATU)	1 (16-bit)
	General-Purpose Timer (UTU)	1 (32-bit): UTU1 1 (16-bit): UTU2
	Hall-Dedicated Timer (HTU)	1 (24-bit)
	System Tick Timer	1
	Independent Watchdog (IWDG)	1
	Window Watchdog (WWDG)	1
Communication Peripherals	UART	2
	I2C	1
	SPI	1
ADC	Number of ADCs (External Analog Channels)	1 (10)
	VREFP Internal Supply Voltage	VDDA / 2.4 V VREF / 3.6 V VREF (1) selectable
	Reference Selection	Internal Voltage Reference VREFINT
	ADC Conversion Rate	2.285MSPS(ADC_CLK=32MHz)
	ADC Resolution	12-bit
Voltage Comparator (CMP)		2
Programmable Operational Amplifier (PGA)		2
96 Bit UID		1

(1). When selecting 2.4 V VREF as the VREFP internal supply voltage, VDD must be above 2.9 V. When selecting 3.6 V VREF, VDD must be above 4 V.

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3 Ordering Information

3.1 Ordering Information

Table 3-1 PM10225A Product Ordering Information

Order number	Marking ID	Package	Description
PM10225AQW	10225A YMDNN	QFN3X3-20	Halogen free RoHS compliant in T/R,3,000 pcs/Reel

3.2 Marking Information

Table 3-2 PM10225A Product Marking Information

Marking	Package	Definition
10225A YMDNN	QFN3X3-20	Product code : 10225A Y : Year code M : Month code D : Day code NN: Serial Number

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4 Function Introduction

4.1 Block Diagram

The device incorporates 32Kbyte of internal Flash memory for storing programmes and data.

The ARM® Cortex®-M0 processor is an embedded 32-bit RISC processor delivering outstanding computational performance and advanced interrupt system responsiveness. The Cortex®-M0 core integrated within this product family is fully compatible with all ARM tools and software.

The functional block diagram of the PM10225A is shown below:

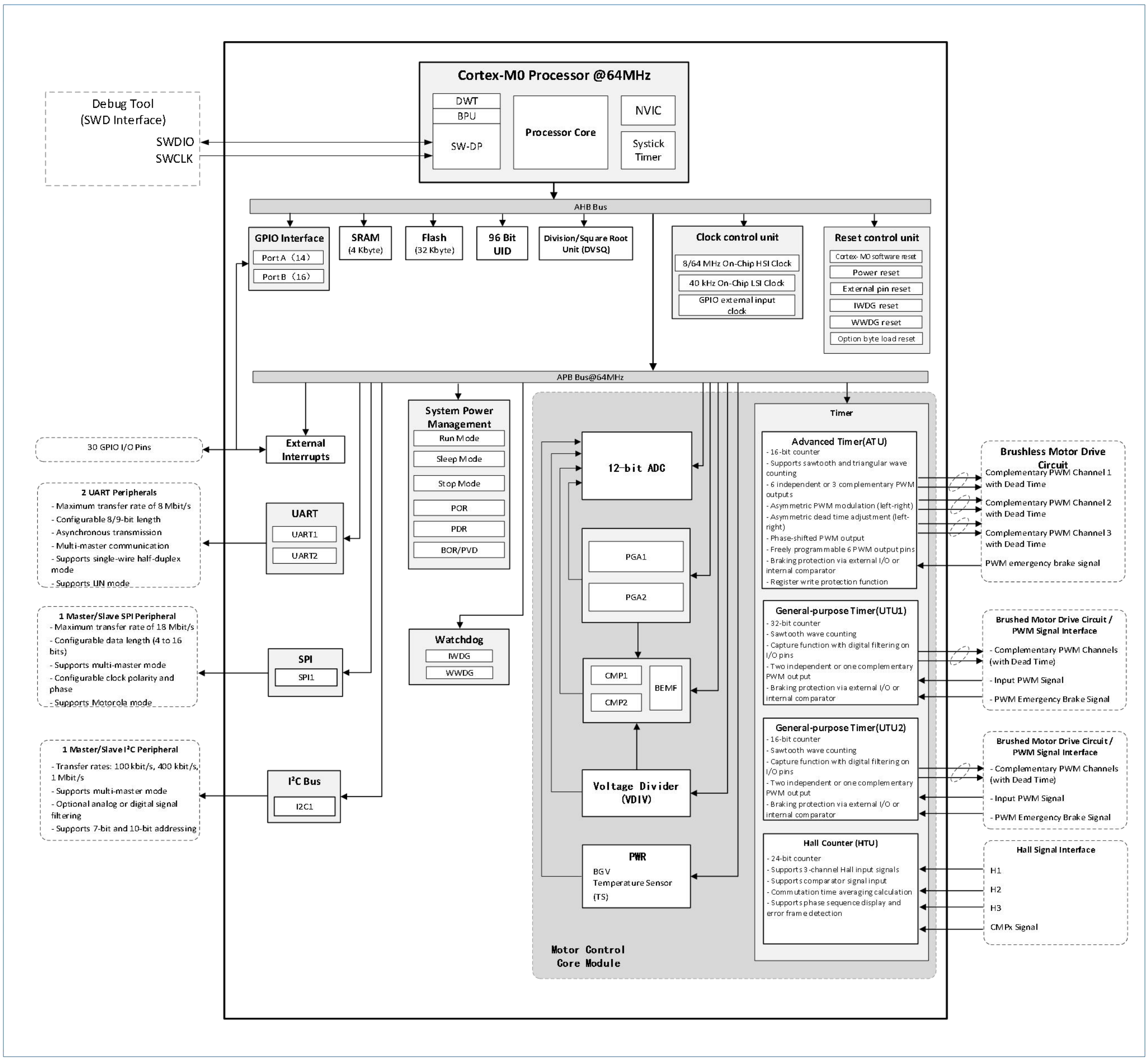

Figure 4-1 PM10225A Block Diagram

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4.2 Memory Mapping Configuration

The memory map of the PM10225A MCU is illustrated in the following figure:

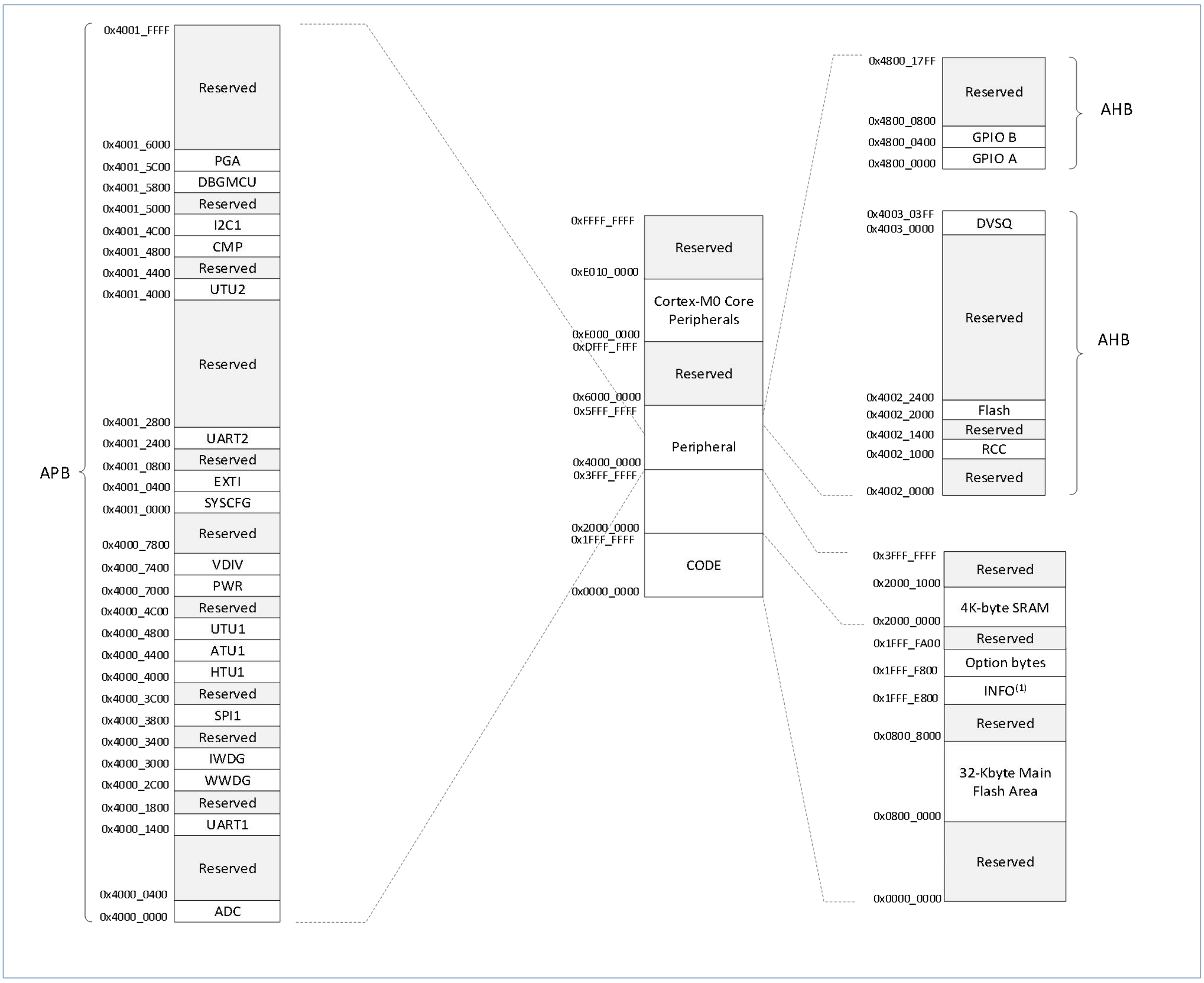

Figure 4-2 PM10225A Memory Map

(1). It is recommended that users employ the INFO (Information) section to store parameters within the application.

4.3 Memory

4.3.1 Flash

- **The Flash consists of the following parts:**
  - **32 Kbyte Main Flash block: for storing programs and data.**
  - **4 Kbyte Information block (INFO): It is recommended that users store application parameters in the INFO area.**
  - **Option bytes**

4.3.2 Embedded SRAM

This series of chips integrates 4 Kbytes of SRAM internally, supporting read/write access by word, half-word, and byte. The CPU can access the SRAM with zero wait states, meeting the requirements of most applications.

4.4 Power Supply Scheme

V_{DD} = 2.2 ~ 5.5 V: External single power supply (no V_{BAT}). The VDD pin supplies power to the chip's digital circuits, I/O pins, and internal voltage regulator. The V_{DD} pin also supplies power to the analog parts such as the ADC, voltage comparators, and operational amplifiers.

Note:

V_{DDA} and V_{SSA} are internally connected to VDD and VSS, respectively.

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4.5 Power Supply Monitors

The chip integrates a power-on reset (POR), power-down reset (PDR), programmable voltage detector (PVD), and brown-out reset (BOR) circuit. The system becomes operational once the supply voltage reaches 2.2 V. When V_{DD}/V_{DDA} falls below the specified limit voltage VPOR/VPDR, the system is held in reset without requiring any external reset circuitry.

During power-up, the brown-out reset (BOR) holds the device in reset until the supply voltage reaches the specified V_{BOR} threshold. When BOR is disabled, the power supply is monitored by POR/PDR. The device also features a programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} supply and compares it with the V_{PVD} threshold. The V_{PVD} threshold can be configured by software. An interrupt is generated when V_{DD} falls below or rises above the V_{PVD} threshold, and the interrupt handler can issue a warning message.

Note:

BOR and PVD cannot be used simultaneously; only one can be active at a time, and they must be enabled by software.

4.6 Low-Power Modes

The device supports Sleep mode and Stop mode.

1. Sleep mode: Only the CPU is stopped. All peripherals remain active and can wake up the CPU when an interrupt/event occurs.
2. Stop mode: While retaining the contents of SRAM and registers, Stop mode achieves the lowest power consumption. In Stop mode, all clocks in the core domain are stopped. The MCU can be woken up from Stop mode by any signal configured as EXTI, which can be one of the 16 external I/Os.

4.7 Reset

4.7.1 System Reset

A system reset resets all registers to their reset state, except for the reset flags in the RCC_CSR register. The source of the reset event can be identified by checking the reset status flags in the RCC_CSR control/status register.

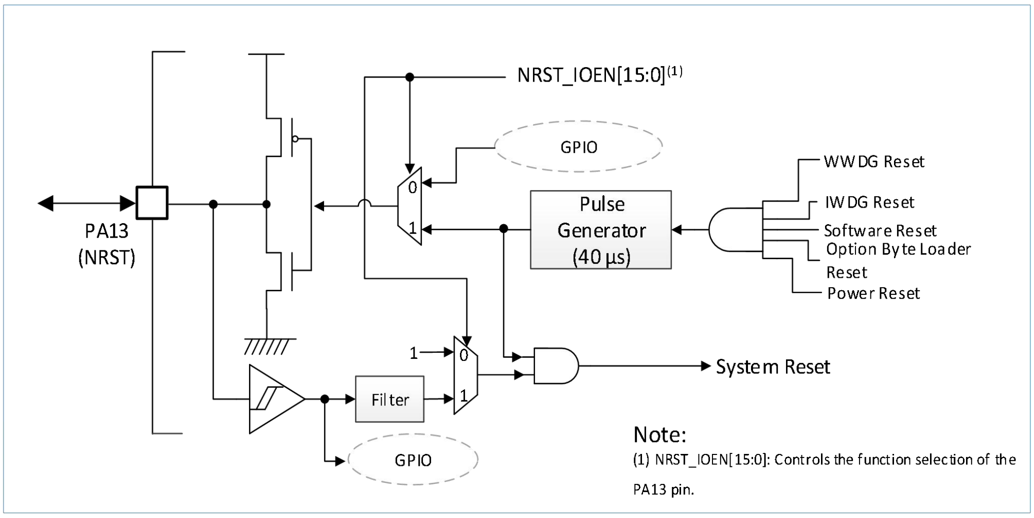

Figure 4-3 Reset Signals

A system reset is generated when any of the following events occurs:

- **Low level on the NRST pin (external reset)**
- **Option byte loader reset**
- **Window watchdog count termination (WWDG reset)**
- **Independent watchdog count termination (IWDG reset)**

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- **Power reset (POR/PDR/BOR)**
- **Software reset (SW reset): Achieved by setting the SYSRESETREQ bit to '1' in the Cortex®-M0 Interrupt Enable and Reset Control Register.**

All reset sources ultimately act on the NRST pin and hold it low during the reset process. The reset entry vector is fixed at address 0x0000 0004. The internal reset signal is output on the NRST pin.

The internal reset signal is output on the NRST pin. A pulse generator ensures that these (external or internal) reset sources generate a pulse with a minimum delay of 40 µs. When the NRST pin is pulled low to generate an external reset, it produces a reset pulse.

4.8 System Configuration Controller (SYSCFG)

This series of chips includes a set of system configuration registers. The main functions of the system configuration controller are as follows:

- **Remap memory to the code start area.**
- **Manage external interrupts connected to GPIO pins.**
- **Control the switching of internal analog signals to I/O outputs.**
- **Control I/O filtering functionality.**
- **Enable/disable the internal noise filter.**

4.8.1 Power Reset

A power reset is generated when any of the following events occurs:

- **Power-on/power-down reset (POR/PDR)**
- **Brown-out reset (BOR)**

The chip integrates an internal power-on reset (POR)/power-down reset (PDR) circuit. This circuit is always active to ensure normal system operation when the supply exceeds 2.2 V. When VDD falls below the POR/PDR threshold, the MCU is reset without requiring any external reset circuitry.

The chip also integrates an internal brown-out reset (BOR) circuit. The BOR option is disabled by default, meaning the power supply is monitored by POR/PDR. Users can enable or disable the BOR function by configuring the MCU option bytes.

4.9 Clock and Clock Tree

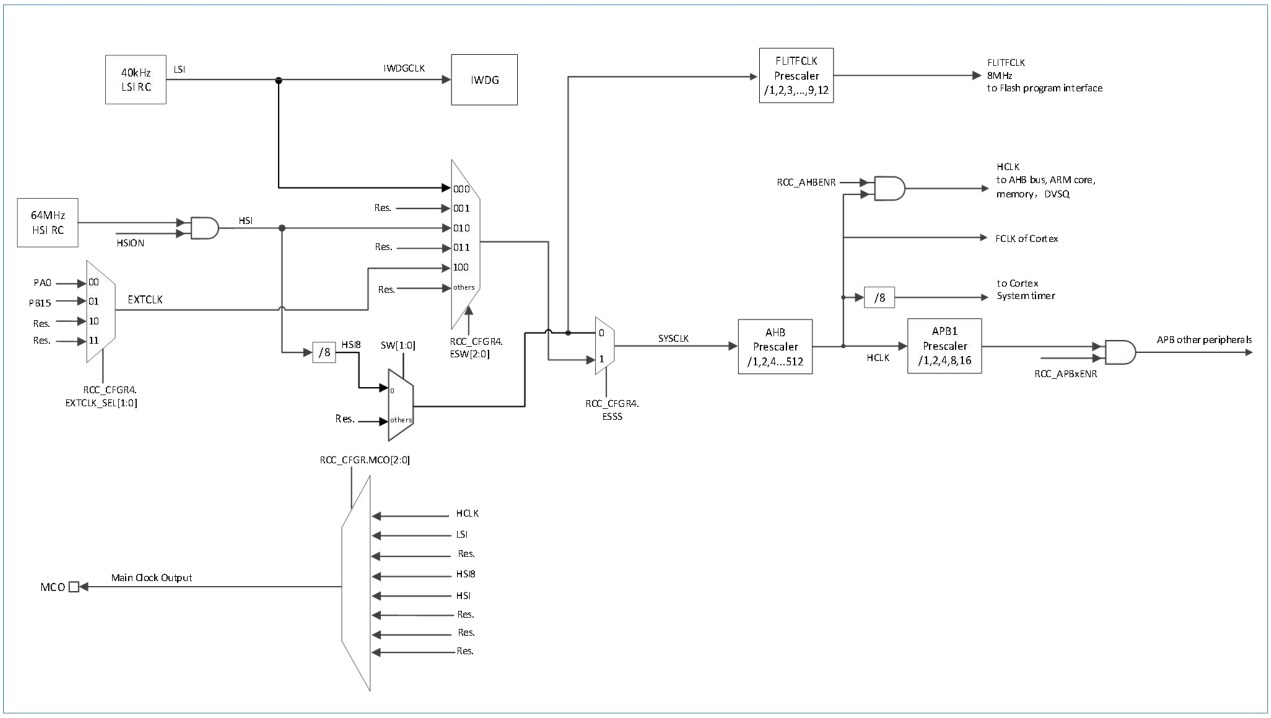

Figure 4-4 Clock Tree

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Upon startup, the device selects the system clock (SYSCLK) as the CPU operating clock. The 64 MHz clock output from the internal oscillator is divided to provide HSI8, which serves as the default system clock after power-on.

The device provides multiple clock sources for the system clock, offering customers flexible and diverse operating modes. The following clocks can be used as the system clock:

- **Internal high-speed clock (HSI): 8 MHz / 64 MHz**
- **Internal low-speed clock (LSI): 40 kHz**
- **GPIO external input clock: 0 MHz to 32 MHz**

The clock frequencies of the AHB and APB domains can be configured via prescalers. The maximum clock frequency of the AHB bus can reach 64 MHz. The maximum clock frequency of the APB domain can reach 64 MHz.

4.10 General-Purpose I/O (GPIO)

Each GPIO pin can be configured by software as output (push-pull or open-drain), input (floating, pull-up, or pull-down), or as an alternate peripheral function. Most GPIO pins are shared with digital or analog peripherals. All GPIO pins have high current capability. If required, the peripheral function of an I/O pin can be locked through a specific operation to prevent accidental write access to the I/O registers. Each I/O has a dedicated 32-bit port control register for configuring its function.

4.11 Interrupts and Events

4.11.1 NVIC

The Nested Vectored Interrupt Controller (NVIC) is tightly coupled with the processor core interface, enabling low-latency interrupt handling and efficient processing of late-arriving interrupts. The NVIC manages interrupts including core exceptions.

- **28 maskable interrupt channels (excluding the 16 Cortex-M0 interrupt lines)**
- **4 programmable interrupt priority levels (using 2-bit interrupt priority)**
- **Low-latency exception and interrupt processing**
- **Power management control**
- **Implementation of system control registers**

4.11.2 EXTI

The Extended Interrupt and Event Controller (EXTI) manages internal and external asynchronous interrupts and events: it generates event requests to the CPU, interrupt requests to the interrupt controller, and wake-up requests to the power management module.

Each interrupt or event EXTI line can be independently masked or enabled.

- **Supports up to 18 event/interrupt requests**
  - **17 configurable EXTI lines**
    - Selectable rising or falling edge trigger
    - Dedicated interrupt status flag
    - Interrupts/events can be triggered by software
  - **1 non-configurable EXTI line (1)**
- **Each interrupt/event line can be individually triggered and masked.**
- **Capable of detecting external signals with pulse widths shorter than the APB clock period.**

Note:

Configurable EXTI lines refer to those where the interrupt/event trigger edge is configurable.

Non-configurable EXTI lines refer to those that do not support configuration via EXTI register bits.

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4.12 Timers

This MCU series includes one advanced control timer, two general-purpose timers, and one hall timer. The timer functions are defined in the following table.

Table 4-1 Timer Function Definition

Type	Timer Name	Counter Resolution	Counter Type	Prescaler Factor	DMA Request	Emergency Brake Input	Hall Input	Capture/ Compare Channel	Complementary Output
Advanced Timer	ATU	16-bit	Up-counting, Down-counting, and Triangular-wave (Center-Aligned) Counting modes	2^n(n=0..3)	None	Yes	None	6	3
General-Purpose Timer	UTU1	32-bit	Up-counting	2^n (n=0..7)	None	Yes	None	2	1
	UTU2	16-bit	Up-counting	2^n (n=0..7)	None	Yes	None	2	1
Hall Timer	HTU	24-bit	Up-counting	2^n (n=0..3)	None	None	3	None	None

4.12.1 Advanced Timer (ATU)

The Advanced Timer (ATU) incorporates a 16-bit auto-reload counter driven by a configurable prescaler.

The ATU can generate multiple types of PWM output waveforms (edge-aligned PWM, center-aligned PWM, complementary PWM with asymmetric dead time, etc.).

The ATU operates completely independently and does not share any resources with other internal timers.

Key features of the ATU timer include:

- **16-bit auto-reload counter, supporting up-counting, down-counting (sawtooth), and triangular-wave (center-aligned) modes.**
- **Programmable timer clock prescaler with division factors of 1, 2, 4, or 8.**
- **Capable of outputting 6 independent PWM waveforms or 3 complementary PWM waveforms.**
  - Independent PWM Waveforms:

    The compare intervals for Channels A and B can be configured independently to output PWM waveforms where Channels A and B operate independently of each other.
  - Center-Aligned Complementary PWM Waveforms:

    The compare intervals for Channels A and B can be freely programmed to form asymmetric PWM waveforms.

    The dead time for Channels A and B can be freely programmed to form asymmetric PWM waveforms with dead time.
  - Independent Inverted PWM Waveforms:

    Sawtooth Mode: Can output waveforms with phase shift and 50% duty cycle.

    Triangular-wave Mode: Can output PWM waveforms with configurable duty cycle.
- **Flexible auto-reload configuration; register values can be auto-reloaded triggered by peak or valley signals.**
- **Protection input signal that can force the ATU output signals to a reset or a predefined state.**
- **Internal IOMUX allowing configuration of the 6 PWM outputs to any of the ATU output pins.**
- **Two trigger signals, TRG0 and TRG1, capable of triggering synchronized ADC sampling.**
- **TRGDB can coordinate with the ADC dual sampling mode to synchronously trigger dual sampling for**

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ADC GroupB.

- **Comparator (CMP) output blanking function to suppress noise generated during PWM switching within a set time period.**
- **Synchronization trigger circuit enabling the ATU to synchronize with other internal timers.**

4.12.2 General-Purpose Timer (UTU)

This series of MCUs integrates two general-purpose timers, UTU1 and UTU2, which share identical functionality except for differing bit widths.Key features of the general-purpose timers include:

- **32/16-bit (UTU1 is 32-bit, UTU2 is 16-bit) automatic counter loading**
- **3-bit real-time programmable prescaler with divisor factors of 2^n (n=0..7) for programmable counter clock frequency.**
- **Supports both input capture and output compare functions with two capture/compare channels.**
- **Input capture features:**
  - Input filtering capability with configurable filter length.
  - Supports rising edge, falling edge, and both edges triggering.
  - Supports single-channel periodic capture.
  - Supports dual-channel PWM period and duty cycle capture.
- **Comparison output features:**
  - Supports two independent PWM output modes.
  - Supports one complementary PWM output mode.
  - Supports pulse output mode (fixed 50% duty cycle).
  - Supports single-cycle output mode, which can be triggered by software, ATU, or another UTU.
  - Supports output protection functionality; polarity, duration, and default protection output polarity of trigger signals are configurable.
  - Supports output protection in debug mode (Halt).
  - Supports automatic cancellation of output protection upon completion of the timing cycle.
- **Synchronous control of other peripherals**
  - Supports single-trigger operation of ATU or another UTU.
  - Supports periodic triggering of ADC sampling.

4.12.3 Hall Timer (HTU)

The Hall Timer Unit (HTU) is driven by a programmable prescaler. The HTU incorporates a 24-bit auto-load counter, supporting three Hall signal inputs for detecting Hall phase sequence and comparator-linked counting.

The HTU is entirely independent, sharing no resources with other timers.

Key features of the HTU include:

- **24-bit auto-load counter with up-counting capability**
- **Support for three Hall signal inputs**
- **Noise filtering for Hall input signals**
- **Eight 24-bit Hall signal buffer registers**
- **Hall sequence detection**
- **Phase-shift averaging functionality supporting 2/4/8-phase averaging**
- **HTU and comparator CMP synchronised counting**

4.12.4 SysTick Timer

The SysTick timer is dedicated to operating systems and functions as a standard decrementing counter. It possesses the following characteristics:

- **24-bit decrementing counter**
- **Reload capability**

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- **Generates a maskable interrupt upon reaching zero**
- **Programmable clock source**

4.13 Independent Watchdog (IWDG)

The independent watchdog is clocked by an internal, independent 40kHz RC oscillator (LSI), featuring a 12-bit decrementing counter and an 8-bit prescaler. As this RC oscillator operates independently of the main clock, it can function during shutdown mode. The IWDG is employed to reset the entire system upon fault detection or functions as a free-running timer for application-level timeout management. Configuration via the option byte enables either software or hardware initiation of the watchdog. During debug mode, this counter may be frozen.

Configuration of the IWDG_WINR register enables the IWDG to operate in window mode.

The IWDG incorporates an interrupt function. When the watchdog counter reaches the value configured in the IWDG_IRQCFG register, it generates the IWDG_IRQ interrupt signal. This can prompt the system to save critical data before a watchdog reset or be utilised for timed wake-up in low-power modes.

4.14 Window Watchdog (WWDG)

The window watchdog incorporates a 7-bit decrementing counter. This counter may be configured for free-running operation or as a watchdog to reset the entire system upon system failure. Driven by the main clock, the window watchdog features an advance warning interrupt function. In debug mode, this counter may be frozen.

4.15 Analog-to-Digital Converter (ADC)

It features a built-in 12-bit Analog-to-Digital Converter (ADC) module with two sample groups. The two sample groups can operate simultaneously or individually. Each group's sampling channels can be configured independently, supporting up to 14 external channels (corresponding to 16 external pins) and 6 internal channels.

- **12-bit fixed resolution.**
- **The ADC operating clock can reach 32 MHz. At 12-bit resolution, the ADC sampling rate can reach up to 2.285 MSPS.**
- **ADC conversion time: At a 2 MSPS conversion rate, the conversion time for 12-bit resolution is 0.5 μs.**
- **The ADC features programmable sampling time; the sampling time for each channel can be configured independently.**
- **Supports synchronized trigger sampling from ATU, UTU1, UTU2, and CMP.**
- **Supports multiple operating modes including Group sampling mode, Dual sampling mode, Continuous sampling mode, and Oversampling averaging mode.**
- **Flexible configuration of sampling sequence for ease of use in different application scenarios.**
- **Conversion data supports both left-aligned and right-aligned formats.**
- **Analog window comparison function, supporting window comparison which can trigger an interrupt.**
- **Configurable number of trigger ignores.**
- **Flexible bias value setting.**
- **Each conversion group channel has an independent result register.**
- **Features priority preemption functionality.**

4.15.1 Internal Reference Voltage (VREFINT)

The internal reference voltage (VREFINT) provides a stable (bandgap) voltage output for the ADC.

4.15.2 VREFP Internal Supply Voltage

The VREFP internal supply voltage can be selected from 2.4V Vref, 3.6V Vref, or VDDA.

Note:

When selecting 2.4V Vref as the VREFP internal supply voltage, VDD must be above 2.9V. When selecting 3.6V Vref, VDD must be above 4V.

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4.15.3 Temperature Sensor (TS)

The temperature sensor generates a voltage that varies linearly with temperature, approximately in the range of 300 mV (@ -40°C) to 600 mV (@ +105°C). The temperature sensor is internally connected to the TS input channel of the ADC, used to convert the sensor's output voltage into a digital value.

Due to process variations, the offset of the temperature sensor differs from chip to chip. The internal temperature sensor is suitable for applications detecting temperature changes rather than measuring absolute temperature. If accurate temperature readings are required, an external temperature sensor component should be used.

4.16 Voltage Divider (VDIV)

An internal 10-bit voltage divider (VDIV) is included, which can be used to convert a digital signal into an analog voltage output. When the VDIV channel is enabled and a value is written to the VDIV channel data register, a corresponding analog output voltage is generated on the VDIV channel.

- **One channel data register**
- **10-bit voltage output**
- **One write-protection register**

4.17 Programmable Gain Amplifier (PGA)

The device integrates two programmable gain amplifiers (PGA1 and PGA2). Their main features are as follows:

- **Rail-to-rail input/output**
- **Low offset voltage**
- **Supports differential input or single-ended input**
- **Multiple gain options (x1, x4, x8, x12, x20, x40)**
- **Built-in multi-level bias voltages (Vref/2, Vref/4, Vref/8, Vref/16)**
- **PGA1 supports polling amplification for two sets of input signals**
- **PGA1 supports automatic or manual switching between the two input signal sets during polling operation**
- **Supports cascaded amplification of PGA1 and PGA2**
- **Supports register write protection**

The PGAs can operate in the following modes:

- **Polling Mode (supported only by PGA1)**
- **Pin-Saving Mode**
- **Cascaded Mode**

4.18 Voltage Comparator (CMP)

The device integrates two comparators, CMP1 and CMP2. These comparators can be used independently and serve the following purposes:

- **Analog signal conditioning.**
- **When combined with the PWM output of a timer, they form a cycle-by-cycle current control loop.**

The main features of the CMP include:

- **Configurable comparator hysteresis mode.**
- **Configurable hysteresis thresholds: 0/10/30/60 mV.**
- **Configurable comparator output polarity.**
- **Flexible input selection for each comparator; both positive and negative inputs are configurable.**
  - Multiple I/O pins are provided for positive/negative input selection.
  - Multiple positive input options such as PGAx_OUTx and PGAx_P are provided.
  - Negative input options such as VDIV_OUT and BEMF_N are provided. VDIV_OUT is the internal VDIV output, and BEMF_N is the internal neutral point.
- **The comparator output can serve as an input protection signal for the ATU/UTU.**
- **Supports digital filter function.**

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- **Built-in real-time BEMF neutral point detection.**
- **ATU PWM blanking time masking function.**
- **The filtered comparator output can be used to trigger ADC sampling.**

4.19 Division and Square Root Unit (DVSQ)

The Division and Square Root (DVSQ) calculation unit supports the following features:

- **Supports 32-bit signed (SDIV) and unsigned (UDIV) division, and 32-bit square root operation.**
- **The DVSQ unit cannot perform division and square root operations simultaneously; only one operation can be executed at a time.**
- **Upon completion of a 32-bit signed/unsigned integer division operation, both the quotient and remainder can be obtained simultaneously and updated to the corresponding registers.**
- **Division operations support the MOD operation.**
- **For unsigned square root operations, high-precision calculation can be selected via software.**
- **Pipeline design, processing 2 bits per clock cycle.**
- **Calculation time varies depending on the operands.**
- **Supports divide-by-zero interrupt and overflow interrupt.**

4.20 I²C Bus

The MCUs of this series feature one I²C bus interface, capable of operating in multi-master and slave modes, supporting Standard mode (up to 100 kHz), Fast mode (up to 400 kHz), and Ultra-Fast mode (up to 1 MHz).

The I²C clock is derived from PCLK2.

Table 4-2 I2C Characteristics

I²C Characteristics	I²C 1
Master/Slave Mode	Supported
Multi-host mode	Supported
Standard/fast mode	Supported
7/10-bit addressing mode	Supported
Broadcast call	Supported
Event management	Supported
Clock extension	Supported
Software reset	Supported
DMA Transfer	Not Supported
Digital and analog filters	Supported

4.21 Universal asynchronous receiver transmitter(UART)

The device integrates two Universal Asynchronous Receiver/Transmitters (UART1/UART2), supporting a maximum communication rate of up to 8 Mbit/s. They support functions such as single-wire half-duplex communication and multi-processor communication. Additionally, they feature noise filtering to eliminate signal glitches and resynchronization to tolerate larger clock deviations.

The extended mode supports LIN master mode break transmission and LIN slave mode break detection functions.

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Table 4-3 UART characteristics

UART Characteristics	UART1/UART2
Data word length	8/9 bits
Multi-processor communication	Supported
Single-wire half-duplex communication	Supported
LIN Mode	Supported
Noise Filtering	Supported
Resynchronization	Supported

4.22 Serial Peripheral Interface (SPI)

The MCUs of this series feature up to one SPI interface, supporting both slave and master modes, as well as full-duplex and half-duplex communication modes. The SPI can use a 3-bit prescaler to generate 8 master mode frequencies, and each frame can be configured for 4-bit to 16-bit data.

Table 4-4 SPI Characteristics

SPI Characteristics	SPI 1
Hardware CRC calculation	Not Supported
RX/TX FIFO	Supported
NSS pulse mode	Supported
TI mode	Not Supported
DMA Transfer	Not Supported

4.23 Debug Interface (DBG)

The embedded ARM SWJ-DP interface enables a Serial Wire Debug (SWDIO/SWCLK) debug interface.

4.24 96-bit UID

The reference number provided by the 96-bit product unique identity (UID) is unique to any individual YuanNengXin chip under all circumstances. This identity cannot be modified by the user. Depending on the application, this 96-bit UID can be read in units of bytes (8 bits), half-words (16 bits), or full words (32 bits). The 96-bit UID is suitable for:

- **Use as a serial number (e.g., for USB string serial numbers or other end applications).**
- **Use as a password. When programming the flash memory, this UID can be used in conjunction with software encryption/decryption algorithms to enhance the security of the code within the flash memory.**
- **Activating a secure boot process with security mechanisms.**

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5 Electrical Characteristics

5.1 Maximum Absolute Ratings

The maximum rated value is only a short-term pressure value.

Notes：

- Do not operate the chip at this value or any other conditions exceeding the recommended values.
- Refer to Table 5-1 to 5-3 for the maximum rated values of the chip. Exceeding the maximum rated values may result in permanent damage to the chip.
- Operating for prolonged periods at maximum rated values may affect the chip's reliability.

5.1.1 Limit Voltage Characteristics

Table 5-1 Limit Voltage Characteristics

Symbol	Description	Minimum	Maximum	Unit
V_{DD}-V_{SS} (1)	Voltage Range	-0.3	5.8	V
V_{IN} (1)	Input voltage on pins	-0.3	5.8	

(1). Guaranteed by process.

5.1.2 Limit Current Characteristics

Table 5-2 Limit Current Ch aracteristics

Symbol	Parameter	Maximum	Unit
I_{VDD}(1)	Total current through V_{DD} power lines (supply current) (5)	120	mA
I_{VSS}(1)	Total current through VSS ground lines (output current) (5)	95	
I_{IO}(1)	Output sink current on any I/O and control pin	50	
	Output source current on any I/O and control pin	50	
$I_{INJ(PIN)}$ (1)	Injected current on a pin (2)(3)	-3/+3	
$\Sigma I_{INJ(PIN)}$ (1)	Total injected current on all I/O and control pins (4)	-30/+30	

(1). Guaranteed by design.

(2). Reverse injected current may disturb the analog performance of the device.

(3). When $V_{IN} > V_{DD}$, a forward injected current occurs; when $V_{IN} < V_{SS}$, a reverse injected current occurs. The injected current must never exceed the specified range.

(4). When several I/O pins have injected current simultaneously, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of forward and reverse injected currents.

(5). All power (V_{DD}) and ground (V_{SS}) pins must always be connected to the power supply system within the externally allowable range.

5.1.3 Limit Temperature Characteristics

Table 5-3 Limit Temperature Characteristic

Symbol	Parameter	Minimum	Maximum	Unit
T_{STG}(1)	Storage temperature range	-65	150	°C
T_J(1)	Maximum junction temperature	-40	125	°C

(1). Design guaranteed.

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5.2 Operating Parameters

5.2.1 Recommended Operating Conditions

Table 5-4 Recommended Operating Condition

Symbol	Parameter	Minimum	Maximum	Unit
f_{HCLK}(1)	Internal APB Clock Frequency	-	64	MHz
f_{PCLK1}(1)	Internal APB1 Clock Frequency	-	64	
V_{DD}	Standard Operating Voltage	2.2	5.5	V
T(1)	Operating Temperature	-40	105	°C

(1). Design guaranteed.

5.2.2 Power-On/Power-Down Slew Rate Operating Conditions

Table 5-5 Power-On/Power-Down Slew Rate Operating Conditions

Symbol	Parameter	Condition	Minimum	Maximum	Unit
t_{VDD}(1)	V_{DD} Rise Slew Rate	-	2	20,000	µs/V
	V_{DD} Fall Slew Rate	-	30	∞	µs/V

(1). Design guaranteed.

5.2.3 Programmable Voltage Detector (PVD) Characteristics

Table 5-6 PVD Characteristics

Symbol	Parameter	Threshold	Minimum	Typical Value	Maximum	Unit
V_{PVD}	PVD detection level selection (V_{DD} rising edge) (-40°C to +105°C)	V_{PVD1}	2.291	2.333	2.383	V
		V_{PVD2}	2.491	2.533	2.582	
		V_{PVD3}	2.681	2.731	2.781	
		V_{PVD4}	2.872	2.928	2.98	
		V_{PVD5}	3.063	3.127	3.172	
		V_{PVD6}	3.259	3.324	3.37	
		V_{PVD7}	3.451	3.524	3.572	
		V_{PVD8}	3.648	3.728	3.772	
		V_{PVD9}	3.852	3.928	3.971	
		V_{PVD10}	4.049	4.13	4.179	
		V_{PVD11}	4.242	4.329	4.373	
		V_{PVD12}	4.442	4.527	4.571	
		V_{PVD13}	4.65	4.74	4.782	
		V_{PVD14}	4.842	4.934	4.982	

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Symbol	Parameter	Threshold	Minimum	Typical Value	Maximum	Unit
	PVD detection level selection (V_{DD} falling edge) (-40°C to +105°C)	V_{PVD1}	2.239	2.284	2.315	V
		V_{PVD2}	2.439	2.484	2.518	
		V_{PVD3}	2.636	2.682	2.719	
		V_{PVD4}	2.835	2.883	2.931	
		V_{PVD5}	3.037	3.085	3.127	
		V_{PVD6}	3.227	3.284	3.329	
		V_{PVD7}	3.428	3.486	3.538	
		V_{PVD8}	3.625	3.69	3.747	
		V_{PVD9}	3.825	3.889	3.949	
		V_{PVD10}	4.026	4.091	4.149	
		V_{PVD11}	4.216	4.291	4.355	
		V_{PVD12}	4.408	4.487	4.548	
		V_{PVD13}	4.629	4.701	4.767	
		V_{PVD14}	4.808	4.891	4.966	

5.2.4 Brown-Out Reset (BOR) Characteristics

Table 5-7 BOR Characteristics

Symbol	Parameter	Threshold	Minimum	Typical Value	Maximum	Unit
V_{BOR}	BOR[1] Detection Level Selection (V_{DD} Rising Edge) (-40°C to +105°C)	V_{BOR1}	2.291	2.333	2.383	V
		V_{BOR2}	2.491	2.533	2.582	
		V_{BOR3}	2.681	2.731	2.781	
		V_{BOR4}	2.872	2.928	2.98	
		V_{BOR5}	3.063	3.127	3.172	
		V_{BOR6}	3.259	3.324	3.37	
		V_{BOR7}	3.451	3.524	3.572	
		V_{BOR8}	3.648	3.728	3.772	
		V_{BOR9}	3.852	3.928	3.971	
		V_{BOR10}	4.049	4.13	4.179	
		V_{BOR11}	4.242	4.329	4.373	
		V_{BOR12}	4.442	4.527	4.571	
		V_{BOR13}	4.65	4.74	4.782	

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Symbol	Parameter	Threshold	Minimum	Typical Value	Maximum	Unit
		V_{BOR14}	4.842	4.934	4.982	
	BOR[1] Detection Level Selection (V_{DD} Falling Edge) (-40°C to +105°C)	V_{BOR1}	2.239	2.284	2.315	V
		V_{BOR2}	2.439	2.484	2.518	
		V_{BOR3}	2.636	2.682	2.719	
		V_{BOR4}	2.835	2.883	2.931	
		V_{BOR5}	3.037	3.085	3.127	
		V_{BOR6}	3.227	3.284	3.329	
		V_{BOR7}	3.428	3.486	3.538	
		V_{BOR8}	3.625	3.69	3.747	
		V_{BOR9}	3.825	3.889	3.949	
		V_{BOR10}	4.026	4.091	4.149	
		V_{BOR11}	4.216	4.291	4.355	
		V_{BOR12}	4.408	4.487	4.548	
		V_{BOR13}	4.629	4.701	4.767	
		V_{BOR14}	4.808	4.891	4.966	
$V_{BORhyst}$	BOR Hysteresis	-	-2	67	155	mV
t_{BORRST}[2]	Effective Time	-	-	40	-	μs

(1). BOR monitors V_{DD} only.

(2). Design guaranteed.

5.2.5 Power-On/Power-Down Reset (POR/PDR) Characteristics

Table 5-8 Power-On/Power-Down Reset characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
$V_{POR/PDR}$	POR/PDR Thresholds[1]	Falling Edge	1.977	2.006	2.049	V
		Rising Edge	2.031	2.07	2.112	V
$V_{PDRhyst}$	PDR Hysteresis	-	12	64	125	mV
$t_{RSTTEMPO}$[2]	Reset Timing	-	-	4	-	ms

(1). PDR and POR monitor V_{DD} only.

(2). Design guaranteed.

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5.2.6 Internal Reference Voltage Characteristics

Table 5-9 Internal Reference Voltage Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value(2)	Maximum	Unit
V_{REFINT}(1)	Internal Reference Voltage	-40 ~ 105°C; VDD =2.2~5.5V	1.18	1.2	1.22	V
$Ripple_{REFINT}$(3)	Reference Voltage Variation Over Full Temperature Range	-40 ~ 105°C; VDD =2.2~5.5V	-1.65	-	1.65	%

(1). Actual test results of multiple samples after trimming completion.

(2). Target value for trimming.

(3). Actual test results of multiple samples for the temperature coefficient at 20°C.

5.2.7 Operating Current Characteristics

Table 5-10 Operating Current Characteristics

Symbol	Mode	Condition	V_{DD}=3.3V				V_{DD}=5V				Unit
			-40°C	25°C	85°C	105°C	-40°C	25°C	85°C	105°C	
I_{DD}	Run Mode	CPU running at 64 MHz; All peripherals enabled.	6.43	6.50	6.52	6.53	6.49	6.57	6.60	6.61	mA
		CPU running at 64 MHz; All peripherals enabled.	4.14	4.22	4.28	4.30	4.19	4.28	4.35	4.37	mA
		CPU running at 8 MHz; All peripherals enabled.	2.12	2.19	2.26	2.29	2.20	2.29	2.36	2.38	mA
		CPU running at 8 MHz; All peripherals enabled.	1.84	1.91	1.99	2.01	1.92	2.01	2.08	2.11	mA
I_{Sleep}	Sleep Mode	CPU running at 64 MHz; All peripherals disabled; All IOs configured in analog mode.	1.95	2.01	2.07	2.09	2.06	2.13	2.19	2.21	mA
		CPU running at 8 MHz; All peripherals disabled; All IOs configured in analog mode.	1.84	1.91	1.98	2.01	1.92	2.01	2.08	2.11	mA
		CPU running at 40 kHz; All peripherals disabled; All IOs configured in analog mode.	0.96	1.04	1.11	1.14	1.08	1.16	1.23	1.26	mA
I_{Stop}	Normal Stop Mode	CPU halted; IWDG disabled; All other peripherals halted; All IOs configured in analog mode.	0.16	0.19	0.22	0.24	0.16	0.19	0.23	0.24	mA

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Symbol	Mode	Condition	V_{DD}=3.3V				V_{DD}=5V				Unit
$I_{lp\text{-}Stop}$	Low-power Stop Mode	CPU halted; IWDG disabled; All other peripherals halted; All IOs configured in analog mode.	0.03	0.04	0.05	0.05	0.04	0.04	0.05	0.06	mA

(1). Design guarantee.

5.2.8 Internal High-speed HSI Clock Characteristics

Table 5-11 HSI Clock Characteristics

Symbol	Parameter	Condition		Minimum	Typical Value	Maximum	Unit
f_{HSI}(1)	Factory Calibration Target Frequency	-		-	64	-	MHz
DuCy(1)	Duty cycle	-		45	-	55	%
ACC	Oscillator accuracy	Factory Calibration, Room Temperature		-1	-	1	%
		Factory calibration	T_A= –40 ~ +105°C	-3.2	-	2.1	%
$T_{su(HSI)}$(1)	Oscillator start time	-		-	3.95	-	μs
$I_{DD(HSI)}$(1)	Power consumption of oscillator	64MHz, V_{DD}=5V		-	430		μA

(1). Design guarantee.

5.2.9 Internal Low-speed LSI Clock Characteristics

Table 5-12 LSI Clock Characteristics

Symbol	Parameter	Condition		Minimum	Typical Value	Maximum	Unit
f_{LSI}(1)	Factory Calibration Target Frequency	-		-	40	-	KHz
ACC	Oscillator accuracy	Factory Calibration, Room Temperature		-1	-	1	%
		Factory calibration	T_A= –40 ~ +105°C	-4.4	-	1.9	%
$T_{su(LSI)}$(1)	Oscillator start time	-		-	2.6	-	μs
$I_{DD(LSI)}$(1)	Power consumption of oscillator			-	30	-	μA

(1). Design guarantee.

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5.2.10 GPIO External Clock Input Characteristics

Supports clock input from PA0 and PB15. The waveform requirements are as follows:

Table 5-13 GPIO External Clock Input Characteristics

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit
F_{Ext}	Input Clock Frequency	0	-	32	MHz
	Input Clock Duty Cycle	45	-	55	%

5.2.11 Flash Memory Characteristics

Table 5-14 Flash Memory Characteristics(1)(2)

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit
T_{PROG}	Half-word write time	10	-	13	μs
T_{ERASE}	Page erase time	2	-	3	ms
	Chip erase time	30	-	40	ms
I_{DDPROG}	Programming current	-	-	1.2	mA
$I_{DDERASE}$	Page/chip erase current	-	-	0.6	mA
I_{DDREAD}	Read current	-	-	1.2(@25MHz)	mA
N_{END}	Write/erase endurance	100	-	-	k times
t_{RET}	Data retention time	10@105°C	20@85°C	100@25°C	years

(1). Typical values are measured at 1.5V TT process and 25°C.

(2). Design guaranteed.

5.2.12 IO Input Pin Characteristics

Table 5-15 IO Input Pin DC Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
V_{IH}	Input High Level	V_{DD}=5.0V	0.7*V_{DD}	-	-	V
V_{IL}	Input Low Level	V_{DD}=5.0V	-	-	0.3* V_{DD}	V
V_{hys}	Schmitt Trigger Hysteresis Voltage	V_{DD}=5.0V	870	920	990	mV
I_{lkg}	Input Leakage Current	V_{DD}=5.0V	-10	-	55	μA
R_{PU}	Pull-up Resistor	V_{DD} =5.0V	18	24	34	KΩ
R_{PD}	Pull-down Resistor	V_{DD} =5.0V	17	23	35	KΩ
C_{IO}(1)	I/O Pin Capacitance	V_{DD} =5.0V	-	5	-	pF

(1). All I/Os support Schmitt trigger functionality; design guaranteed.

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5.2.13 IO Output Pin Characteristics

Table 5-16 IO Output Pin DC Characteristics(1)

Symbol	Parameter	Condition			Minimum	Typical Value	Maximum	Unit
		Drive Strength OSPEEDRy[1:0]	V_{DD} Voltage (V)	$V_{OH(min)}/V_{OL(max)}$ Voltage Value(V)				
I_{OH}	Output source current	2'bx0	2.5	1.7	-	2.39	-	mA
			3.3	2.4	-	3.67	-	mA
			5	3.5	-	7.87	-	mA
		2'b01	2.5	1.7	-	12.68	-	mA
			3.3	2.4	-	18.79	-	mA
			5	3.5	-	38.49	-	mA
		2'b11	2.5	1.7	-	16.37	-	mA
			3.3	2.4	-	23.9	-	mA
			5	3.5	-	49.14	-	mA
I_{OL}	Output sink current	2'bx0	2.5	0.5	-	2.16	-	mA
			3.3	0.66	-	3.74	-	mA
			5	1	-	7.66	-	mA
		2'b01	2.5	0.5	-	12.3	-	mA
			3.3	0.66	-	20.89	-	mA
			5	1	-	42.20	-	mA
		2'b11	2.5	0.5	-	16.01	-	mA
			3.3	0.66	-	27.06	-	mA
			5	1	-	53.74	-	mA

(1). Design guaranteed.

Table 5-17 IO Output AC Characteristics(1)

Symbol	Parameter	Condition			Minimum	Typical Value	Maximum	Unit
		C_L	Drive Strength OSPEEDRy[1:0]	V_{DD} Voltage (V)				
t_R	Rise Time (Low-to-High Level Output)	C_L=65pF	2'bx0	2.5	-	96	-	ns
				3.3	-	83	-	ns
				5	-	55	-	ns
			2'b01	2.5	-	11.4	-	ns
				3.3	-	10.13	-	ns
				5	-	9.73	-	ns
			2'b11	2.5	-	10.73	-	ns
				3.3	-	8.4	-	ns
				5	-	7.87	-	ns
t_F	Fall Time (High-to-Low Level Output)	C_L=65pF	2'bx0	2.5	-	96	-	ns
				3.3	-	79.67	-	ns
				5	-	53.67	-	ns
			2'b01	2.5	-	10.47	-	ns
				3.3	-	9.67	-	ns

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Symbol	Parameter	Condition			Minimum	Typical Value	Maximum	Unit
		C_L	Drive Strength OSPEEDRy[1:0]	V_{DD} Voltage (V)				
				5	-	8.2	-	ns
			2'b11	2.5	-	9	-	ns
				3.3	-	8	-	ns
				5	-	7.27	-	ns

(1). Design guaranteed.

5.2.14 NRST Reset Pin Characteristics

The NRST pin integrates a pull-up resistor inside, and the peripheral application circuit can be connected to any circuit or an external RC circuit.

Table 5-18 NRST Pin Input Characteristics

Symbol	Parameter	Minimum	Maximum	Unit
T_{Noise}	Low-level is ignored	-	260	ns

An external filter capacitor on the NRST pin is used for noise immunity, preventing unintended chip resets caused by interference. Users must ensure the voltage on the NRST pin remains below the maximum V_{IL} threshold; otherwise, the reset signal will be ignored.

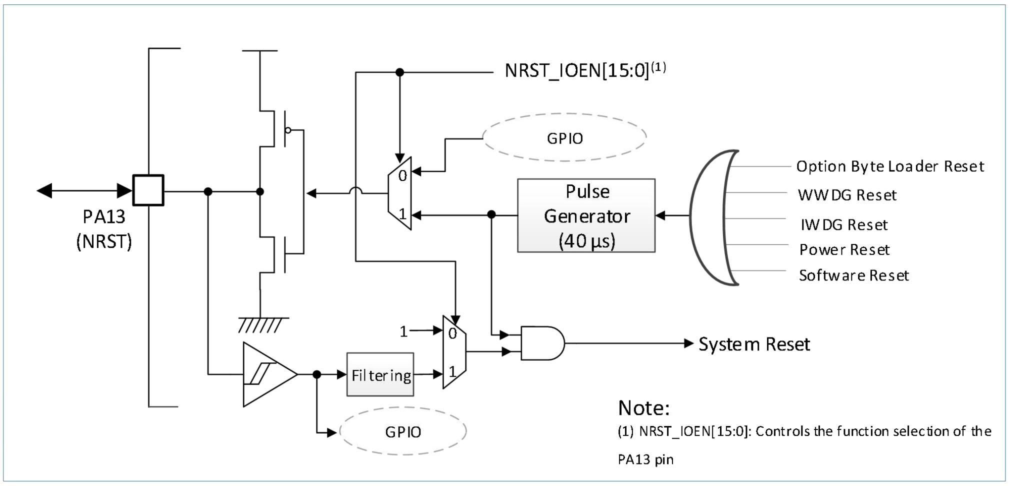

Figure 5-1 Recommended Reset Circuit

5.2.15 Advanced Timer Characteristics

Table 5-19 ATU Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
f_{EXT}(1)	PWM_IO0 ~ PWM_IO5 Output Frequency	$f_{TIMxCLK}$(2)	-	-	$f_{TIMxCLK}/2$	MHz
$t_{res(ATU)}$	Timer Resolution Time	$f_{TIMxCLK}$=64MHz	-	15.6	-	ns
t_{MAX_COUNT}	Clock Period of the 16-bit Counter (when internal clock is selected)	-	-	2^{16}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=64MHz	-	1024	-	µs

(1). Design guaranteed.

(2). The maximum value of $f_{TIMxCLK}$ is 64MHz.

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5.2.16 General-Purpose Timer Characteristics

Table 5-20 UTU Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
f_{EXT}(1)	PWM_IO0 ~ PWM_IO1 Output Frequency	$f_{TIMxCLK}$(2)	-	-	$f_{TIMxCLK}/2$	MHz
$t_{res(UTU)}$	Timer Resolution Time	$f_{TIMxCLK}$=64MHz	-	15.625	-	ns
$t_{MAX\_COUNT\_UTU1}$	Clock Period of the 32-bit Counter (when internal clock is selected)	-	-	2^{32}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=64MHz	-	67.108864	-	s
$t_{MAX\_COUNT\_UTU2}$	Clock Period of the 16-bit Counter (when internal clock is selected)	-	-	2^{16}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=64MHz	-	1024	-	μs

(1). Design guaranteed.

(2). The maximum value of $f_{TIMxCLK}$ is 64MHz.

5.2.17 Hall Timer Characteristics

Table 5-21 HTU Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
$t_{res(HTU)}$	Timer Resolution Time	$f_{TIMxCLK}$=64MHz	-	15.6	-	ns
t_{MAX_COUNT}	Clock Period of the 24-bit Counter (when internal clock is selected)	-	-	2^{24}	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=64MHz	-	262144	-	μs

(1). Design guaranteed.

(2). The maximum value of $f_{TIMxCLK}$ is 64MHz.

5.2.18 Serial Peripheral Interface (SPI) Characteristics

Table 5-22 SPI Characteristics

Symbol	Parameter	Condition	Minimum	Maximum	Unit
f_{SCK} $1/f_{C(SCK)}$	SPI Clock Frequency	Master Mode	-	16	MHz
		Slave Mode	-	24	
$t_{r(SCK)}$ $t_{f(SCK)}$	SPI Clock Rise Time	V_{DD} =5V, Vcore=1.5V, C_{LOAD} = 30 pF	-	2.749	ns
		V_{DD} =3.3V, Vcore=1.5V, C_{LOAD} = 30 pF	-	1.681	ns
		V_{DD} =2.4V, Vcore=1.5V, C_{LOAD} = 30 pF	-	4.128	ns
	SPI Clock Fall Time	V_{DD} =5V, Vcore=1.5V, C_{LOAD} = 30 pF	-	2.071	ns
		V_{DD} =3.3V, Vcore=1.5V, C_{LOAD} = 30 pF	-	1.168	ns
		V_{DD} =2.4V, Vcore=1.5V, C_{LOAD} = 30 pF	-	3.39	ns
$DuCy_{(SCK)}$	SPI Slave Input Clock Duty Cycle	-	30%	70%	ns

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Symbol	Parameter	Condition		Minimum	Maximum	Unit
$t_{SU(NSS)}$	NSS Setup Time	Slave Mode		$4t_{pclk}$	-	ns
$t_{h(NSS)}$	NSS Hold Time	Slave Mode		$2\ t_{pclk} + 10$	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK High Time and SCK Low Time	Master Mode, PCLK = 64 MHz, Prescaler Divisor = 4		$2\ t_{pclk} - 2$	2tpclk + 1	ns
$t_{su(MI)}$	Data Input Setup Time	Master Mode	V_{DD} =5V, Vcore=1.5V, C_{LOAD} = 30 pF	9.815	-	ns
			V_{DD} =3.3V, Vcore=1.5V, C_{LOAD} = 30 pF	9.733	-	ns
			V_{DD} =2.4V, Vcore=1.5V, C_{LOAD} = 30 pF	11.974	-	ns
$t_{su(SI)}$	Data Input Setup Time	Slave Mode	V_{DD} =5V, Vcore=1.5V, C_{LOAD} = 30 pF	-	9.74	ns
			V_{DD} =3.3V, Vcore=1.5V, C_{LOAD} = 30 pF	-	9.717	ns
			V_{DD} =2.4V, Vcore=1.5V, C_{LOAD} = 30 pF	-	9.693	ns
$t_{h(MI)}$	Data Input Hold Time	Master Mode	V_{DD} =5V, Vcore=1.5V, C_{LOAD} = 30 pF	-7.073	-	ns
			V_{DD} =3.3V, Vcore=1.5V, C_{LOAD} = 30 pF	-7.022	-	ns
			V_{DD} =2.4V, Vcore=1.5V, C_{LOAD} = 30 pF	-9.133	-	ns
$t_{h(SI)}$	Data Input Hold Time	Slave Mode	V_{DD} =5V, Vcore=1.5V, C_{LOAD} = 30 pF	-	9.018	ns
			V_{DD} =3.3V, Vcore=1.5V, C_{LOAD} = 30 pF	-	9.073	ns
			V_{DD} =2.4V, Vcore=1.5V, C_{LOAD} = 30 pF	-	9.113	ns
$t_{v(SO)}$	Data Output Valid Time	Slave Mode (after edge enable)	V_{DD} =5V, Vcore=1.5V, C_{LOAD} = 30 pF	-	12.723	ns
			V_{DD} =3.3V, Vcore=1.5V, C_{LOAD} = 30 pF	-	12.934	ns
			V_{DD} =2.4V, Vcore=1.5V, C_{LOAD} = 30 pF	-	15.213	ns
$t_{v(MO)}$	Data Output Valid Time	Master Mode (after edge enable)	V_{DD} =5V, Vcore=1.5V, C_{LOAD} = 30 pF	-	3.569	ns
			V_{DD} =3.3V, Vcore=1.5V, C_{LOAD} = 30 pF	-	3.479	ns
			V_{DD} =2.4V, Vcore=1.5V, C_{LOAD} = 30 pF	-	3.599	ns
$t_{h(SO)}$	Data Output Hold Time	Slave Mode (after edge enable)	V_{DD} =5V, Vcore=1.5V, C_{LOAD} = 30 pF	-	10.714	ns
			V_{DD} =3.3V, Vcore=1.5V, C_{LOAD} = 30 pF	-	10.869	ns
			V_{DD} =2.4V, Vcore=1.5V, C_{LOAD} = 30 pF	-	12.95	ns
$t_{h(MO)}$	Data Output Hold Time	Master Mode (after edge enable)	V_{DD} =5V, Vcore=1.5V, C_{LOAD} = 30 pF	-2.188	-	ns
			V_{DD} =3.3V, Vcore=1.5V, C_{LOAD} = 30 pF	0	-	ns
			V_{DD} =2.4V, Vcore=1.5V, C_{LOAD} = 30 pF	-2.276	-	ns

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5.2.19 ADC Characteristics

Table 5-23 ADC Characteristics

Symbol	Description	Condition	Minimum	Typical Value	Maximum	Unit
V_{DD}	Analog supply voltage when ADC is on	-	2.2	-	5.5	V
f_{ADC}	ADC clock frequency	V_{DD} =2.2~2.7V	-	-	16	MHz
		V_{DD} =2.7~5.5V	-	-	32	MHz
f_S (1)	sampling frequency	f_{ADC} = 32 MHz	-	-	2.285	MSPS
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 32 MHz	-	-	1.88	MHz
		-	-	-	17	Cycles
V_{AIN}	Conversion voltage range	-	V_{SS}	-	V_{DD}	V
R_{AIN} (1)	External input impedance				Please refer to Table 5- 24 for details	kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	0.305	kΩ
C_{ADC} (1)	sample-and-hold capacitor	-	-	4	-	pF
t_S (1)	Sampling time	f_{ADC} = 32 MHz	1.5	-	55.5	Cycles
t_{CONV} (1)	The total conversion time includes the sampling time	12-bit resolution	14	-	68	Cycles

(1). Design guarantee.

The maximum allowable input impedance RAIN must satisfy the following formula:

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

Where: N(Resolution) = 12,T_S is the ADC sampling period (in clock cycles).The allowable error is less than 1/4 LSB Least Significant Bit, LSB.

Table 5-24 Maximum Input Impedance(f_{ADC} = 32 MHz)

Sampling Period Ts(Cycles)	Sampling Time t_S(μs)	Maximum Input Impedance(kΩ)
1.5	0.05	0.9
2.5	0.08	1.71
3.5	0.11	2.51
4.5	0.14	3.32
5.5	0.17	4.12
6.5	0.2	4.93
7.5	0.23	5.73
8.5	0.27	6.54

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Sampling Period Ts(Cycles)	Sampling Time t_S(μs)	Maximum Input Impedance(kΩ)
13.5	0.42	10.56
28.5	0.89	22.64
41.5	1.3	33.11
55.5	1.73	44.38

Table 5-25 ADC Accuracy

Symbol	Parameter(3)	Test Conditions(2)	Minimum	Maximum	Unit
ET	Total unadjustable error	f_{ADC}=32MHz	-6	6	LSB
EO	Offset error	f_{ADC}=32MHz	-2	4	
EG	Gain error	V_{DD}=5V	-3	5	
ED	Differential linearity error (1)	Input Impedance < 1 kΩ	-1.5	1.5	
EL	Integral linearity error (1)	Tested after ADC Calibration	-3	+3	

(1). Design guaranteed.

(2). Test results from multiple samples across the full temperature range.

(3). Parameter description is as follows:

- Total non-adjustable error: the maximum deviation between the actual transfer curve and the ideal transfer curve.
- Offset error: The deviation between the first actual conversion and the first ideal conversion.
- Gain error: The deviation between the last ideal transition and the last actual transition.
- Differential linearity error: the maximum deviation between the actual step and the ideal step.
- Integral linearity error: The maximum deviation between any actual transition and the end point correlation line.

Note：

- ADC accuracy and negative injection current: Avoid injecting negative current on any standard non-robust analog input pin, as this can significantly reduce the accuracy of performing conversions on another analog input pin. It is recommended to add a Schottky diode pin to the standard analog pin that may inject negative current to ground.
- Better ADC performance can be achieved within a limited range of V_{DDA}, frequency, and temperature.
- The data is based on characterization results and has not been tested in production.

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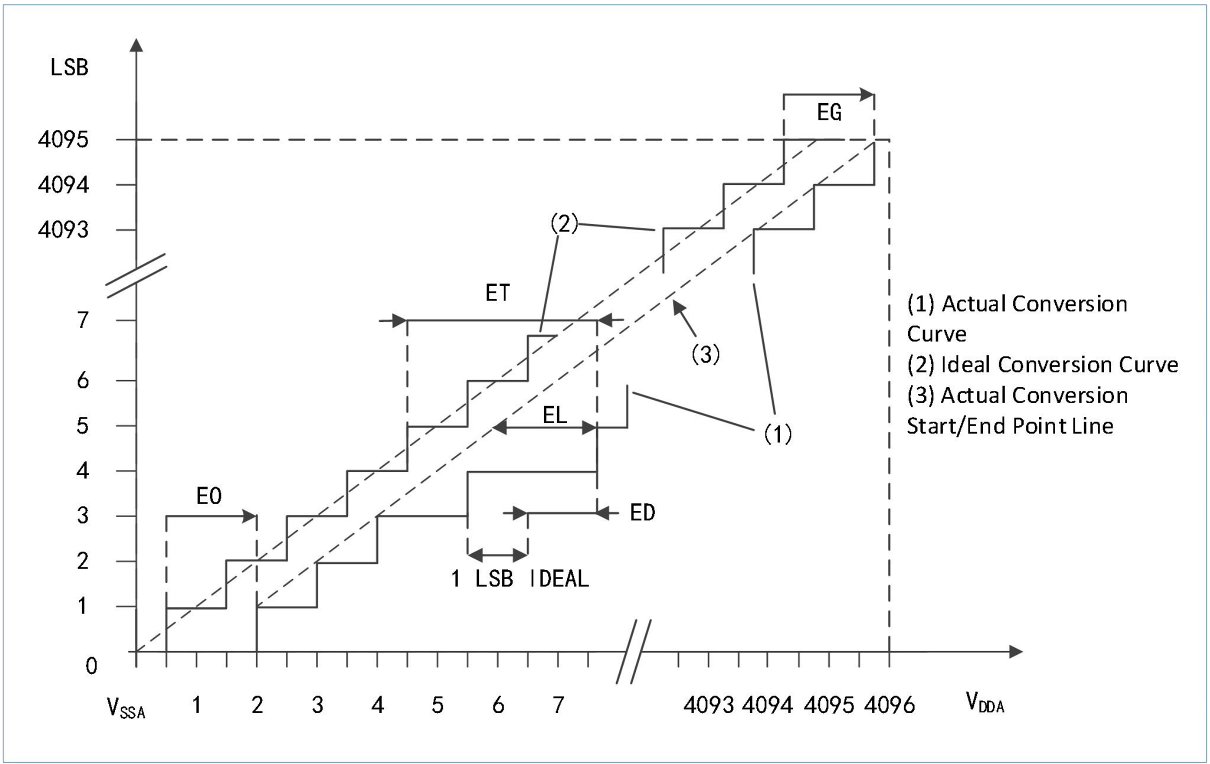

Figure 5-2 ADC Accuracy Characteristics

Note：

For the parameter descriptions represented by EO, ET, EG, EL, and ED, please refer to Table 5-25.

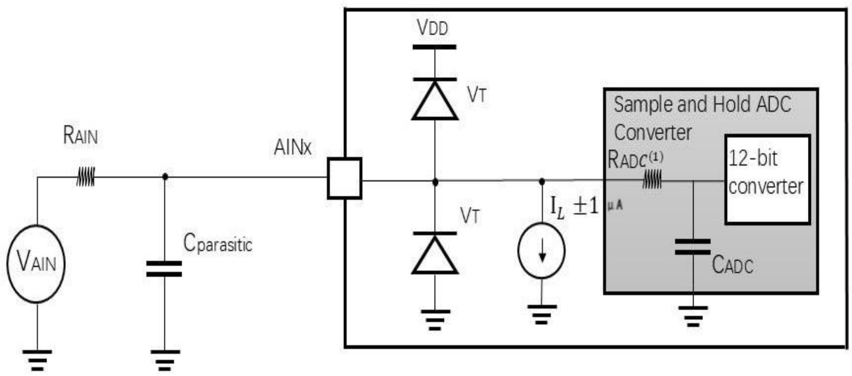

Figure 5-3 Typical ADC Connection Diagram

(1). For R_{ADC} and C_{ADC} values, refer to Table 5-23.

Cparasitic is equal to the PCB capacitance (depending on soldering and PCB layout quality) plus the pad capacitance (approximately 7 pF). If the parasitic capacitance is too high, it will reduce conversion accuracy. To compensate for this, fADC should be minimized.

PCB design recommendations for ADC sampling: Power supply decoupling should follow the guidelines in 6.1 Power Supply. To ensure ADC conversion accuracy, a 10 nF ceramic capacitor is recommended and should be placed as close as possible to the chip.

5.2.20 VREFP Internal Supply Voltage Characteristics

The chip integrates two internal supply voltage levels, 2.4V and 3.6V, to power the ADC VREFP.

Note:

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When selecting 2.4V Vref as the VREFP internal supply voltage, VDD must be above 2.9V. When selecting 3.6V Vref, VDD must be above 4V.

Table 5-26 VREFP Internal Supply Voltage Characteristics

Symbol	Parameter	Conditions	Minimum	Typical Value(2)	Maximum	Unit
VREFP(1)	VREFP Internal Supply Voltage	-40 ~ 105°C; V_{DD} =2.9~5.5V	2.4	2.4	2.44	V
		-40 ~ 105°C; V_{DD} =4~5.5V	3.59	3.6	3.66	V

(1). Actual test results of multiple samples after trimming completion.

(2). Target value for trimming.

5.2.21 Voltage Divider (VDIV) Characteristics

Table 5-27 VDIV Characteristics

Symbol	Parameter	Conditions	Minimum	Typical Value(2)	Maximum	Unit
V_{DD}(1)	VDIV Operating Voltage	-	2.2	-	5.5	V
R_O(1) (2)	Output Impedance	-	-	9	-	kΩ
VDIV_OUT(3)	Output Voltage Range	-	V_{SS}	-	V_{DD}	V
$I_{operating}$	Operating Power Consumption	V_{DD}=5V	255.2	676.1	883.5	μA

(1). Design guaranteed.

(2). VDIV operates without a buffer.

(3). Rail-to-rail output.

5.2.22 Temperature Sensor (TS) Characteristics

Table 5-28 TS Characteristics

Symbol	Parameter	Conditions	Minimum	Typical Value	Maximum	Unit
T_L	Temperature Sensor Linearity Error	-40°C~105°C	-	-	±8	°C
V_{20}	Output Voltage	20°C	378.73	413.14	436.10	mV
Avg_Slope	Temperature Sensor Slope	-	-	1.1762	-	mV/°C

5.2.23 Voltage Comparator (CMP) Characteristics

Table 5-29 CMP Characteristics

Symbol	Description	Conditions	Minimum	Typical Value	Maximum	Unit
V_{DD}(1)	Analog Supply Voltage	-	2.2	5	5.5	V
V_{com}(1)	Input Common-Mode Voltage	-	0.2	-	V_{DD}-0.2	V

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Symbol	Description	Conditions	Minimum	Typical Value	Maximum	Unit
V_{diff}(1)	Input Differential Voltage	V_{DDA}=5V, V_{com}=2.5V No Hysteresis	5	-	-	mV
V_{hy}(1)	Hysteresis Voltage	Threshold 1	-	0	-	mV
		Threshold 2	-	10	-	
		Threshold 3	-	30	-	
		Threshold 4	-	60	-	
I_{OP}(1)	Quiescent Operating Current	V_{DD} =5V	97.82	142.90	158.20	μA
T_{dly}(1)	Output Delay	Rising Edge	12.00	15.20	31.34	ns
		Falling Edge	16.62	29.58	44.11	

(1) Design guarantee.

5.2.24 Operational Amplifier (PGA) Characteristics

Table 5-30 PGA Characteristics

Symbol	Description	Conditions	Minimum	Typical Value	Maximum	Unit
V_{DD}(1)	Analog Supply Voltage	-	2.2	5	5.5	V
V_{OUT}	Output Voltage	-	V_{SS}	-	V_{DD}	V
C_{MIR}(1)	Input Common-Mode Voltage	-	0	-	5.5	V
I_{bias}(1)	Input Bias Current	-	0.8	1	1.2	μA
I_{load}	Output Current	RL=100Ω, V_{DD} =5V	-	10	-	mA
I_q	Operating Current	No Load, Quiescent Mode	780	970	1100	μA
I_l(1)	Leakage Current	Amplifier Disabled	480	700	1780	nA
V_{OS}	Input Offset Voltage	Before Calibration	-	±50	-	mV
		After Calibration, VIP=0.5* V_{DD}	-	0.638	-	
		After Calibration, VIP=0.2V	-	2.29	-	
CMRR(1)	Common-Mode Rejection Ratio	-	51	-	145	dB
PSRR_min(1)	Power Supply Rejection Ratio	Buffer Mode	-95.28	-64.89	-51.60	dB
		Single-Ended Gain ×4	-52.43	-47.52	-31.99	
		Single-Ended Gain ×8	-28.31	-40.82	-70.61	

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Symbol	Description	Conditions	Minimum	Typical Value	Maximum	Unit
		Single-Ended Gain ×12	-60.04	-37.17	-24.78	
		Single-Ended Gain ×20	-59.98	-32.77	-20.44	
		Single-Ended Gain ×40	-49.88	-27.13	-15.73	
		Differential Gain ×4	-75.84	-46.59	-35.66	
		Differential Gain ×8	-73.15	-40.49	-27.98	
		Differential Gain ×12	-71.49	-37.01	-24.45	
		Differential Gain ×20	-68.98	-32.69	-20.08	
		Differential Gain ×40	-65.08	-26.97	-14.72	
PSRR_max(1)	Power Supply Rejection Ratio	Buffer Mode	-3.83	-2.86	-1.79	dB
		Single-Ended Gain ×4	-1.78	-1.28	-0.89	
		Single-Ended Gain ×8	-2.67	-2.49	-2.05	
		Single-Ended Gain ×12	-3.08	-2.80	-2.57	
		Single-Ended Gain ×20	-3.31	-3.08	-2.80	
		Single-Ended Gain ×40	-3.40	-3.15	-2.92	
		Differential Gain ×4	-2.16	-1.65	-0.91	
		Differential Gain ×8	-3.49	-3.17	-2.84	
		Differential Gain ×12	-3.82	-3.59	-3.38	
		Differential Gain ×20	-3.87	-3.67	-3.48	
		Differential Gain ×40	-3.70	-3.50	-3.28	
GBW	Bandwidth	Single-Ended Gain ×1	8.2710	24.5400	41.7400	MHz
		Single-Ended Gain ×4	3.1170	4.4770	6.2090	
		Single-Ended Gain ×8	1.6840	2.4690	3.4800	
		Single-Ended Gain ×12	1.1390	1.6720	2.3690	
		Single-Ended Gain ×20	0.6963	1.0190	1.4460	
		Single-Ended Gain ×40	0.3647	0.5297	0.7505	
		Differential Gain ×4	3.1560	4.5500	6.3330	

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Symbol	Description	Conditions	Minimum	Typical Value	Maximum	Unit
		Differential Gain ×8	1.6890	2.4750	3.4930	
		Differential Gain ×12	1.1420	1.6720	2.3710	
		Differential Gain ×20	0.6992	1.0190	1.4460	
		Differential Gain ×40	0.37	0.53	0.75	
SR_rise	Positive Slew Rate	Gain=1	14.29	15.85	17.62	V/μs
		Gain=4	17.73	18.11	22.15	
		Gain=8	9.27	18.79	24.49	
		Gain=12	5.87	14.31	19.93	
		Gain=20	3.43	9.15	13.79	
		Gain=40	1.69	4.67	7.16	
SR_fall	Negative Slew Rate	Gain=1	14.54	17.08	19.85	V/μs
		Gain=4	14.82	17.48	20.02	
		Gain=8	9.15	15.98	19.53	
		Gain=12	6.05	13.25	17.21	
		Gain=20	3.52	9.35	13.38	
		Gain=40	1.77	4.85	7.50	
φ	Phase Margin	Buffer Mode	44.90	64.28	87.58	Deg
		Single-Ended Gain ×4	56.07	61.68	65.30	
		Single-Ended Gain ×8	75.78	78.97	80.75	
		Single-Ended Gain ×12	82.17	84.09	84.99	
		Single-Ended Gain ×20	86.15	87.23	87.63	
		Single-Ended Gain ×40	88.01	88.84	89.14	
		Differential Gain ×4	55.54	61.54	65.38	
		Differential Gain ×8	75.95	78.86	80.62	
		Differential Gain ×12	82.25	83.98	84.86	
		Differential Gain ×20	86.17	87.13	87.55	
		Differential Gain ×40	87.98	88.76	89.14	
PGA gain	PGA Closed-Loop Gain	Buffer Mode	-	0.99	-	times

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Symbol	Description	Conditions	Minimum	Typical Value	Maximum	Unit
		Single-Ended Gain ×4	-	3.90	-	
		Single-Ended Gain ×8	-	7.72	-	
		Single-Ended Gain ×12	-	11.47	-	
		Single-Ended Gain ×20	-	18.74	-	
		Single-Ended Gain ×40	-	35.83	-	
		Differential Gain ×4	-	3.20	-	
		Differential Gain ×8	-	7.16	-	
		Differential Gain ×12	-	10.78	-	
		Differential Gain ×20	-	18.4	-	
		Differential Gain ×40	-	35.67	-	

(1). Design guarantee.

PGA Differential Gain Derivation Diagram and Table

Derivation Process:

A_PGA_O = (((VREF/2 - A_VP) * VREF_GAIN + A_VP) - A_VN) * PGA_GAIN + A_VN

Set A_PGA_O = VREF/2 (when A_VP = A_VN = 0):

VREF/2 = VREF/2 * VREF_GAIN * PGA_GAIN

Thus: PGA_GAIN = 1 / VREF_GAIN

Simplified: A_PGA_O = VREF/2 + (PGA_GAIN - 1) * (A_VP - A_VN)

REAL_GAIN = PGA_GAIN - 1

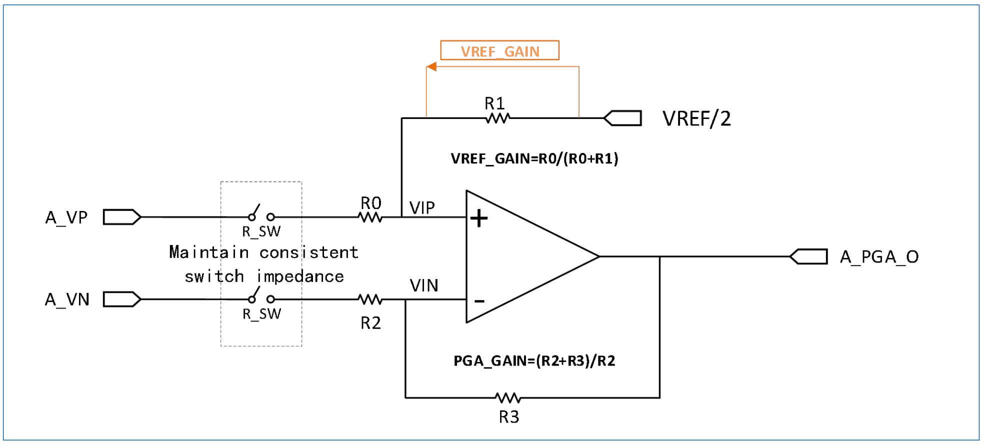

Figure 5-4 PGA Differential Gain Derivation Diagram

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Table 5-31 PGA Internal Resistor Design Characteristics

PGA_GAIN Setting (Multiple)	R0+R_SW (kΩ)	R1 (kΩ)	VREF_GAIN (Multiple)	R2+R_SW (kΩ)	R3 (kΩ)	Actual Single-Ended Gain
4	32.05	95.25	0.2517	32.05	95.25	3.972
8	16.18	111.1	0.1271	16.17	111.1	7.870
12	10.88	116.4	0.0854	10.88	116.4	11.70
20	6.650	120.7	0.0522	6.650	120.7	19.14
40	3.475	123.8	0.0273	3.475	123.8	36.63

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6 Typical Circuits

6.1 Power Supply

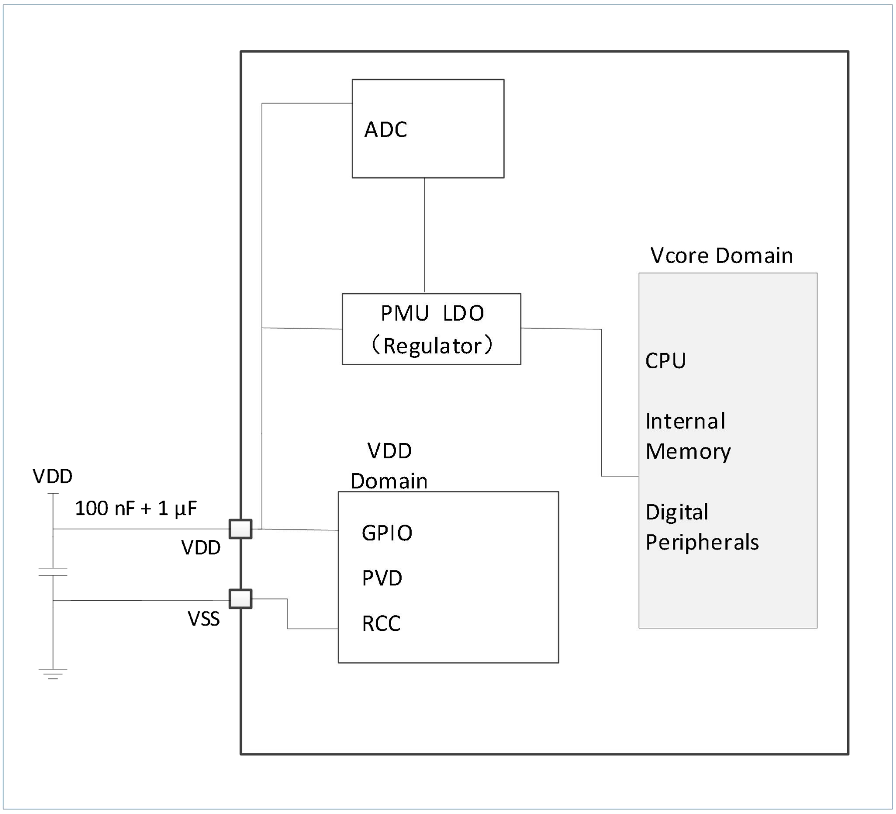

Figure 6-1 Power Supply Block Diagram

6.2 Typical Application Circuit

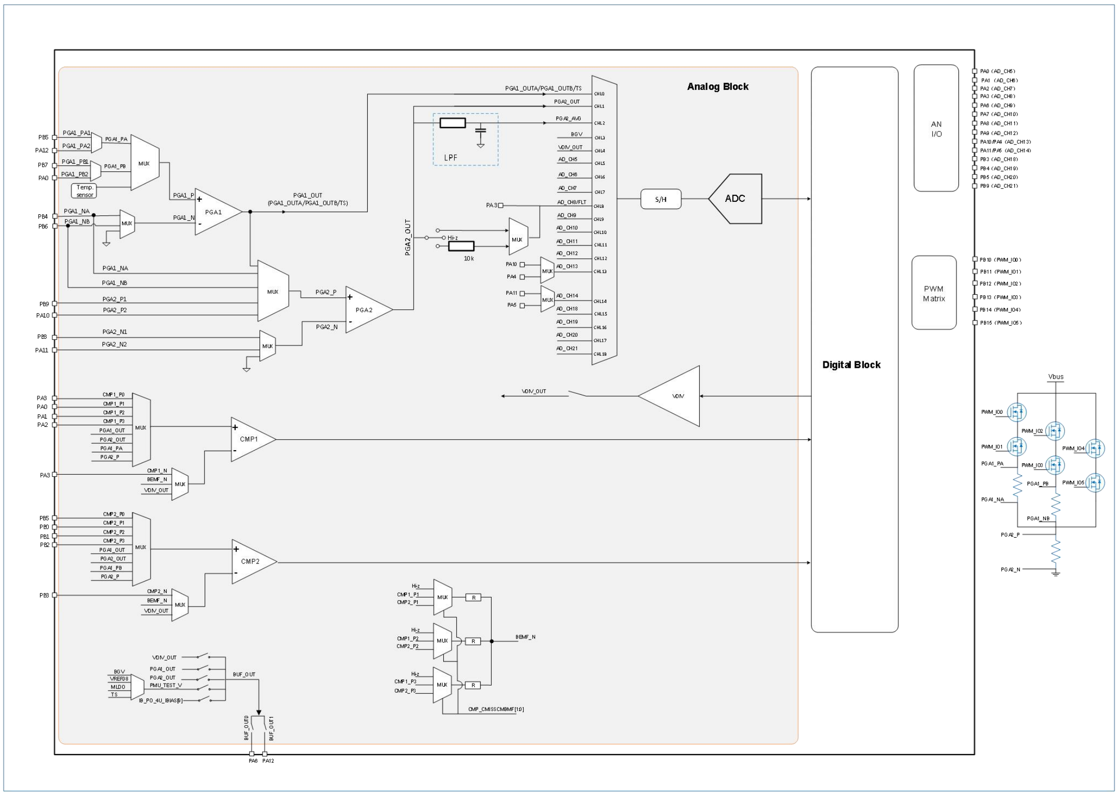

Figure 6-2 Typical Application Circuit

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7 Pin Definition

PM10225A MCU uses QFN3X3-20 package, with the following pin definitions.

7.1 QFN3X3-20 Package

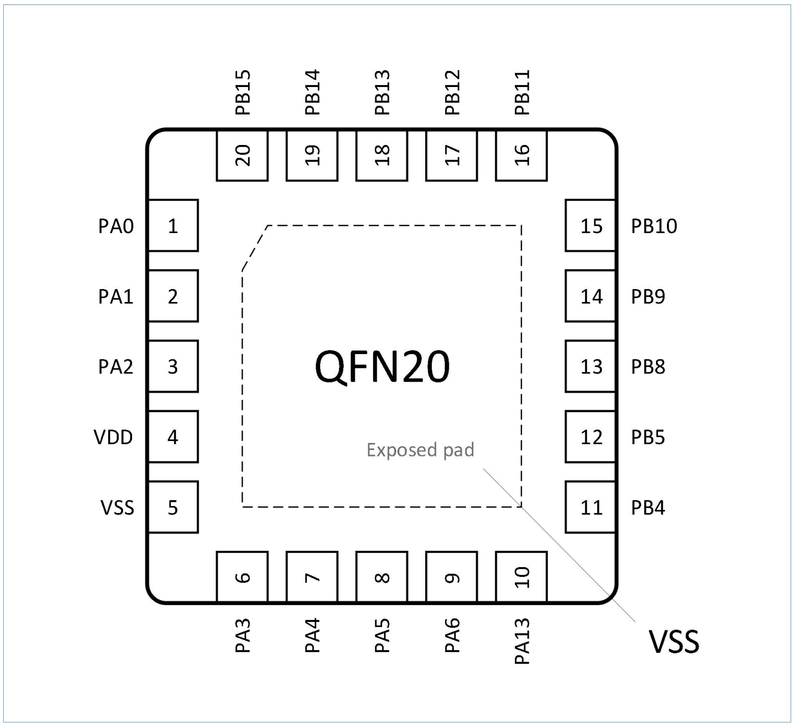

Figure 7-1 QFN3X3-20 Package

7.2 Pin Definition

Table 7-1 Pin Definition

QFN3X3-20	Pin Name (Default Function After Reset)	Pin Type[(1)]	Pin Alternate Function[(2)]	Pin Additional Functions
0	VSS	S	Digital Ground (Pin 0 is the thermal pad on the bottom of the QFN3X3-20 package)	
1	PA0	I/O	RCC_CLK1 Hall_A UART1_TX[(3)]	AD_CH5 CMP1_P1 PGA1_PB2
2	PA1	I/O	RCC_MCO UTIOU1B Hall_B UART1_RX	AD_CH6 CMP1_P2
3	PA2	I/O	UBKI1 Hall_C ADC_IP_TEST_LV	AD_CH7 CMP1_P3
4	VDD	S	Digital Power Supply	
5	VSS	S	Ground	
6	PA3	I/O	ATU_BKIN0 UBKI2 ADC_Trigo	AD_CH8 CMP1_N CMP1_P0

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QFN3X3-20	Pin Name (Default Function After Reset)	Pin Type(1)	Pin Alternate Function(2)	Pin Additional Functions
7	PA4 (SWCLK)	I/O	SWCLK UTIOU1A UART2_TX I2C1_SCL PWM_DIR	AD_CH13
8	PA5 (SWDIO)	I/O	RCC_MCO SWDIO UTIOU2A UART2_RX I2C1_SDA	AD_CH14
9	PA6	I/O	UTIOU1B UART2_RX I2C1_SCL CMP1_Out	AD_CH9 BUF_OUT0
-	PA7	I/O	UTIOU1A UART2_TX I2C1_SDA CMP2_Out	AD_CH10
-	PA8	I/O	ATU_BKIN0 UART2_RX SPI1_MISO	AD_CH11
-	PA9	I/O	ATU_BKIN1 UART1_TX SPI1_MOSI	AD_CH12
-	PA10	I/O	SPI1_CLK	AD_CH13 PGA2_P2
-	PA11	I/O	UBKI1 ADC_Trigo	AD_CH14 PGA2_N2
-	PA12	I/O	UTIOU2A CMP1_Out	PGA1_PA2 BUF_OUT1
10	PA13(NRST)	I/O	UTIOU2B UART1_TX ADC_Trigo	NRST
-	PB0	I/O	ATU_BKIN0 Hall_A UART2_TX ADC_Trigo	CMP2_P1
-	PB1	I/O	ATU_BKIN1 Hall_B UART2_RX	CMP2_P2
-	PB2	I/O	UBKI2 Hall_C I2C1_SDA	CMP2_P3
-	PB3	I/O	I2C1_SCL SPI1_CS PWM_DIR	AD_CH18 CMP2_N

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QFN3X3-20	Pin Name (Default Function After Reset)	Pin Type[(1)]	Pin Alternate Function[(2)]	Pin Additional Functions
11	PB4	I/O	RCC_MCO ATU_BKIN1 UTIOU2A I2C1_SDA SPI1_MOSI	AD_CH19 PGA1_NA
12	PB5	I/O	ATU_BKIN0 UTIOU2B I2C1_SCL SPI1_MISO	AD_CH20 CMP2_P0 PGA1_PA1
-	PB6	I/O	UTIOU1A SPI1_MOSI	PGA1_NB
-	PB7	I/O	UTIOU1B SPI1_MISO	PGA1_PB1
13	PB8	I/O	UBKI2 SPI1_CS	PGA2_N1
14	PB9	I/O	SPI1_CLK	AD_CH21 PGA2_P1
15	PB10	I/O	PWM_IO0 UTIOU2A	-
16	PB11	I/O	PWM_IO1 UTIOU2B	-
17	PB12	I/O	PWM_IO2 UART1_RX SPI1_MOSI	-
18	PB13	I/O	PWM_IO3 UART1_TX SPI1_MISO	-
19	PB14	I/O	PWM_IO4 UART2_RX SPI1_CS	-
20	PB15	I/O	RCC_CLK2 PWM_IO5 UART2_TX SPI1_CLK	-

(1). "I" represents input, "O" represents output, "I/O" represents input/output, "S" represents power supply.

(2). For pin alternate functions, please refer to "7- 2 Pin Multiplexing Function Table".

(3). Both UART1 and UART2 support swapping the TX and RX pin functions.

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7.3 Pin Multiplexing (AF) Function Table

Table 7-2 Pin Multiplexing Function Table

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	Hall_A	-	UART1_TX(1)	-	-	-	RCC_CLK1
PA1	-	Hall_B	UTIOU1B	UART1_RX	-	-	-	RCC_MCO
PA2	-	Hall_C	UBKI1	-	-	-	-	-
PA3	ATU_BKIN0	-	UBKI2	-	-	-	-	ADC_Trigo
PA4	SWCLK	-	UTIOU1A	UART2_TX	I2C1_SCL	-	-	PWM_DIR
PA5	SWDIO	-	UTIOU2A	UART2_RX	I2C1_SDA	-	-	RCC_MCO
PA6	-	-	UTIOU1B	UART2_RX	I2C1_SCL	-	-	CMP1_Out
PA7	-	-	UTIOU1A	UART2_TX	I2C1_SDA	-	-	CMP2_Out
PA8	ATU_BKIN0	-	-	UART2_RX	-	SPI1_MISO	-	
PA9	ATU_BKIN1	-	-	UART1_TX	-	SPI1_MOSI	-	
PA10	-	-	-	-	-	SPI1_CLK	-	-
PA11	-	-	UBKI1	-	-	-	-	ADC_Trigo
PA12	-	-	UTIOU2A	-	-	-	-	CMP1_Out
PA13	-	-	UTIOU2B	UART1_TX	-	-	-	ADC_Trigo
PB0	ATU_BKIN0	Hall_A	-	UART2_TX	-	-	-	ADC_Trigo
PB1	ATU_BKIN1	Hall_B	-	UART2_RX	-	-	-	-
PB2	-	Hall_C	UBKI2	-	I2C1_SDA	-	-	-
PB3	-	-	-	-	I2C1_SCL	SPI1_CS	-	PWM_DIR
PB4	ATU_BKIN0	-	UTIOU2A	-	I2C1_SDA	SPI1_MOSI	-	RCC_MCO
PB5	ATU_BKIN1	-	UTIOU2B	-	I2C1_SCL	SPI1_MISO	-	-
PB6	-	-	UTIOU1A	-	-	SPI1_MOSI	-	-
PB7	-	-	UTIOU1B	-	-	SPI1_MISO	-	-
PB8	-	-	UBKI2		-	SPI1_CS	-	-
PB9	-	-	-		-	SPI1_CLK	-	-
PB10	PWM_IO0	-	UTIOU2A		-	-	-	-
PB11	PWM_IO1	-	UTIOU2B		-	-	-	-
PB12	PWM_IO2	-	-	UART1_RX	-	SPI1_MOSI	-	-
PB13	PWM_IO3	-	-	UART1_TX	-	SPI1_MISO	-	-
PB14	PWM_IO4	-	-	UART2_RX	-	SPI1_CS	-	-
PB15	PWM_IO5	-	-	UART2_TX	-	SPI1_CLK	-	RCC_CLK2

(1). The table above indicates that both UART1 and UART2 support TX and RX pin function swapping.

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8 Package Parameter

8.1 Package Size-QFN3X3-20 Package

The QFN3X3-20 package measures 3.0 mm × 3.0 mm with a 0.40 mm pitch.

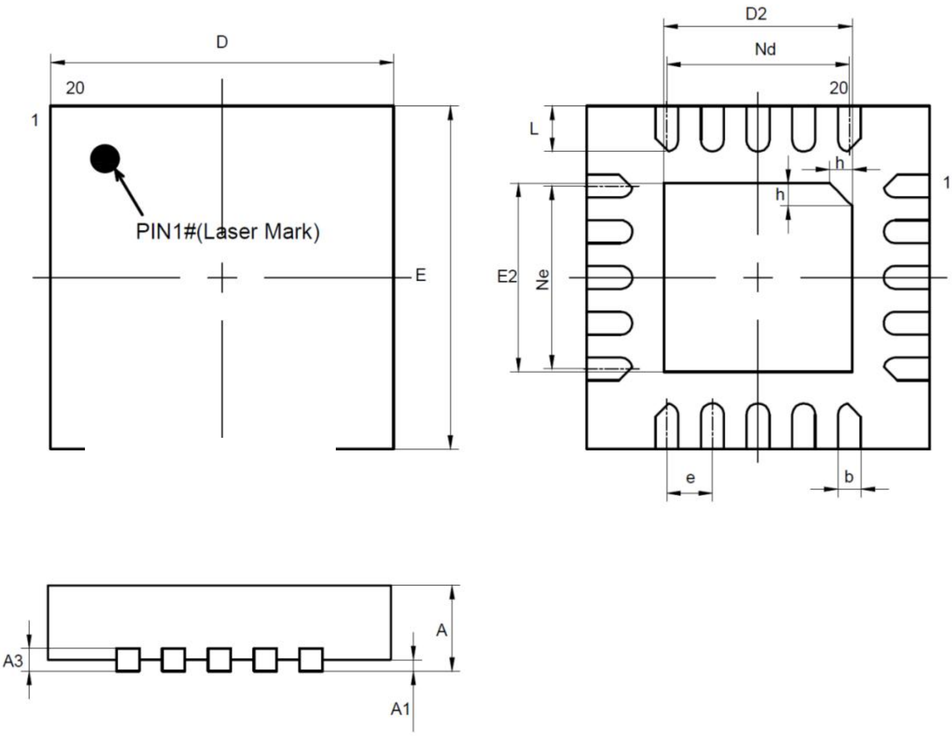

Figure 8-1 QFN3X3-20 Package Size

Table 8-1 QFN3X3-20 Package Size Parameter

Symbol	Minimum(mm)	Typical Value(mm)	Maximum(mm)
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
D	2.90	3.00	3.10
E	2.90	3.00	3.10
D2	1.60	1.65	1.70
E2	1.60	1.65	1.70
e	0.40		
h	0.25 REF		
L	0.35	0.40	0.45

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9 Acronyms and Terminology

9.1 Acronyms

Acronyms	Full Name
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
GPIO	General Purpose Input Output
HSI	High-Speed Internal(Clock Signal)
IAP	In-Application Programming
ICP	In Circuit Programming
LSI	Low-Speed Internal(Clock Signal)
MCU	Microcontroller Unit
OBL	Option Byte Loader
SWD	Serial Wire Debug

9.2 Terminology

Name	Description
Byte	8-bit data length.
Half word	16-bit data or instruction length.
Option byte	MCU configuration bytes stored in Flash.
Word	32-bit data or instruction length.

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10 Version History

Version	Date	Changes
Rev.1.0	2026-04-02	Initial release

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