PM30225Q-0405 Datasheet

40V , 5A , High Density All in One Motor Driver

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1 Introduction

This document serves as the data sheet for the PM30225Q-0405 chip.

Users may consult the PM30225Q-0405 User Manual for further details regarding the functionality of this chip series.

2 Product Description

The PM30225Q-0405 series is a dedicated motor driver chip utilising the ARM® Cortex®-M0 core, operating at a maximum frequency of 64MHz, with integrated 32Kbyte Flash and 4Kbyte SRAM.

The PM30225Q-0405 incorporates one 16-bit advanced timer, one 32-bit general-purpose timer, one 16-bit general-purpose timer, and one 24-bit Hall sensor dedicated timer.

The integrated analog circuit includes: one 12-bit ADC (supporting 14 external analog input channels and 6 internal input channels), two programmable operational amplifiers (with PGA1 supporting dual-phase current polling amplify), two voltage comparators (incorporating BEMF neutral point real-time detection),one power-on/power-down reset circuit (POR/PDR), one Programmable Voltage Detector/Brown-Out Reset circuit (PVD/BOR), one internal temperature sensor, one internal reference voltage (sampled via the on-chip ADC), and an internal analog power supply circuit delivering 2.4V/3.6V outputs.

All pins on the PM30225Q-0405, except power supply and ground, can function as GPIO, peripheral I/O, or external interrupt inputs.

The PM30225Q-0405 supports conventional Flash read/write protection.

The PM30225Q-0405 supports multiple communication interfaces: 2 serial UARTs and 1 I²C.

The PM30225Q-0405 further integrates a hardware division-square root unit (DVSQ) to enhance software processing capabilities and rapid response to external events.

The PM30225Q-0405 supports low-power Sleep and Stop modes, making it suitable for applications demanding high chip power efficiency.

The PM30225Q-0405 incorporates a three-phase brushless gate driver capable of operating up to 36V, designed to drive P+N structure MOSFETs.

It integrates three half-bridge P+N MOSFETs supporting low RDS(ON) values.

Operating within a temperature range of -40°C to +105°C and a supply voltage of 5V to 24V, the PM30225Q-0405 meets the requirements of most application environments.

With these extensive peripherals, the PM30225Q-0405 is particularly well-suited for square wave/FOC drive control applications in BLDC/PMSM motors:

- **Cooker hoods**
- **Water pumps**
- **Ceiling fans**
- **Pedestal fans**
- **Air fryers**
- **Electric ovens**
- **Cooling fans**

2.1 Product Features

- **CPU Core**
  - **ARM® Cortex®-M0**
  - **Maximum clock frequency：64 MHz**
  - **24-bit SysTick Timer**
- **Operating Voltage Range**
  - **5V ~ 24 V**
- **Operating Temperature Range**
  - **-40°C ~ +105°C**
- **Memory**

- **32 Kbyte Flash**
  - Supports zero-wait-cycle access to Flash when CPU clock frequency does not exceed 24 MHz.
  - Flash incorporates data security protection, enabling separate configuration of read and write protection.
- **4 Kbyte SRAM**

Clock

- **On-chip high-speed clock HSI:8/64 MHz**
- **On-chip slow clock LSI:40 kHz**
- **GPIO external input clock:≤32MHz**

Reset

- **External pin reset (NRST pin)**
- **Option byte loader reset**
- **Window watchdog timer termination (WWDG reset)**
- **Independent watchdog timer termination (IWDG reset)**
- **Power-on reset (POR/PDR/BOR)**
- **Software reset (SW reset)**

GPIO port

- **Support up to 14 GPIO ports**

Data communication interface

- **2 UART channels**
  - Supports LIN mode.
- **1 I^2C channel**
  - 1MHz / 400kHz / 100kHz transmission modes

Timers

- **1 x 16-bit Advanced Timer for Motor Applications (ATU)**
  - 3 complementary PWM outputs, each with asymmetrical pre- and post-dead time
  - Supports 6 independent PWM outputs
  - Supports external pin signal braking and internal comparator output signal braking
  - Supports two independent trigger signals for ADC synchronous sampling
  - Supports ADC dual-group sampling mode triggering
- **2 General-purpose timers (UTU1: 32-bit, UTU2: 16-bit)**
  - Supports 2 independent PWM output modes
  - Supports 1 complementary PWM output mode
  - Supports single-trigger activation of ATU or another UTU
  - Supports periodic triggering of ADC sampling
- **1 24-bit Hall timer (HTU)**
  - Supports three Hall signal inputs
  - Hall sequence detection
  - Phase-shift averaging timing function supports 2/4/8 phase-shift averaging
  - HTU and comparator CMP linked counting

Division and Square Root Unit (DVSQ)

- **Supports 32-bit fixed-point division, simultaneously yielding quotient and remainder**
- **Supports 32-bit fixed-point high-precision square root**

On-chip analog circuit

- **1 x 12-bit SAR ADC (Up to 14 external analog input channels, corresponding to 16 external pins)**
  - 12-bit resolution

- Maximum conversion rate: 2.285 MSPS
- ADC features programmable sampling time; sampling time can be configured independently per channel.
- Conversion data support left-aligned and right-aligned formats.
- Supports internal analog circuit sampling (PGA1_OUTA, PGA1_OUTB, PGA2_OUT, VDIV_OUT, internal temperature sensor, internal reference voltage).
- Supports two sample groups (channels customizable per group).
- Supports software trigger and multiple hardware trigger sources (ATU's TRG0 & TRG1, UTU1/2, CMP, etc.).
- Supports analog window comparator function.
- Sample groups have independent channel data result registers.
- Supports oversampling and averaging function.
- VREFP internal supply voltage options: Selectable from 2.4V, 3.6V, or VDDA as the ADC reference voltage.

Internal Reference Voltage VREFINT (i.e., BGV)

- Internal reference voltage output is connected to a dedicated ADC channel.

2 x Voltage Comparators

- Comparator reference voltage can be from external signal input or from the internal voltage divider (VDIV).
- Comparator output can be used as a brake source for the Advanced Timer (ATU).
- Supports BEMF internal neutral point detection.
- Supports blanking function via PWM blanking signal from ATU.

2 x Programmable Operational Amplifiers

- Programmable gain (x1, x4, x8, x12, x20, x40).
- Supports built-in bias voltage for positive (P) input.
- PGA1 supports two sets of input signal polling amplification.
- Amplifier output is directly connected to ADC for sampling.

5V LDO Circuit

- **Supports 50 mA output current**
- **Integrated output short-circuit protection**

Three-Phase Brushless Gate Driver

- **Integrated dead time: 50 ns (typ.)**
- **Integrated over-temperature protection function**

MOSFET

- **N-channel: VDS = 24V, ID = 5A**
- **P-Channel: VDS = -24V, ID = -5A**

96-bit UID

- **Used as a serial number and security key**
- **Activates secure boot process**

CPU Tracing and Debugging

- **SWD debugging interface**
- **ARM® Core Sight™ Debug Components (ROM-Table, DWT, BPU)**
- **Custom DBGMCU debug controller (low-power mode simulation control, debug peripheral clock control, debug and trace interface allocation)**

Meet AEC-Q100 requirements

2.2 Device Overview

Table 2- 1 PM30225Q-0405 Series Feature

Product Feature		PM30225Q-0405
GPIO		14
Package		TSSOP-25
working voltage		5V ~ 24 V
working temperature		-40°C~+105°C
Memory	Flash (Kbyte)	32
	SRAM (Kbyte)	4
CPU	kernel	Cortex®-M0
	working frequency	64MHz
DVSQ		1
Clock	Internal LSI	40 kHz
	Internal HSI	8 MHz /64 MHz
	External GPIO clock	0~32MHz
Timer	General-Purpose Timer (UTU)	1 (32-bit) : UTU1 1 (16-bit) : UTU2
	Hall Timer (HTU)	1 (24-bit)
	System Tick Timer	1
	Independent Watchdog (IWDG)	1
	Window Watchdog (WWDG)	1
Communication Interface	UART	2
	I^2C	1
ADC	Number of ADCs and external channels	1(9+4)
	VREFP Internal Supply Voltage	VDDA / 2.4V Vref / 3.6V Vref Selectable
	Reference Selection	Internal Reference Voltage VREFINT
	ADC Conversion Rate	2.285MSPS（ADC_CLK=32MHz）
	ADC accuracy	12-bit
Voltage Comparator (CMP)		2
Programmable Operational Amplifier (PGA)		2
96-bit UID		1

3 Ordering Information

3.1 Ordering Information

Table 3-1 PM30225Q-0405 Product Ordering Information

Order number	Marking ID	Package	Operating Voltage Range	Description
PM30225Q-0405B	PM30225Q 0405BYMDNN	TSSOP-25	5V ~ 24 V	Halogen free RoHS compliant in T/R, 2,500 pcs/Reel

3.2 Marking Information

Table 3-2 PM30225Q-0405 Product Marking Information

Marking	Package	Definition
PM30225Q 0405BYMDNN	TSSOP-25	Product code : PM30225Q Voltage/Current/Package code : 0405B Y : Year code M : Month code D : Day code NN: Serial Number

4 Function Introduction

4.1 Block Diagram

The device incorporates 32Kbyte of internal Flash memory for storing programmes and data.

The ARM® Cortex®-M0 processor is an embedded 32-bit RISC processor delivering outstanding computational performance and advanced interrupt system responsiveness. The Cortex®-M0 core integrated within this product family is fully compatible with all ARM tools and software.

The system architecture of the PM30225Q-0405 MCU is illustrated in Figure 4-1.

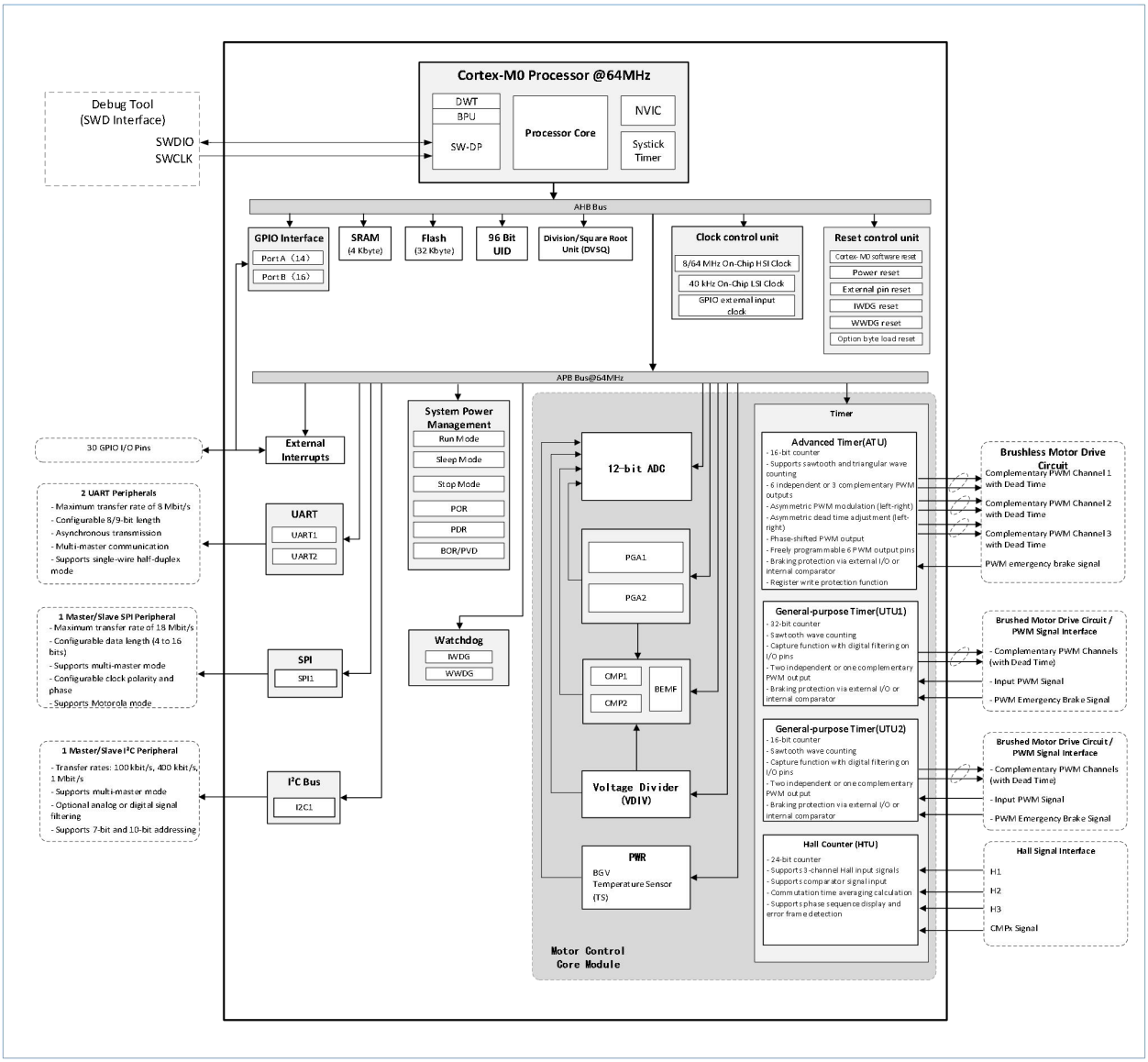


Figure 4- 1 PM30225Q-0405 Block Diagram

4.2 System Block Diagram

PM30225Q-0405 is a highly integrated chip that internally integrates an MCU, Driver, 5V LDO, and three sets of P+N MOS. The system block diagram illustrates the internal resources and connections of PM30225Q-0405.

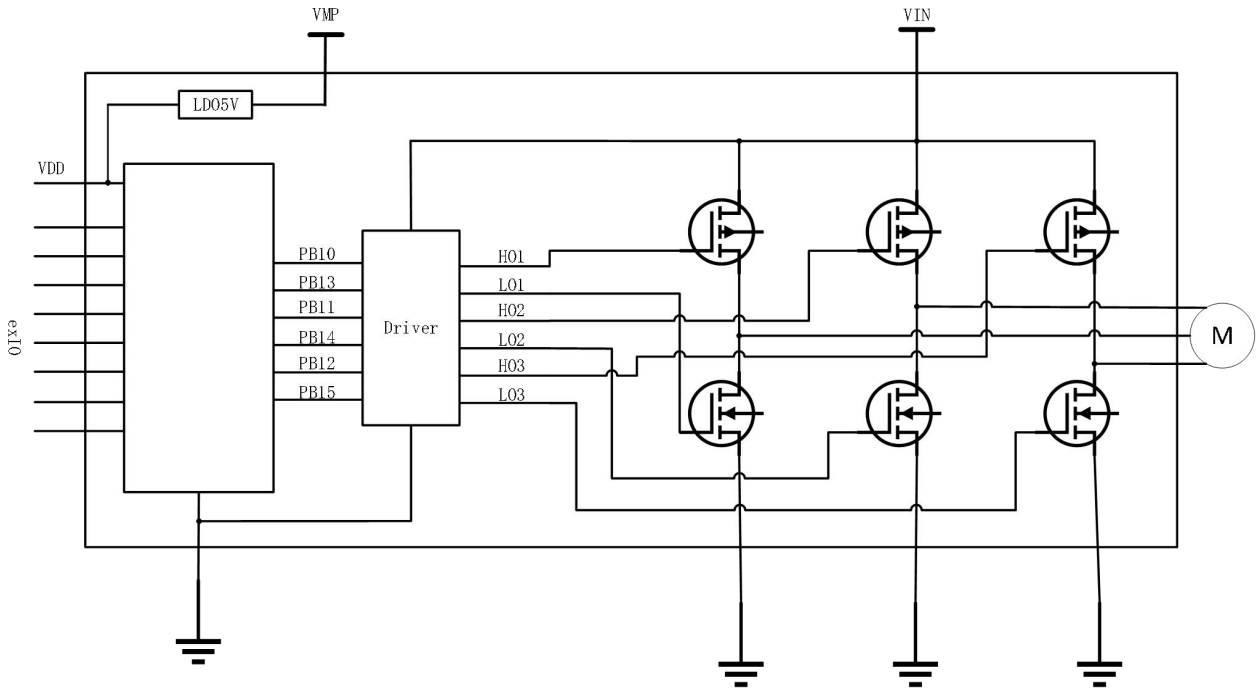


Figure 4-2 PM30225Q-0405 System Block Diagram

4.3 Memory Mapping Configuration

The memory map of the PM30225Q-0405 MCU is illustrated in the following figure:

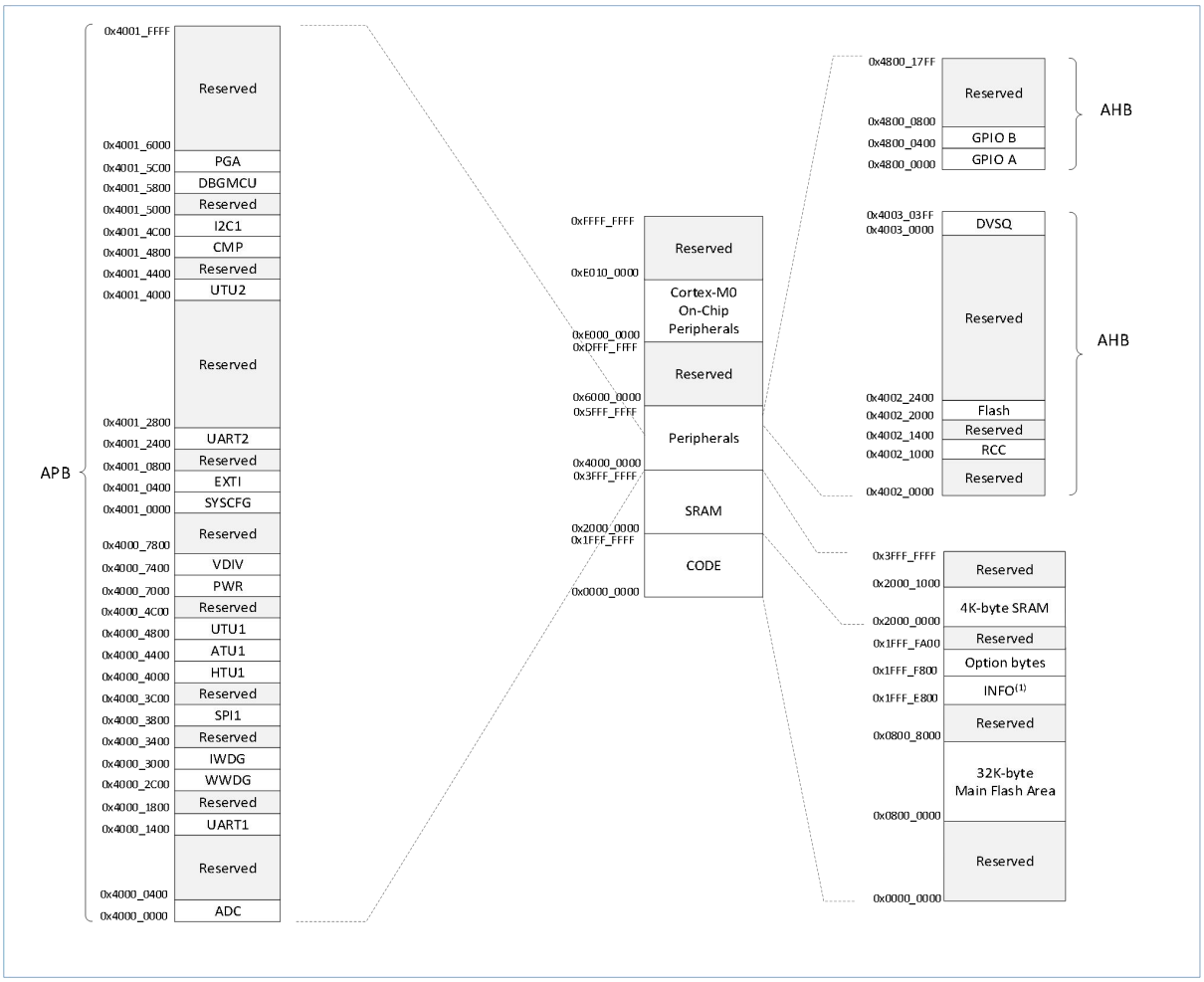


Figure 4- 3 PM30225Q-0405 Memory Map

(1). It is recommended that users employ the INFO (Information) section to store parameters within the application.

4.4 Memory

4.4.1 Flash

Flash Memory Composition:

- **32 Kbyte Main Flash Block: Used for storing programs and data.**
- **4 Kbyte Information Block (INFO): It is recommended for users to utilize the INFO area for storing application parameters.**
- **Option Bytes**

4.4.2 SRAM

The devices of this series integrate 4 Kbyte of SRAM internally, supporting word, halfword, and byte read/write access. The CPU can perform fast read and write operations with zero wait cycles, which can meet the requirements of most applications.

4.5 Power Supply Plan

The PM30225Q-0405 has three power supply groups: VIN, VMP, and LDO5V. VIN provides an input of 5–24V to power the internal MOSFETs and driver of the chip. VIN, through a series resistor, powers VMP and outputs 5V to the LDO5V pin. LDO5V is internally connected to V_{DD}/V_{DDA} to supply power to the digital circuits, I/O pins, internal voltage regulators, ADC, voltage comparators, operational amplifiers, and other analog sections of the chip.

4.6 Power Monitor

The chip integrates a Power-On Reset (POR), Power-Down Reset (PDR), Programmable Voltage Detector (PVD), and Brown-Out Reset (BOR) circuit. The system becomes operational once the supply voltage reaches 2.2 V. When V_{DD}/V_{DDA} falls below the specified threshold voltage V_{POR}/V_{PDR}, the system is held in a reset state without requiring an external reset circuit.

During power-up, the Brown-Out Reset (BOR) holds the device in reset until the supply voltage reaches the specified V_{BOR} threshold. When BOR is disabled, the power supply is monitored by the POR/PDR circuits. The device also includes a Programmable Voltage Detector (PVD) that monitors the V_{DD}/V_{DDA} supply and compares it to a software-configurable threshold V_{PVD}. An interrupt is generated when V_{DD} drops below or rises above the V_{PVD} threshold, allowing the interrupt service routine to issue a warning message.

Notes：.

- The BOR and PVD functions are mutually exclusive and cannot be used simultaneously. The desired function must be enabled via software configuration.

4.7 Low power consumption mode

The device supports Sleep mode and Stop mode.

- **Sleep Mode**

Only the CPU is halted. All peripherals remain active and can wake up the CPU when an interrupt/event occurs.

- **Stop Mode**

The lowest power consumption is achieved in Stop mode while retaining the contents of SRAM and registers. In Stop mode, all clocks in the core domain are switched off. The MCU can be woken up from Stop mode by any signal configured as an EXTI source. The EXTI signal can originate from any one of the 16 external I/O ports.

4.8 Reset

4.8.1 System Reset

A system reset initializes all registers to their reset values, with the exception of the reset flags within the RCC_CSR register. The source of a reset event can be identified by checking the reset status flags located in the RCC_CSR control and status register.

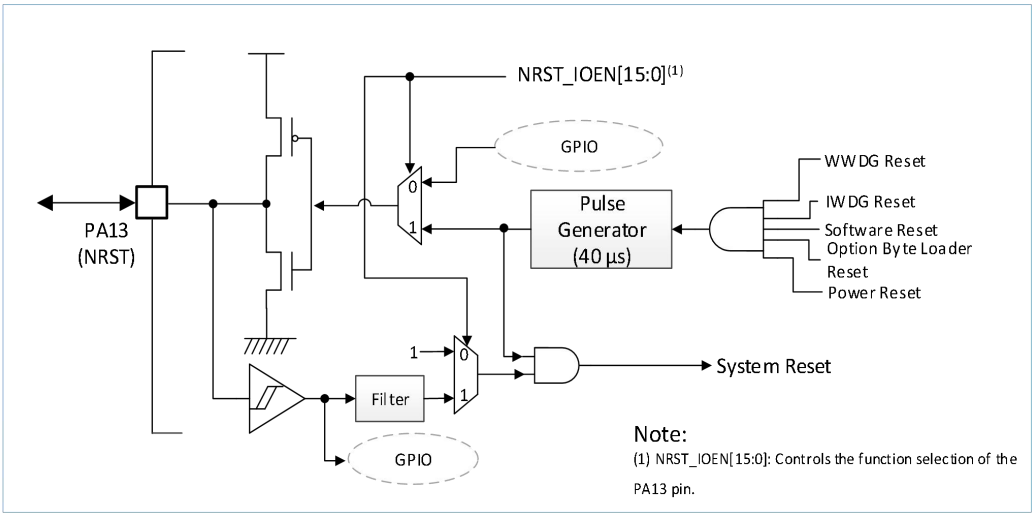


Figure 4-4 Reset Signal

When any of the following events occurs, a system reset will be generated:

- **A low level on the NRST pin (external reset)**
- **Option byte loader reset**

- **Window watchdog count termination (WWDG reset)**
- **Independent watchdog count termination (IWDG reset)**
- **Power reset (POR/PDR/BOR)**
- **Software reset (SW reset): A software reset is achieved by setting the SYSRESETREQ bit in the Cortex®-M0 Interrupt Application and Reset Control Register to '1'.**

All reset sources ultimately affect the NRST pin and hold it low during the reset process. The reset entry vector is fixed at address 0x0000 0004. The internal reset signal of the chip is output on the NRST pin.

The internal reset signal is output on the NRST pin. A pulse generator ensures that these (external or internal) reset sources generate a pulse with a minimum delay of 40 µs. When the NRST pin is pulled low to generate an external reset, it will generate a reset pulse.

4.8.2 Power reset

When any of the following events occurs, a power reset will occur:

- **Power-on/power-down reset POR/PDR**
- **Under-voltage reset BOR**

The chip integrates an internal Power-On Reset (POR)/Power-Down Reset (PDR) circuit. This circuit is always active to ensure proper system operation when the supply voltage exceeds 2.2V. When V_{DD} falls below the POR/PDR threshold, the MCU is held in reset without requiring an external reset circuit.

The chip also integrates an internal Brown-Out Reset (BOR) circuit. The BOR option is disabled by default, in which case the power supply is monitored by the POR/PDR circuits. Users can configure the MCU option bytes to enable or disable the BOR function.

4.9 Clock and clock tree

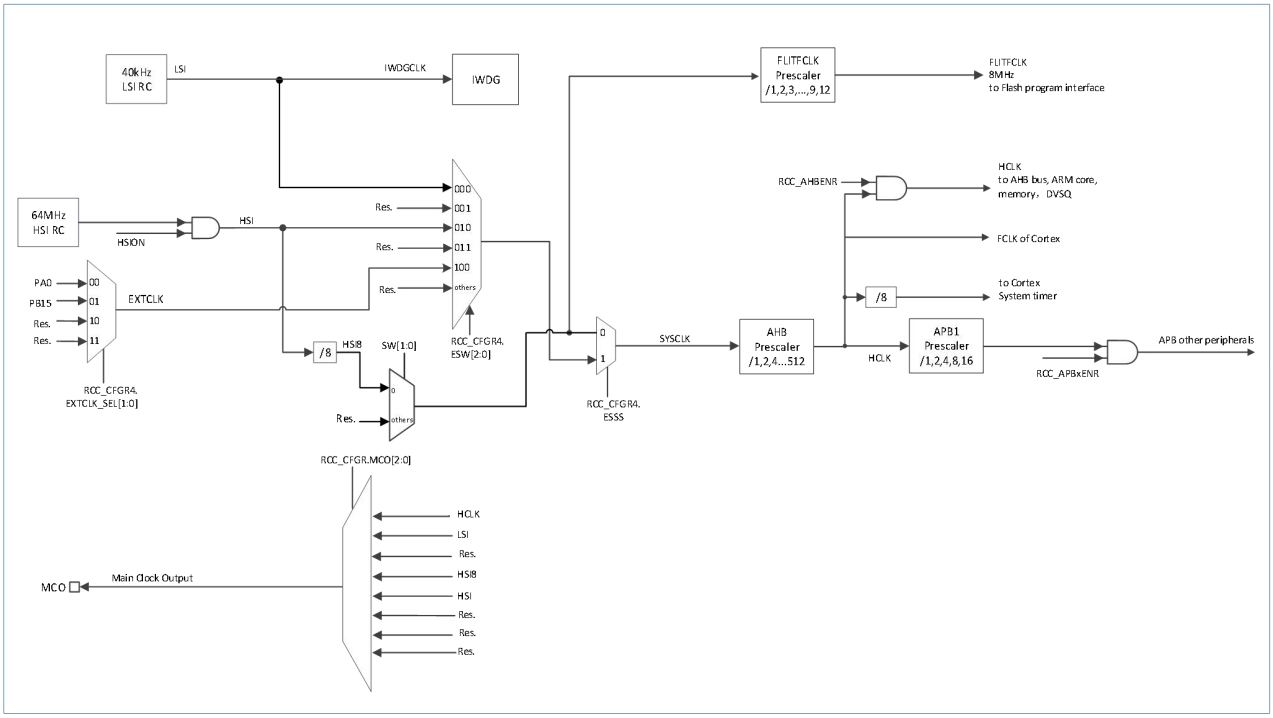


Figure 4- 5 PM30225Q-0405 Clock Tree

The device selects the system clock (SYSCLK) as the CPU operating clock during startup. The 64 MHz clock output from the internal oscillator is divided down to HSI8, which serves as the default system clock after power-on.

The device offers multiple clock sources for the system clock, providing customers with lightweight, flexible, and diverse operating modes. The following clocks can all be used as the system clock:

- **On-chip high-speed clock (HSI): 8 MHz / 64 MHz**

- **On-chip low-speed clock (LSI): 40 kHz**
- **GPIO external input clock: 0 ~ 32 MHz**

The clock frequencies for the AHB and APB domains can be configured via dividers. The maximum clock frequency for the AHB bus can reach 64 MHz. The maximum clock frequency for the APB domain can reach 64 MHz.

4.10 SYSCFG

The devices of this series feature a set of system configuration registers. The primary functions of the system configuration controller are as follows:

- **Remapping memory to the code start area.**
- **Managing external interrupts connected to GPIO pins.**
- **Controlling the switching of internal analog signals to output pins.**
- **Controlling the IO filtering function.**
- **The internal noise filter features an enable/disable function.**

4.11 GPIO

Each GPIO pin can be individually configured by software as an output (push-pull or open-drain), input (floating, pull-up, or pull-down), or as an alternate function for other peripherals. Most GPIO pins are shared with digital or analog peripherals. All GPIO pins are capable of sourcing/sinking high current. The peripheral function of an I/O pin can be locked via a specific locking mechanism to prevent spurious writes to the I/O registers. Each IO possesses a dedicated 32-bit port control register for configuring its functionality.

4.12 Interrupts and Events

4.12.1 NVIC

The Nested Vectored Interrupt Controller (NVIC) is closely coupled to the processor core, enabling low-latency interrupt processing and efficient handling of late-arriving interrupts. The NVIC manages interrupts, including core exceptions.

- **28 maskable interrupt channels (excluding the 16 Cortex®-M0 interrupt lines)**
- **4 programmable interrupt priority levels (utilizing 2 priority bits)**
- **Low-latency exception and interrupt handling**
- **Power management control**
- **Implementation of system control registers**

4.12.2 EXTI

The Extended Interrupt and Event Controller (EXTI) manages internal and external asynchronous interrupts and events: it generates event requests to the CPU, interrupt requests to the interrupt controller, and wake-up requests to the power management module.

Each EXTI line for interrupts or events can be individually masked or enabled.

- **Supports up to 18 event/interrupt requests**
  - **17 configurable EXTI lines (1)**
    - Trigger edge selectable (rising, falling, or both)
    - Dedicated interrupt status flag
    - Interrupt/event generation can be triggered by software
  - **1 non-configurable EXTI line (1)**
- **Each interrupt/event line can be individually triggered and masked.**
- **Capable of detecting external signals with pulse widths shorter than the APB clock period.**

Explain：

Configurable EXTI lines refer to lines whose interrupt/event trigger edges are configurable via EXTI registers.

Non-configurable EXTI lines refer to lines that do not support configuration via EXTI register bits.

4.13 Timer

The MCUs of this series include one Advanced-control Timer, two General-purpose Timers, and one Hall Timer. The timer functionalities are defined in the table below.

Table 4-1 Timer Function Definition

Type	Timer Name	Counter Resolution	Counter Type	Prescaler Factor	DMA Request	Emergency Brake Input	Hall Input	Capture/ Compare Channel	Complementary Output
Advanced Timer	ATU	16-bit	Up-counting, Down-counting, and Triangular-wave (Center-Aligned) Counting modes	2^n(n=0..3)	None	Yes	None	6	3
General-Purpose Timer	UTU1	32-bit	Up-counting	2^n (n=0..7)	None	Yes	None	2	1
	UTU2	16-bit	Up-counting	2^n (n=0..7)	None	Yes	None	2	1
Hall Timer	HTU	24-bit	Up-counting	2^n (n=0..3)	None	None	3	None	None

4.13.1 Advanced Timer(ATU)

The Advanced Timer (ATU) incorporates a 16-bit auto-reload counter driven by a configurable prescaler.

The ATU can generate multiple types of PWM output waveforms (edge-aligned PWM, center-aligned PWM, complementary PWM with asymmetric dead time, etc.).

The ATU operates completely independently and does not share any resources with other internal timers.

Key features of the ATU timer include:

- **16-bit auto-reload counter, supporting up-counting, down-counting (sawtooth), and triangular-wave (center-aligned) modes.**
- **Programmable timer clock prescaler with division factors of 1, 2, 4, or 8.**
- **Capable of outputting 6 independent PWM waveforms or 3 complementary PWM waveforms.**
  - Independent PWM Waveforms:

    The compare intervals for Channels A and B can be configured independently to output PWM waveforms where Channels A and B operate independently of each other.
  - Center-Aligned Complementary PWM Waveforms:

    The compare intervals for Channels A and B can be freely programmed to form asymmetric PWM waveforms.

    The dead time for Channels A and B can be freely programmed to form asymmetric PWM waveforms with dead time.
  - Independent Inverted PWM Waveforms:

    Sawtooth Mode: Can output waveforms with phase shift and 50% duty cycle.

    Triangular-wave Mode: Can output PWM waveforms with configurable duty cycle.
- **Flexible auto-reload configuration; register values can be auto-reloaded triggered by peak or valley signals.**
- **Protection input signal that can force the ATU output signals to a reset or a predefined state.**
- **Internal IOMUX allowing configuration of the 6 PWM outputs to any of the ATU output pins.**
- **Two trigger signals, TRG0 and TRG1, capable of triggering synchronized ADC sampling.**
- **TRGDB can coordinate with the ADC dual sampling mode to synchronously trigger dual sampling for**

ADC GroupB.

- **Comparator (CMP) output blanking function to suppress noise generated during PWM switching within a set time period.**
- **Synchronization trigger circuit enabling the ATU to synchronize with other internal timers.**

4.13.2 General-Purpose Timer(UTU)

This series of MCUs integrates two general-purpose timers, UTU1 and UTU2, which share identical functionality except for differing bit widths.Key features of the general-purpose timers include:

- **32/16-bit (UTU1 is 32-bit, UTU2 is 16-bit) automatic counter loading**
- **3-bit real-time programmable prescaler with divisor factors of 2^n (n=0..7) for programmable counter clock frequency.**
- **Supports both input capture and output compare functions with two capture/compare channels.**
- **Input capture features:**
  - Input filtering capability with configurable filter length.
  - Supports rising edge, falling edge, and both edges triggering.
  - Supports single-channel periodic capture.
  - Supports dual-channel PWM period and duty cycle capture.
- **Comparison output features:**
  - Supports two independent PWM output modes.
  - Supports one complementary PWM output mode.
  - Supports pulse output mode (fixed 50% duty cycle).
  - Supports single-cycle output mode, which can be triggered by software, ATU, or another UTU.
  - Supports output protection functionality; polarity, duration, and default protection output polarity of trigger signals are configurable.
  - Supports output protection in debug mode (Halt).
  - Supports automatic cancellation of output protection upon completion of the timing cycle.
- **Synchronous control of other peripherals**
  - Supports single-trigger operation of ATU or another UTU.
  - Supports periodic triggering of ADC sampling.

4.13.3 Hall Timer(HTU)

The Hall Timer Unit (HTU) is driven by a programmable prescaler. The HTU incorporates a 24-bit auto-load counter, supporting three Hall signal inputs for detecting Hall phase sequence and comparator-linked counting.

The HTU is entirely independent, sharing no resources with other timers.

Key features of the HTU include:

- **24-bit auto-load counter with up-counting capability**
- **Support for three Hall signal inputs**
- **Noise filtering for Hall input signals**
- **Eight 24-bit Hall signal buffer registers**
- **Hall sequence detection**
- **Phase-shift averaging functionality supporting 2/4/8-phase averaging**
- **HTU and comparator CMP synchronised counting**

4.13.4 SysTick Timer

The SysTick timer is dedicated to operating systems and functions as a standard decrementing counter. It possesses the following characteristics:

- **24-bit decrementing counter**
- **Reload capability**

- **Generates a maskable interrupt upon reaching zero**
- **Programmable clock source**

4.14 Independent Watchdog（IWDG）

The independent watchdog is clocked by an internal, independent 40kHz RC oscillator (LSI), featuring a 12-bit decrementing counter and an 8-bit prescaler. As this RC oscillator operates independently of the main clock, it can function during shutdown mode. The IWDG is employed to reset the entire system upon fault detection or functions as a free-running timer for application-level timeout management. Configuration via the option byte enables either software or hardware initiation of the watchdog. During debug mode, this counter may be frozen.

Configuration of the IWDG_WINR register enables the IWDG to operate in window mode.

The IWDG incorporates an interrupt function. When the watchdog counter reaches the value configured in the IWDG_IRQCFG register, it generates the IWDG_IRQ interrupt signal. This can prompt the system to save critical data before a watchdog reset or be utilised for timed wake-up in low-power modes.

4.15 Window Watchdog（WWDG）

The window watchdog incorporates a 7-bit decrementing counter. This counter may be configured for free-running operation or as a watchdog to reset the entire system upon system failure. Driven by the main clock, the window watchdog features an advance warning interrupt function. In debug mode, this counter may be frozen.

4.16 Analog-to-Digital Converter (ADC)

It features a built-in 12-bit Analog-to-Digital Converter (ADC) module with two sample groups. The two sample groups can operate simultaneously or individually. Each group's sampling channels can be configured independently, supporting up to 14 external channels (corresponding to 16 external pins) and 6 internal channels.

- **12-bit fixed resolution.**
- **The ADC operating clock can reach 32 MHz. At 12-bit resolution, the ADC sampling rate can reach up to 2.285 MSPS.**
- **ADC conversion time: At a 2 MSPS conversion rate, the conversion time for 12-bit resolution is 0.5 μs.**
- **The ADC features programmable sampling time; the sampling time for each channel can be configured independently.**
- **Supports synchronized trigger sampling from ATU, UTU1, UTU2, and CMP.**
- **Supports multiple operating modes including Group sampling mode, Dual sampling mode, Continuous sampling mode, and Oversampling averaging mode.**
- **Flexible configuration of sampling sequence for ease of use in different application scenarios.**
- **Conversion data supports both left-aligned and right-aligned formats.**
- **Analog window comparison function, supporting window comparison which can trigger an interrupt.**
- **Configurable number of trigger ignores.**
- **Flexible bias value setting.**
- **Each conversion group channel has an independent result register.**
- **Features priority preemption functionality.**

4.16.1 Internal Reference Voltage (VREFINT)

The internal reference voltage (VREFINT) provides a stable (bandgap) voltage output for the ADC.

4.16.2 VREFP Internal Supply Voltage

The VREFP internal supply voltage can be selected from 2.4V Vref, 3.6V Vref, or VDDA.

Note:

When selecting 2.4V Vref as the VREFP internal supply voltage, V_{DD} must be above 2.9V. When selecting 3.6V Vref, V_{DD} must be above 4V.

4.16.3 Temperature Sensor (TS)

The temperature sensor generates a voltage that varies linearly with temperature, approximately in the range of 300 mV (@ -40°C) to 600 mV (@ +105°C). The temperature sensor is internally connected to the TS input channel of the ADC, used to convert the sensor's output voltage into a digital value.

Due to process variations, the offset of the temperature sensor differs from chip to chip. The internal temperature sensor is suitable for applications detecting temperature changes rather than measuring absolute temperature. If accurate temperature readings are required, an external temperature sensor component should be used.

4.17 Voltage Divider (VDIV)

An internal 10-bit voltage divider (VDIV) is included, which can be used to convert a digital signal into an analog voltage output. When the VDIV channel is enabled and a value is written to the VDIV channel data register, a corresponding analog output voltage is generated on the VDIV channel.

- **One channel data register**
- **10-bit voltage output**
- **One write-protection register**

4.18 Programmable Gain Amplifier (PGA)

The device integrates two programmable gain amplifiers (PGA1 and PGA2). Their main features are as follows:

- **Rail-to-rail input/output**
- **Low offset voltage**
- **Supports differential input or single-ended input**
- **Multiple gain options (x1, x4, x8, x12, x20, x40)**
- **Built-in multi-level bias voltages (Vref/2, Vref/4, Vref/8, Vref/16)**
- **PGA1 supports polling amplification for two sets of input signals**
- **PGA1 supports automatic or manual switching between the two input signal sets during polling operation**
- **Supports cascaded amplification of PGA1 and PGA2**
- **Supports register write protection**

The PGAs can operate in the following modes:

- **Polling Mode (supported only by PGA1)**
- **Pin-Saving Mode**
- **Cascaded Mode**

4.19 Voltage Comparator (CMP)

The device integrates two comparators, CMP1 and CMP2. These comparators can be used independently and serve the following purposes:

- **Analog signal conditioning.**
- **When combined with the PWM output of a timer, they form a cycle-by-cycle current control loop.**

The main features of the CMP include:

- **Configurable comparator hysteresis mode.**
- **Configurable hysteresis thresholds: 0/10/30/60 mV.**
- **Configurable comparator output polarity.**
- **Flexible input selection for each comparator; both positive and negative inputs are configurable.**
  - Multiple I/O pins are provided for positive/negative input selection.
  - Multiple positive input options such as PGAx_OUTx and PGAx_P are provided.
  - Negative input options such as VDIV_OUT and BEMF_N are provided. VDIV_OUT is the internal VDIV output, and BEMF_N is the internal neutral point.
- **The comparator output can serve as an input protection signal for the ATU/UTU.**
- **Supports digital filter function.**

- **Built-in real-time BEMF neutral point detection.**
- **ATU PWM blanking time masking function.**
- **The filtered comparator output can be used to trigger ADC sampling.**

4.20 Division and Square Root Unit (DVSQ)

The Division and Square Root (DVSQ) calculation unit supports the following features:

- **Supports 32-bit signed (SDIV) and unsigned (UDIV) division, and 32-bit square root operation.**
- **The DVSQ unit cannot perform division and square root operations simultaneously; only one operation can be executed at a time.**
- **Upon completion of a 32-bit signed/unsigned integer division operation, both the quotient and remainder can be obtained simultaneously and updated to the corresponding registers.**
- **Division operations support the MOD operation.**
- **For unsigned square root operations, high-precision calculation can be selected via software.**
- **Pipeline design, processing 2 bits per clock cycle.**
- **Calculation time varies depending on the operands.**
- **Supports divide-by-zero interrupt and overflow interrupt.**

4.21 I²C Bus

The MCUs of this series feature one I²C bus interface, capable of operating in multi-master and slave modes, supporting Standard mode (up to 100 kHz), Fast mode (up to 400 kHz), and Ultra-Fast mode (up to 1 MHz).

The I²C clock is derived from PCLK2.

Table 4- 2 I²C Characteristics

I²C Characteristics	I²C 1
Master/Slave Mode	Supported
Multi-host mode	Supported
Standard/fast mode	Supported
7/10-bit addressing mode	Supported
Broadcast call	Supported
Event management	Supported
Clock extension	Supported
Software reset	Supported
DMA Transfer	Not Supported
Digital and analog filters	Supported

4.22 Universal asynchronous receiver transmitter（UART）

The device integrates two Universal Asynchronous Receiver/Transmitters (UART1/UART2), supporting a maximum communication rate of up to 8 Mbit/s. They support functions such as single-wire half-duplex communication and multi-processor communication. Additionally, they feature noise filtering to eliminate signal glitches and resynchronization to tolerate larger clock deviations.

The extended mode supports LIN master mode break transmission and LIN slave mode break detection functions.

Table 4- 3 UART characteristics

UART Characteristics	UART1/UART2
Data word length	8/9 bits
Multi-processor communication	Supported
Single-wire half-duplex communication	Supported
LIN Mode	Supported
Noise Filtering	Supported
Resynchronization	Supported

4.23 Debug Interface (DBG)

The embedded ARM SWJ-DP interface enables a Serial Wire Debug (SWDIO/SWCLK) debug interface.

4.24 96-bit UID

The reference number provided by the 96-bit product unique identity (UID) is unique to any individual MetaWells chip under all circumstances. This identity cannot be modified by the user. Depending on the application, this 96-bit UID can be read in units of bytes (8 bits), half-words (16 bits), or full words (32 bits). The 96-bit UID is suitable for:

- **Use as a serial number (e.g., for USB string serial numbers or other end applications).**
- **Use as a password. When programming the flash memory, this UID can be used in conjunction with software encryption/decryption algorithms to enhance the security of the code within the flash memory.**
- **Activating a secure boot process with security mechanisms.**

4.25 Built-in Driver

The chip integrates a three-phase brushless gate driver designed to drive P+N structure MOSFETs. It includes a built-in input voltage V_{IN} undervoltage lockout (UVLO) protection function, effectively preventing the power transistors from operating at excessively low voltages. It also features built-in over-temperature protection and dead time, providing effective protection for the power devices.

4.25.1 Dead Time Function

A fixed dead time protection circuit is implemented internally. During the dead time, the high-side is set to a high level and the low-side output is set to a low level. The configured dead time must ensure that one power transistor is fully turned off before another is turned on, effectively preventing shoot-through conditions between the high-side and low-side power transistors. If an external dead time (EDT) is set via the logic inputs, the total dead time equals the external dead time (EDT) plus the internally set dead time (DT).

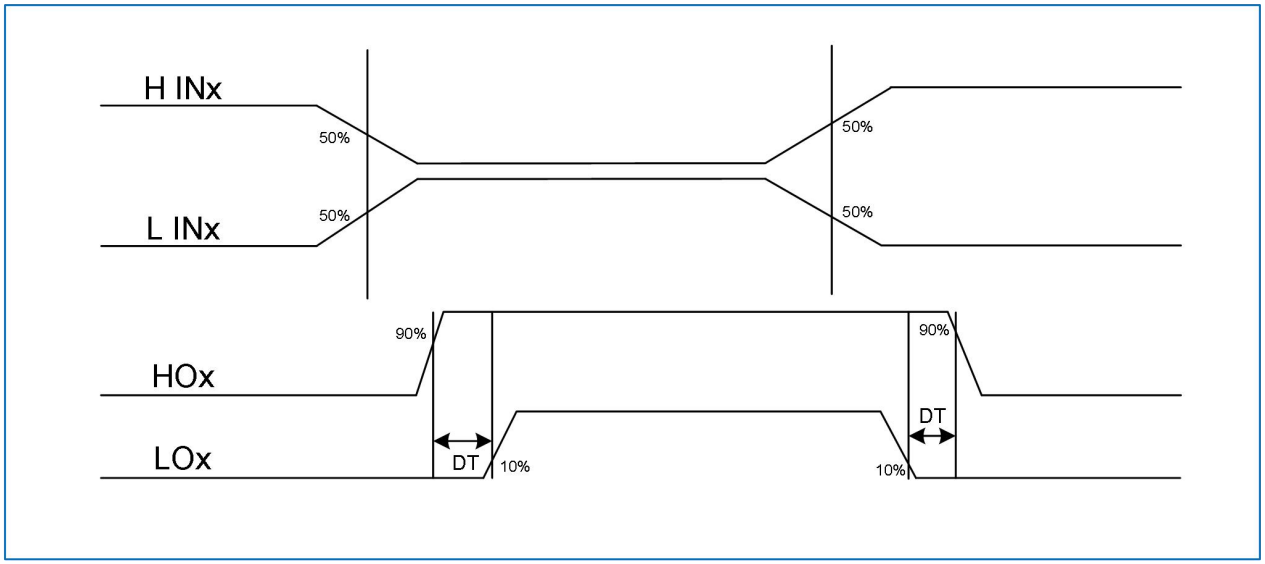


Figure 4- 6 Dead Time Diagram

4.26 LDO

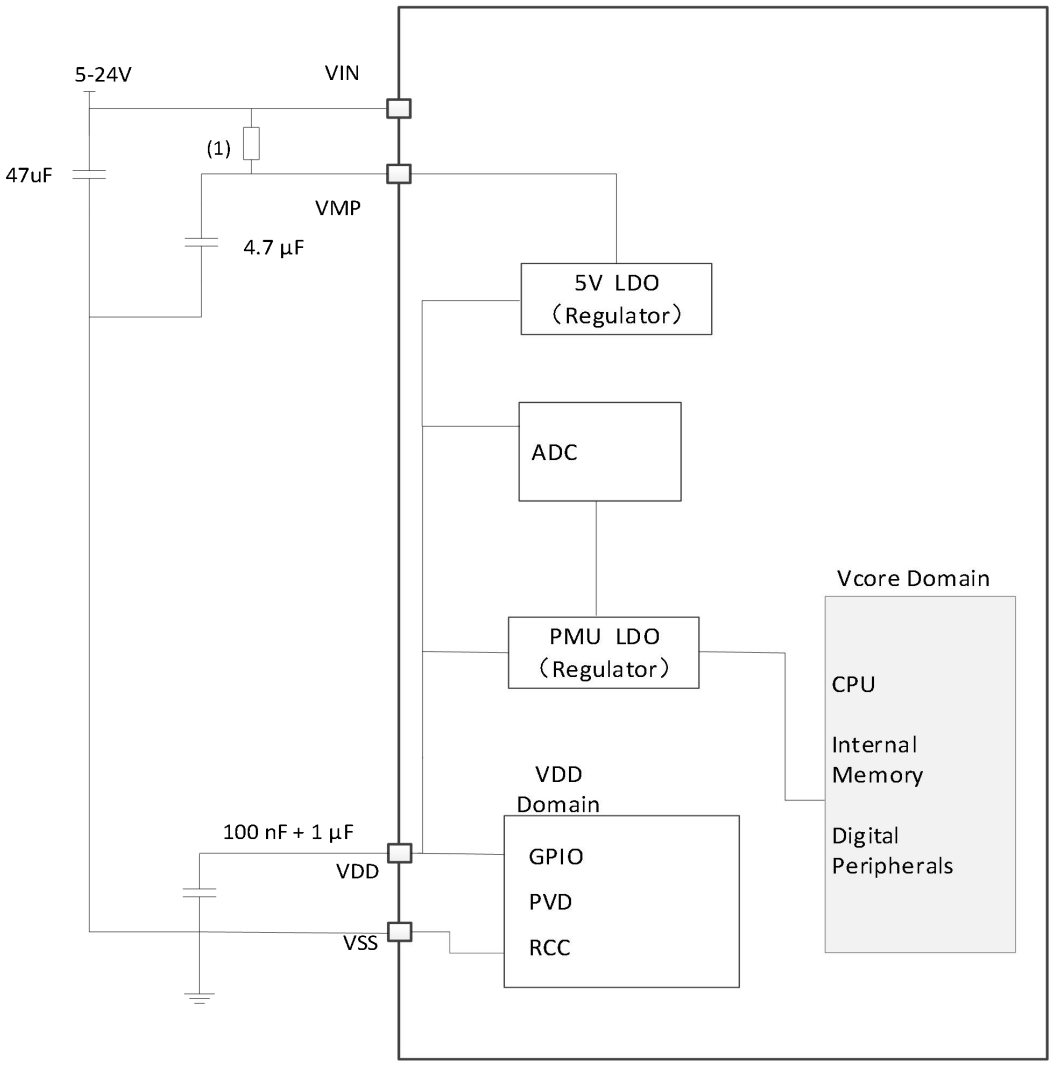
The chip integrates one 5V / 50mA LDO.

4.27 MOSFET

The chip integrates three half-bridge MOSFETs in P+N configuration with low RDS(ON).

5 Electrical Characteristics

5.1 Power Supply



(1). Select resistor values according to the actual application.

Figure 5- 1 Power Supply Block Diagram

5.2 Maximum Absolute Ratings

The maximum rated value is only a short-term stress ratings.

Notes：

- Do not operate the chip at this value or any other conditions exceeding the recommended values.
- Refer to Tables 5-1 to 5-3 for the maximum rated values of the chip. Exceeding the maximum rated values may result in permanent damage to the chip.
- Operating for prolonged periods at maximum rated values may affect the chip's reliability.

5.2.1 Limit Voltage Characteristics

Table 5- 1 Limit Voltage Characteristics

Symbol	Description	Minimum	Maximum	Unit
V_{IN}	Voltage Range	5	40	V

Symbol	Description	Minimum	Maximum	Unit
V_{IO}	Input voltage on pins	-0.3	5.8	

5.2.2 Limit Current Characteristics

Table 5-2 Limit Current Characteristics

Symbol	Parameter	Maximum	Unit
I_{VIN}	Maximum current flowing through V_{IN}	5000	mA
I_{VDD}(1)	Total current passing through V_{DD} power lines (supply current)(5)	120	
I_{VSS}(1)	Total current passing through V_{SS} ground lines (drain current) (5)	95	
I_{IO}(1)	Output sinking current on any I/O and control pin	50	
	Output pulling current on any I/O and control pin	50	
$I_{INJ(PIN)}$(1)	Injection current on I/O pins (2)(3)	-3/+3	
$\Sigma I_{INJ(PIN)}$(1)	Total injection current on all I/O and control pins (4)	-30/+30	

(1). Design guaranteed.

(2). Reverse injection current can interfere with the analog performance of the device.

(3). When $V_{IN} > V_{DD}$, a forward injection current occurs; when $V_{IN} < V_{SS}$, a reverse injection current occurs. The absolute value of the injection current must not exceed the specified limits.

(4). When multiple I/O pins have injection currents simultaneously, the maximum value of $\Sigma I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of the forward and reverse injection currents.

(5). All power supply (V_{DD}) and ground (V_{SS}) pins must always be connected to an external power system within the allowable range.

5.2.3 Limit Temperature Characteristics

Table 5-3 Limit Temperature Characteristic

Symbol	Parameter	Minimum	Maximum	Unit
T_{STG}(1)	Storage temperature range	-65	150	°C
T_J(1)	Maximum junction temperature	-40	125	°C

(1). Design guaranteed.

5.2.4 LDO Characteristics

Table 5-4 LDO Characteristics

Symbol	Description	Maximum	Unit
V_{LDO5V}	5V LDO Output / MCU V_{DD} Input	5.5	V
I_{LDO5V}	5V LDO Maximum Output Current: 50 mA	50	mA

5.3 Operating Parameters

5.3.1 Recommended Operating Conditions

Table 5-5 Recommended Operating Condition

Symbol	Parameter	Minimum	Maximum	Unit
V_{IN}	Power supply voltage range	5	24	V
$V_{LDO5Vout}$	5V LDO output voltage range		5.5	V
$I_{LDO5Vout}$	5V LDO output current range		30	mA
f_{HCLK}(1)	Internal APB Clock Frequency	-	64	MHz
f_{PCLK1}(1)	Internal APB1 Clock Frequency	-	64	
V_{DD}	Standard Operating Voltage	8	24	V
T(1)	Operating Temperature	-40	105	°C

(1). Design guaranteed.

5.3.2 Power-On/Power-Down Slew Rate Operating Conditions

Table 5-6 Power-On/Power-Down Slew Rate Operating Conditions

Symbol	Parameter	Condition	Minimum	Maximum	Unit
t_{VDD}(1)	V_{DD} Rise Slew Rate	-	2	20,000	μs/V
	V_{DD} Fall Slew Rate	-	30	∞	μs/V

(1). Design guaranteed.

5.3.3 Programmable Voltage Detector (PVD) Characteristics

Table 5-7 PVD Characteristics

Symbol	Parameter	Threshold	Minimum	Typical Value	Maximum	Unit
V_{PVD}	PVD detection level selection (V_{DD} rising edge) (-40°C to +105°C))	V_{PVD1}	2.291	2.333	2.383	V
		V_{PVD2}	2.491	2.533	2.582	
		V_{PVD3}	2.681	2.731	2.781	
		V_{PVD4}	2.872	2.928	2.98	
		V_{PVD5}	3.063	3.127	3.172	
		V_{PVD6}	3.259	3.324	3.37	
		V_{PVD7}	3.451	3.524	3.572	
		V_{PVD8}	3.648	3.728	3.772	
		V_{PVD9}	3.852	3.928	3.971	
		V_{PVD10}	4.049	4.13	4.179	
		V_{PVD11}	4.242	4.329	4.373	

Symbol	Parameter	Threshold	Minimum	Typical Value	Maximum	Unit
		V_{PVD12}	4.442	4.527	4.571	
		V_{PVD13}	4.65	4.74	4.782	
		V_{PVD14}	4.842	4.934	4.982	
	PVD detection level selection (V_{DD} falling edge) (-40°C to +105°C)	V_{PVD1}	2.239	2.284	2.315	V
		V_{PVD2}	2.439	2.484	2.518	
		V_{PVD3}	2.636	2.682	2.719	
		V_{PVD4}	2.835	2.883	2.931	
		V_{PVD5}	3.037	3.085	3.127	
		V_{PVD6}	3.227	3.284	3.329	
		V_{PVD7}	3.428	3.486	3.538	
		V_{PVD8}	3.625	3.69	3.747	
		V_{PVD9}	3.825	3.889	3.949	
		V_{PVD10}	4.026	4.091	4.149	
		V_{PVD11}	4.216	4.291	4.355	
		V_{PVD12}	4.408	4.487	4.548	
		V_{PVD13}	4.629	4.701	4.767	
		V_{PVD14}	4.808	4.891	4.966	

5.3.4 Brown-Out Reset (BOR) Characteristics

Table 5-8 BOR Characteristics

Symbol	Parameter	Threshold	Minimum	Typical Value	Maximum	Unit
V_{BOR}	BOR(1) Detection Level Selection (V_{DD} Rising Edge) (-40°C to +105°C)	V_{BOR1}	2.291	2.333	2.383	V
		V_{BOR2}	2.491	2.533	2.582	
		V_{BOR3}	2.681	2.731	2.781	
		V_{BOR4}	2.872	2.928	2.98	
		V_{BOR5}	3.063	3.127	3.172	
		V_{BOR6}	3.259	3.324	3.37	
		V_{BOR7}	3.451	3.524	3.572	
		V_{BOR8}	3.648	3.728	3.772	
		V_{BOR9}	3.852	3.928	3.971	
		V_{BOR10}	4.049	4.13	4.179	

Symbol	Parameter	Threshold	Minimum	Typical Value	Maximum	Unit
		V_{BOR11}	4.242	4.329	4.373	
		V_{BOR12}	4.442	4.527	4.571	
		V_{BOR13}	4.65	4.74	4.782	
		V_{BOR14}	4.842	4.934	4.982	
	BOR(1) Detection Level Selection (V_{DD} Falling Edge) (-40°C to +105°C)	V_{BOR1}	2.239	2.284	2.315	V
		V_{BOR2}	2.439	2.484	2.518	
		V_{BOR3}	2.636	2.682	2.719	
		V_{BOR4}	2.835	2.883	2.931	
		V_{BOR5}	3.037	3.085	3.127	
		V_{BOR6}	3.227	3.284	3.329	
		V_{BOR7}	3.428	3.486	3.538	
		V_{BOR8}	3.625	3.69	3.747	
		V_{BOR9}	3.825	3.889	3.949	
		V_{BOR10}	4.026	4.091	4.149	
		V_{BOR11}	4.216	4.291	4.355	
		V_{BOR12}	4.408	4.487	4.548	
		V_{BOR13}	4.629	4.701	4.767	
		V_{BOR14}	4.808	4.891	4.966	
$V_{BORhyst}$	BOR Hysteresis	-	-2	67	155	mV
t_{BORRST}(2)	Effective Time	-	-	40	-	μs

(1). BOR monitors V_{DD} only.

(2). Design guaranteed.

5.3.5 Power-On/Power-Down Reset (POR/PDR) Characteristics

Table 5-9 Power-On/Power-Down Reset characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
$V_{POR/PDR}$	POR/PDR Thresholds(1)	Falling Edge	1.977	2.006	2.049	V
		Rising Edge	2.031	2.07	2.112	V
$V_{PDRhyst}$	PDR Hysteresis	-	12	64	125	mV
$t_{RSTTEMPO}$ (2)	Reset Timing	-	-	4	-	ms

(1). PDR and POR monitor V_{DD} only.

(2). Design guaranteed.

5.3.6 Internal Reference Voltage Characteristics

Table 5-10 Internal Reference Voltage Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value(2)	Maximum	Unit
V_{REFINT}(1)	Internal Reference Voltage	-40 ~ 105°C;V_{DD} =3.3V	1.18	1.2	1.22	V
$Ripple_{REFINT}$(3)	Reference Voltage Variation Over Full Temperature Range	-40 ~ 105°C;V_{DD} =3.3V	-1.65	-	1.65	%

(1). Actual test results of multiple samples after trimming completion.

(2). Target value for trimming.

(3). Actual test results of multiple samples for the temperature coefficient at 20°C.

5.3.7 Operating Current Characteristics

Table 5-11 Operating Current Characteristics

Symbol	Mode	Condition	V_{DD}=3.3V				V_{DD}=5V				Unit
			-40°C	25°C	85°C	105°C	-40°C	25°C	85°C	105°C	
I_{DD}	Run Mode	CPU running at 64 MHz; All peripherals enabled.	6.43	6.50	6.52	6.53	6.49	6.57	6.60	6.61	mA
		CPU running at 64 MHz; All peripherals enabled.	4.14	4.22	4.28	4.30	4.19	4.28	4.35	4.37	mA
		CPU running at 8 MHz; All peripherals enabled.	2.12	2.19	2.26	2.29	2.20	2.29	2.36	2.38	mA
		CPU running at 8 MHz; All peripherals enabled.	1.84	1.91	1.99	2.01	1.92	2.01	2.08	2.11	mA
I_{Sleep}	Sleep Mode	CPU running at 64 MHz; All peripherals disabled; All IOs configured in analog mode.	1.95	2.01	2.07	2.09	2.06	2.13	2.19	2.21	mA
		CPU running at 8 MHz; All peripherals disabled; All IOs configured in analog mode.	1.84	1.91	1.98	2.01	1.92	2.01	2.08	2.11	mA
		CPU running at 40 kHz; All peripherals disabled; All IOs configured in analog mode.	0.96	1.04	1.11	1.14	1.08	1.16	1.23	1.26	mA
I_{Stop}	Normal Stop Mode	CPU halted; IWDG disabled; All other peripherals halted; All IOs configured in	0.16	0.19	0.22	0.24	0.16	0.19	0.23	0.24	mA

Symbol	Mode	Condition	V_{DD}=3.3V				V_{DD}=5V				Unit
		analog mode.									
$I_{lp\text{-}Stop}$	Low-power Stop Mode	CPU halted; IWDG disabled; All other peripherals halted; All IOs configured in analog mode.	0.03	0.04	0.05	0.05	0.04	0.04	0.05	0.06	mA

(1). Design guarantee.

5.3.8 Internal High-speed HSI Clock Characteristics

Table 5- 12 HSI Clock Characteristics

Symbol	Parameter	Condition		Minimum	Typical Value	Maximum	Unit
f_{HSI}(1)	Factory Calibration Target Frequency	-		-	64	-	MHz
DuCy(1)	Duty cycle	-		45	-	55	%
ACC	Oscillator accuracy	Factory Calibration, Room Temperature		-1	-	1	
		Factory calibration	T_A= –40 ~ +105°C	-3.2	-	2.1	
$T_{su\ (HSI)}$ (1)	Oscillator start time	-		-	3.95	-	μs
$I_{DD\ (HSI)}$ (1)	Power consumption of oscillator	64MHz, V_{DD}=5V		-	430		μA

(1). Design guarantee.

5.3.9 Internal Low-speed LSI Clock Characteristics

Table 5- 13 LSI Clock Characteristics

Symbol	Parameter	Condition		Minimum	Typical Value	Maximum	Unit
f_{HSI}(1)	Factory Calibration Target Frequency	-		-	40	-	MHz
ACC	Oscillator accuracy	Factory Calibration, Room Temperature		-1	-	1	%
		Factory calibration	T_A= –40 ~ +105°C	-4.4	-	1.9	
$T_{su\ (HSI)}$ (1)	Oscillator start time	-		-	2.6	-	μs
$I_{DD\ (HSI)}$ (1)	Power consumption of oscillator			-	30	-	μA

(1). Design guarantee.

5.3.10 GPIO External Clock Input Characteristics

Supports clock input from PA0 and PB15. The waveform requirements are as follows:

Table 5-14 GPIO External Clock Input Characteristics

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit
F_{Ext}	Input Clock Frequency	0	-	32	MHz
	Input Clock Duty Cycle	45	-	55	%

5.3.11 Flash Memory Characteristics

Table 5-15 Flash Memory Characteristics

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit
T_{PROG}	Half-word write time	10	-	13	μs
T_{ERASE}	Page erase time	2	-	3	ms
	Chip erase time	30	-	40	ms
I_{DDPROG}	Programming current	-	-	1.2	mA
$I_{DDERASE}$	Page/chip erase current	-	-	0.6	mA
I_{DDREAD}	Read current	-	-	1.2(@25MHz)	mA
N_{END}	Write/erase endurance	100	-	-	k times
t_{RET}	Data retention time	10@105°C	20@85°C	100@25°C	years

(1). Typical values are measured at 1.5V TT process and 25°C.

(2). Design guaranteed.

5.3.12 IO Input Pin Characteristics

Table 5-16 IO Input Pin DC Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
V_{IH}	Input High Level	V_{DD}=5.0V	0.7*V_{DD}	-	-	V
V_{IL}	Input Low Level	V_{DD}=5.0V	-	-	0.3* V_{DD}	V
V_{hys}	Schmitt Trigger Hysteresis Voltage	V_{DD}=5.0V	870	920	990	mV
I_{lkg}	Input Leakage Current	V_{DD}=5.0V	-10	-	55	μA
R_{PU}	Pull-up Resistor	V_{DD} =5.0V	18	24	34	KΩ
R_{PD}	Pull-down Resistor	V_{DD} =5.0V	17	23	35	KΩ
C_{IO}(1)	I/O Pin Capacitance	V_{DD} =5.0V	-	5	-	pF

(1). All I/Os support Schmitt trigger functionality; design guaranteed.

5.3.13 IO Output Pin Characteristics

Table 5-17 IO Output Pin DC Characteristics

Symbol	Parameter	Condition			Minimum	Typical Value	Maximum	Unit
		Drive Strength Setting OSPEEDRy[1:0]	V_{DD} Voltage (V)	VOH $_{(min)}$ /VOL $_{(max)}$ Voltage Value (V)				
I_{OH}	Source Current	2'bx0	2.5	1.7	-	2.39	-	mA
			3.3	2.4	-	3.67	-	mA
			5	3.5	-	7.87	-	mA
		2'b01	2.5	1.7	-	12.68	-	mA
			3.3	2.4	-	18.79	-	mA
			5	3.5	-	38.49	-	mA
		2'b11	2.5	1.7	-	16.37	-	mA
			3.3	2.4	-	23.9	-	mA
			5	3.5	-	49.14	-	mA
I_{OL}	Sink Current	2'bx0	2.5	0.5	-	2.16	-	mA
			3.3	0.66	-	3.74	-	mA
			5	1	-	7.66	-	mA
		2'b01	2.5	0.5	-	12.3	-	mA
			3.3	0.66	-	20.89	-	mA
			5	1	-	42.20	-	mA
		2'b11	2.5	0.5	-	16.01	-	mA
			3.3	0.66	-	27.06	-	mA
			5	1	-	53.74	-	mA

Table 5-18 IO Output AC Characteristics

Symbol	Parameter	Condition			Minimum	Typical Value	Maximum	Unit
		C_L	Drive Strength OSPEEDRy[1:0]	V_{DD} Voltage (V)				
t_R	Rise Time (Low-to-High Level Output)	C_L=65pF	2'bx0	2.5	-	96	-	ns
				3.3	-	83	-	ns
				5	-	55	-	ns
			2'b01	2.5	-	11.4	-	ns
				3.3	-	10.13	-	ns
				5	-	9.73	-	ns
			2'b11	2.5	-	10.73	-	ns
				3.3	-	8.4	-	ns
				5	-	7.87	-	ns
t_F	Fall Time (High-to-Low Level Output)	C_L=65pF	2'bx0	2.5	-	96	-	ns
				3.3	-	79.67	-	ns
				5	-	53.67	-	ns
			2'b01	2.5	-	10.47	-	ns
				3.3	-	9.67	-	ns

Symbol	Parameter	Condition			Minimum	Typical Value	Maximum	Unit
		C_L	Drive Strength OSPEEDRy[1:0]	V_{DD} Voltage (V)				
				5	-	8.2	-	ns
			2'b11	2.5	-	9	-	ns
				3.3	-	8	-	ns
				5	-	7.27	-	ns

5.3.14 NRST Reset Pin Characteristics

The NRST pin integrates a pull-up resistor inside, and the peripheral application circuit can be connected to any circuit or an external RC circuit.

Table 5-19 NRST Pin Input Characteristics

Symbol	Parameter	Minimum	Maximum	Unit
T_{Noise}	Filtered Pulse Width or Pulse width ignored	-	260	ns

An external filter capacitor on the NRST pin is used for noise immunity, preventing unintended chip resets caused by interference. Users must ensure the voltage on the NRST pin remains below the maximum V_{IL} threshold; otherwise, the reset signal will be ignored.

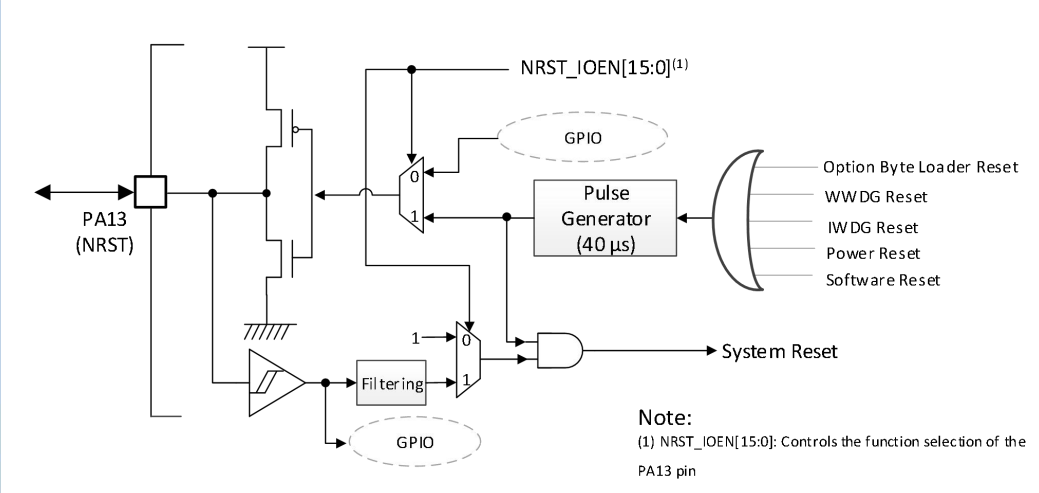


Figure 5-2 Recommended Reset Circuit

5.3.15 Advanced Timer Characteristics

Table 5-20 ATU Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
f_{EXT}(1)	PWM_IO0 ~ PWM_IO5 Output Frequency	$f_{TIMxCLK}$(2)	-	-	$f_{TIMxCLK}/2$	MHz
$t_{res(ATU)}$	Timer Resolution Time	$f_{TIMxCLK}$=64MHz	-	15.6	-	ns
t_{MAX_COUNT}	Clock Period of the 16-bit Counter (when internal clock is selected)	-	-	216	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=64MHz	-	1024	-	µs

(1). Design guaranteed.

(2). The maximum value of $f_{TIMxCLK}$ is 64MHz.

5.3.16 General-Purpose Timer Characteristics

Table 5-21 UTU Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
f_{EXT}(1)	PWM_IO0 ~ PWM_IO1 Output Frequency	$f_{TIMxCLK}$(2)	-	-	$f_{TIMxCLK}/2$	MHz
$t_{res(UTU)}$	Timer Resolution Time	$f_{TIMxCLK}$=64MHz	-	15.625	-	ns
$t_{MAX\_COUNT\_UTU1}$	Clock Period of the 32-bit Counter (when internal clock is selected)	-	-	232	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=64MHz	-	67.108864	-	s
$t_{MAX\_COUNT\_UTU2}$	Clock Period of the 16-bit Counter (when internal clock is selected)	-	-	216	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=64MHz	-	1024	-	μs

(1). Design guaranteed.

(2). The maximum value of $f_{TIMxCLK}$ is 64MHz.

5.3.17 Hall Timer Characteristics

Table 5-22 HTU Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
$t_{res(UTU)}$	Timer Resolution Time	$f_{TIMxCLK}$=64MHz	-	15.6	-	ns
t_{MAX_COUNT}	Clock Period of the 24-bit Counter (when internal clock is selected)	-	-	224	-	$t_{TIMxCLK}$
		$f_{TIMxCLK}$=64MHz	-	262144	-	s

(1). Design guaranteed.

(2). The maximum value of $f_{TIMxCLK}$ is 64MHz.

5.3.18 ADC Characteristics

Table 5-24 ADC Characteristics

Program	Description	Condition	Minimum	Typical Value	Maximum	Unit
V_{DD}	Analog supply voltage when ADC is on	-	2.2	-	5.5	V
f_{ADC}	ADC clock frequency	V_{DD} =2.2~2.7V	-	-	16	MHz
		V_{DD} =2.7~5.5V	-	-	32	MHz
f_S (1)	sampling frequency	f_{ADC} = 32 MHz	-	-	2.28	MSPS
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 32 MHz	-	-	1.88	MHz
		-	-	-	17	Cycles
V_{AIN}	Conversion voltage range	-	V_{SS}	-	V_{DD}	V
R_{AIN} (1)	External input impedance				Please refer to Table 5-25 for details	kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	0.305	kΩ
C_{ADC} (1)	sample-and-hold capacitor	-	-	4	-	pF
t_S (1)	Sampling time	f_{ADC} = 32 MHz	1.5	-	55.5	Cycles
t_{CONV} (1)	The total conversion time includes the sampling time	12-bit resolution	14	-	68	Cycles

(1). Design guarantee.

(2). The maximum allowable input impedance RAIN must satisfy the following formula:

$$R_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

Where: N(Resolution) = 12,T_S is the ADC sampling period (in clock cycles).The allowable error is less than 1/4 LSB Least Significant Bit, LSB.

Table 5-25 Maximum Input Impedance（f_{ADC} = 32 MHz）

Sampling Period Ts（Cycles）	Sampling Time t_S（μs）	Maximum Input Impedance（kΩ）
1.5	0.05	0.9
2.5	0.08	1.71
3.5	0.11	2.51
4.5	0.14	3.32
5.5	0.17	4.12
6.5	0.2	4.93
7.5	0.23	5.73
8.5	0.27	6.54

Sampling Period Ts（Cycles）	Sampling Time t_S（μs）	Maximum Input Impedance（kΩ）
13.5	0.42	10.56
28.5	0.89	22.64
41.5	1.3	33.11
55.5	1.73	44.38

Table 5-26 ADC Accuracy

Symbol	Parameter(3)	Test Conditions(2)	Minimum	Maximum	Unit
ET	Total unadjustable error	f_{ADC}=32MHz	-6	6	LSB
EO	Offset error	f_{ADC}=32MHz	-2	4	
EG	Gain error	V_{DD}=5V	-3	5	
ED	Differential linearity error (1)	Input Impedance < 1 kΩ	-1.5	1.5	
EL	Integral linearity error ((1)	Tested after ADC Calibration	-3	+3	

(1). Design guaranteed.

(2). Test results from multiple samples across the full temperature range.

(3). Parameter description is as follows:

- Total non-adjustable error: the maximum deviation between the actual transfer curve and the ideal transfer curve.
- Offset error: The deviation between the first actual conversion and the first ideal conversion.
- Gain error: The deviation between the last ideal transition and the last actual transition.
- Differential linearity error: the maximum deviation between the actual step and the ideal step.
- Integral linearity error: The maximum deviation between any actual transition and the end point correlation line.

Explain：

- ADC accuracy and negative injection current: Avoid injecting negative current on any standard non-robust analog input pin, as this can significantly reduce the accuracy of performing conversions on another analog input pin. It is recommended to add a Schottky diode pin to the standard analog pin that may inject negative current to ground.
- Better ADC performance can be achieved within a limited range of V_{DDA}, frequency, and temperature.
- The data is based on characterization results and has not been tested in production.

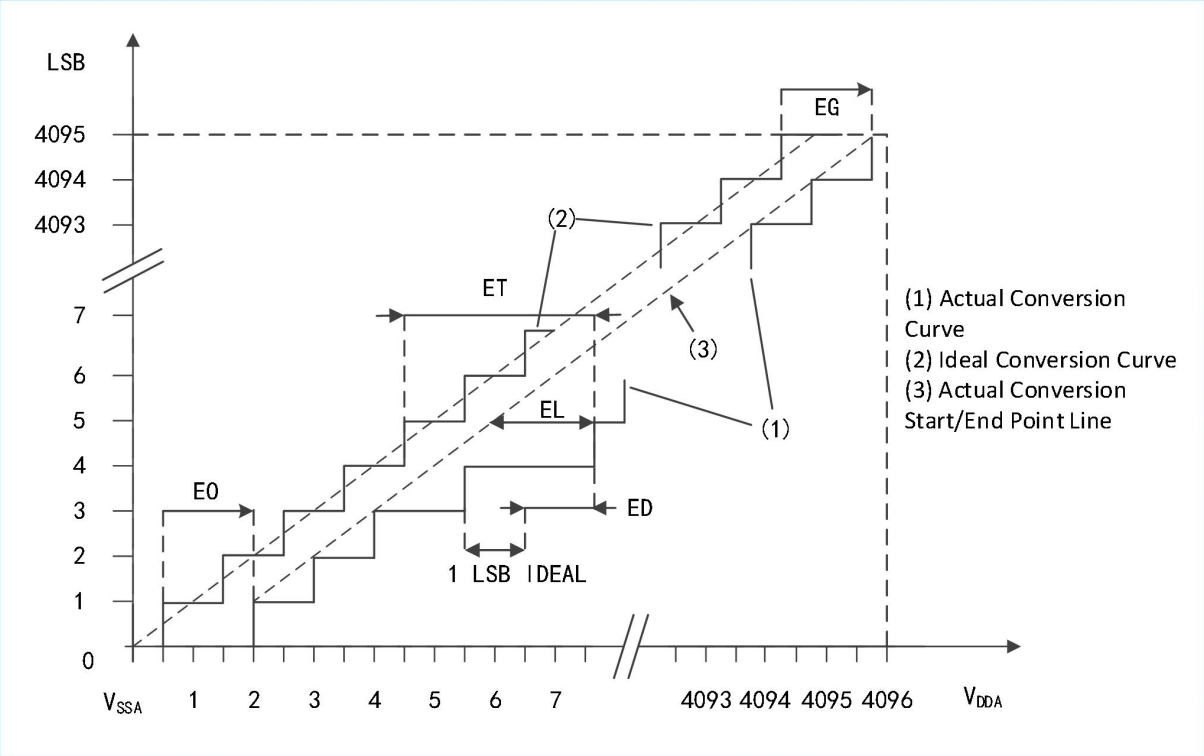


Figure 5-3 ADC Accuracy Characteristics

Explain：

For the parameter descriptions represented by EO, ET, EG, EL, and ED, please refer to Table 5-26.

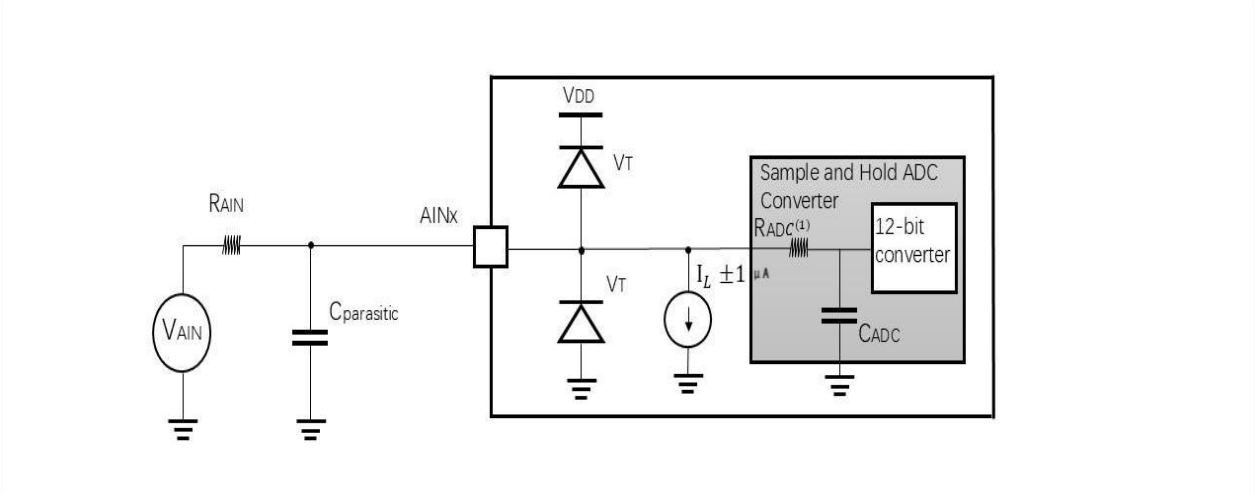


Figure 5-4 Typical ADC Connection Diagram

(1). For R_{ADC} and C_{ADC} values, refer to Table 5-24.

$C_{parasitic}$ equals PCB capacitance depending on soldering and PCB layout quality plus pad capacitance of approximately 7 pF. A too high tangential value will reduce the conversion accuracy. To compensate for this, fADC should be minimized.

Recommendations for PCB design for ADC sampling: power decoupling should be carried out according to Figure 5-1. To ensure the accuracy of ADC conversion, it is recommended to use ceramic capacitors with a capacitance of 10 nF and place them as close to the chip as possible.

5.3.19 VREFP Internal Supply Voltage Characteristics

The chip integrates two internal supply voltage levels, 2.4V and 3.6V, to power the ADC VREFP.

Note:

When selecting 2.4V Vref as the VREFP internal supply voltage, V_{DD} must be above 2.9V. When selecting 3.6V Vref, V_{DD} must be above 4V.

Table 5-27 VREFP Internal Supply Voltage Characteristics

Symbol	Parameter	Conditions	Minimum	Typical Value(2)	Maximum	Unit
VREFP(1)	VREFP Internal Supply Voltage	-40 ~ 105°C; V_{DD} =2.9~5.5V	2.4	2.4	2.44	V
		-40 ~ 105°C; V_{DD} =4~5.5V	3.59	3.6	3.66	V

(1). Actual test results of multiple samples after trimming completion.

(2). Target value for trimming.

5.3.20 Voltage Divider (VDIV) Characteristics

Table 5-28 VDIV Characteristics

Symbol	Parameter	Conditions	Minimum	Typical Value(2)	Maximum	Unit
V_{DD}(1)	VDIV Operating Voltage	-	2.2	-	5.5	V
R_O(1) (2)	Output Impedance	-	-	9	-	kΩ
VDIV_OUT(3)	Output Voltage Range	-	V_{SS}	-	V_{DD}	V
$I_{operating}$	Operating Power Consumption	V_{DD}=5V	255.2	676.1	883.5	μA

(1). Design guaranteed.

(2). VDIV operates without a buffer.

(3). Rail-to-rail output.

5.3.21 Temperature Sensor (TS) Characteristics

Table 5-29 TS Characteristics

Symbol	Parameter	Conditions	Minimum	Typical Value	Maximum	Unit
T_L	Temperature Sensor Linearity Error	-40°C~105°C	-	-	±8	°C
V_{20}	Output Voltage	20°C	378.73	413.14	436.10	mV
Avg_Slope	Temperature Sensor Slope	-	-	1.1762	-	mV/°C

5.3.22 Voltage Comparator (CMP) Characteristics

Table 5-30 CMP Characteristics

Program	Description	Conditions	Minimum	Typical Value	Maximum	Unit
V_{DD}(1)	Analog Supply Voltage	-	2.2	5	5.5	V

Program	Description	Conditions	Minimum	Typical Value	Maximum	Unit
V_{com}(1)	Input Common-Mode Voltage	-	0.2	-	V_{DD}-0.2	V
V_{diff}(1)	Input Differential Voltage	V_{DDA}=5V, V_{com}=2.5V No Hysteresis	5	-	-	mV
V_{hy}(1)	Hysteresis Voltage	Threshold 1	-	0	-	mV
		Threshold 2	-	10	-	
		Threshold 3	-	30	-	
		Threshold 4	-	60	-	
I_{OP}(1)	Quiescent Operating Current	V_{DD} =5V	97.82	142.90	158.20	μA
T_{dly}(1)	Output Delay	Rising Edge	12.00	15.20	31.34	ns
		Falling Edge	16.62	29.58	44.11	

(1) Design guarantee.

5.3.23 Operational Amplifier (PGA) Characteristics

Table 5- 31 PGA Characteristics

Symbol	Description	Conditions	Minimum	Typical Value	Maximum	Unit
V_{DD}(1)	Analog Supply Voltage	-	2.2	5	5.5	V
V_{OUT}	Output Voltage	-	V_{SS}	-	V_{DD}	V
C_{MIR}(1)	Input Common-Mode Voltage	-	0	-	5.5	V
I_{bias}(1)	Input Bias Current	-	0.8	1	1.2	μA
I_{load}	Output Current	RL=100Ω, V_{DD} =5V	-	10	-	mA
I_q	Operating Current	No Load, Quiescent Mode	780	970	1100	μA
I_l(1)	Leakage Current	Amplifier Disabled	480	700	1780	nA
V_{OS}	Input Offset Voltage	Before Calibration	-	±50	-	mV
		After Calibration, VIP=0.5* V_{DD}	-	0.638	-	
		After Calibration, VIP=0.2V	-	2.29	-	
CMRR(1)	Common-Mode Rejection Ratio	-	51	-	145	dB
PSRR_min(1)	Power Supply Rejection Ratio	Buffer Mode	-95.28	-64.89	-51.60	dB
		Single-Ended Gain ×4	-52.43	-47.52	-31.99	

Symbol	Description	Conditions	Minimum	Typical Value	Maximum	Unit
		Single-Ended Gain ×8	-28.31	-40.82	-70.61	
		Single-Ended Gain ×12	-60.04	-37.17	-24.78	
		Single-Ended Gain ×20	-59.98	-32.77	-20.44	
		Single-Ended Gain ×40	-49.88	-27.13	-15.73	
		Differential Gain ×4	-75.84	-46.59	-35.66	
		Differential Gain ×8	-73.15	-40.49	-27.98	
		Differential Gain ×12	-71.49	-37.01	-24.45	
		Differential Gain ×20	-68.98	-32.69	-20.08	
		Differential Gain ×40	-65.08	-26.97	-14.72	
PSRR_max(1)	Power Supply Rejection Ratio	Buffer Mode	-3.83	-2.86	-1.79	dB
		Single-Ended Gain ×4	-1.78	-1.28	-0.89	
		Single-Ended Gain ×8	-2.67	-2.49	-2.05	
		Single-Ended Gain ×12	-3.08	-2.80	-2.57	
		Single-Ended Gain ×20	-3.31	-3.08	-2.80	
		Single-Ended Gain ×40	-3.40	-3.15	-2.92	
		Differential Gain ×4	-2.16	-1.65	-0.91	
		Differential Gain ×8	-3.49	-3.17	-2.84	
		Differential Gain ×12	-3.82	-3.59	-3.38	
		Differential Gain ×20	-3.87	-3.67	-3.48	
		Differential Gain ×40	-3.70	-3.50	-3.28	
GBW	Bandwidth	Single-Ended Gain ×1	8.2710	24.5400	41.7400	MHz
		Single-Ended Gain ×4	3.1170	4.4770	6.2090	
		Single-Ended Gain ×8	1.6840	2.4690	3.4800	
		Single-Ended Gain ×12	1.1390	1.6720	2.3690	
		Single-Ended Gain ×20	0.6963	1.0190	1.4460	
		Single-Ended Gain ×40	0.3647	0.5297	0.7505	

Symbol	Description	Conditions	Minimum	Typical Value	Maximum	Unit
		Differential Gain ×4	3.1560	4.5500	6.3330	
		Differential Gain ×8	1.6890	2.4750	3.4930	
		Differential Gain ×12	1.1420	1.6720	2.3710	
		Differential Gain ×20	0.6992	1.0190	1.4460	
		Differential Gain ×40	0.37	0.53	0.75	
SR_rise	Positive Slew Rate	Gain=1	14.29	15.85	17.62	V/μs
		Gain=4	17.73	18.11	22.15	
		Gain=8	9.27	18.79	24.49	
		Gain=12	5.87	14.31	19.93	
		Gain=20	3.43	9.15	13.79	
		Gain=40	1.69	4.67	7.16	
SR_fall	Negative Slew Rate	Gain=1	14.54	17.08	19.85	V/μs
		Gain=4	14.82	17.48	20.02	
		Gain=8	9.15	15.98	19.53	
		Gain=12	6.05	13.25	17.21	
		Gain=20	3.52	9.35	13.38	
		Gain=40	1.77	4.85	7.50	
φ	Phase Margin	Buffer Mode	44.90	64.28	87.58	Deg
		Single-Ended Gain ×4	56.07	61.68	65.30	
		Single-Ended Gain ×8	75.78	78.97	80.75	
		Single-Ended Gain ×12	82.17	84.09	84.99	
		Single-Ended Gain ×20	86.15	87.23	87.63	
		Single-Ended Gain ×40	88.01	88.84	89.14	
		Differential Gain ×4	55.54	61.54	65.38	
		Differential Gain ×8	75.95	78.86	80.62	
		Differential Gain ×12	82.25	83.98	84.86	
		Differential Gain ×20	86.17	87.13	87.55	
		Differential Gain ×40	87.98	88.76	89.14	
PGA gain	PGA Closed-Loop Gain	Buffer Mode	-	0.99	-	times

Symbol	Description	Conditions	Minimum	Typical Value	Maximum	Unit
		Single-Ended Gain ×4	-	3.90	-	
		Single-Ended Gain ×8	-	7.72	-	
		Single-Ended Gain ×12	-	11.47	-	
		Single-Ended Gain ×20	-	18.74	-	
		Single-Ended Gain ×40	-	35.83	-	
		Differential Gain ×4	-	3.20	-	
		Differential Gain ×8	-	7.16	-	
		Differential Gain ×12	-	10.78	-	
		Differential Gain ×20	-	18.4	-	
		Differential Gain ×40	-	35.67	-	

(1). Design guarantee.

PGA Differential Gain Derivation Diagram and Table

Derivation Process:

A_PGA_O = (((VREF/2 - A_VP) * VREF_GAIN + A_VP) - A_VN) * PGA_GAIN + A_VN

Set A_PGA_O = VREF/2 (when A_VP = A_VN = 0):

VREF/2 = VREF/2 * VREF_GAIN * PGA_GAIN

Thus: PGA_GAIN = 1 / VREF_GAIN

Simplified: A_PGA_O = VREF/2 + (PGA_GAIN - 1) * (A_VP - A_VN)

REAL_GAIN = PGA_GAIN - 1

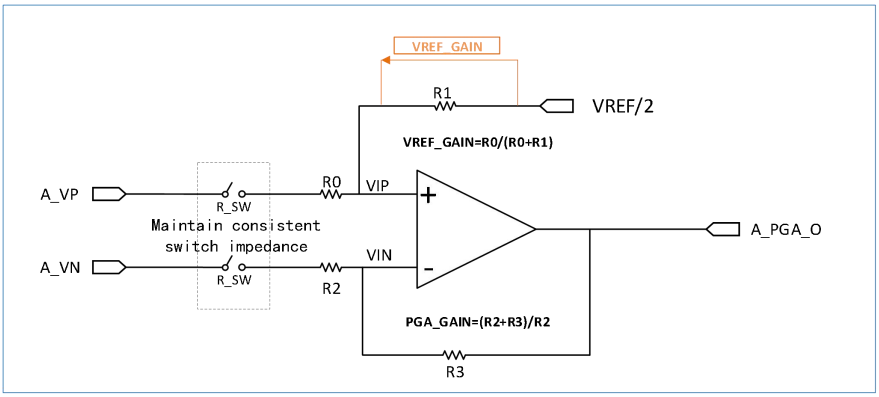


Figure 5- 5 PGA Differential Gain Derivation Diagram

Table 5-32 PGA Internal Resistor Design Characteristics

PGA_GAIN Setting (Multiple)	R0+R_SW (kΩ)	R1 (kΩ)	VREF_GAIN (Multiple)	R2+R_SW (kΩ)	R3 (kΩ)	Actual Single-Ended Gain
4	32.05	95.25	0.2517	32.05	95.25	3.972
8	16.18	111.1	0.1271	16.17	111.1	7.870
12	10.88	116.4	0.0854	10.88	116.4	11.70
20	6.650	120.7	0.0522	6.650	120.7	19.14
40	3.475	123.8	0.0273	3.475	123.8	36.63

5.3.24 Three-Phase Gate Driver Characteristics

Table 5-33 Three-Phase Gate Driver Characteristics

Symbol	Definition	Minimum	Typical Value	Maximum	Unit
I_{VIN}	VIN Quiescent Current		0.6	1.2	mA
V_{UVLO_F}	VIN UVLO Threshold (Falling Edge)		4.05	4.40	V
V_{UVLO_R}	VIN UVLO Threshold (Rising Edge)		4.25	4.60	V
V_{UVLO_H}	VIN UVLO hysteresis		200		mV
R_{PD}	Pull-down resistor		80		kΩ
T_{OND}	Turn-on delay		90		nS
T_{OFFD}	Turn-off delay(OK)		30		nS
DT	Dead time		50		nS
T_{OTP}	Over-temperature protection threshold, turns off entire driver section		150		°C
T_{OTPHYS}	Over-temperature protection hysteresis		15		°C

5.3.25 N-MOS Electrical Characteristics

Table 5-34 N-MOS Electrical Characteristics

Symbol	Description	Condition	Minimum	Typical Value	Maximum	Unit
Cut-off characteristics						
BV_{DSS}	Drain-source breakdown voltage	VGS =0V, ID =250μA	40	-	-	V
I_{DSS}	Drain current with gate-source short-circuited	VDS =40V, VGS =0V	-	-	1	μA
I_{GSS}	Gate current with drain-source short-circuited	VDS =0V, VGS=±20V	-	-	±100	nA
Conduction characteristics						
$R_{DS(ON)}$	Drain-source on-state resistance	VIN=7V,ID=0.5A	-	15	-	mΩ

5.3.26 P-MOS Electrical Characteristics

Table 5-35 P-MOS Electrical Characteristics

Symbol	Description	Condition	Minimum	Typical Value	Maximum	Unit
Cut-off characteristics						
BV_{DSS}	Drain-source breakdown voltage	VGS =0V, ID =-250μA	-40	-	-	V
I_{DSS}	Drain current with gate-source short-circuited	VDS =-40V, VGS =0V	-	-	-1	μA
I_{GSS}	Gate current with drain-source short-circuited	VDS =0V, VGS=±20V	-	-	±100	nA
Conduction characteristics						
$R_{DS(ON)}$	Drain-source on-state resistance	VIN=7V,ID=0.5A	-	35	-	mΩ

6 Pin Definition

PM30225Q-0405 MCU uses TSSOP-25 package, with the following pin definitions.

6.1 TSSOP-25 Package

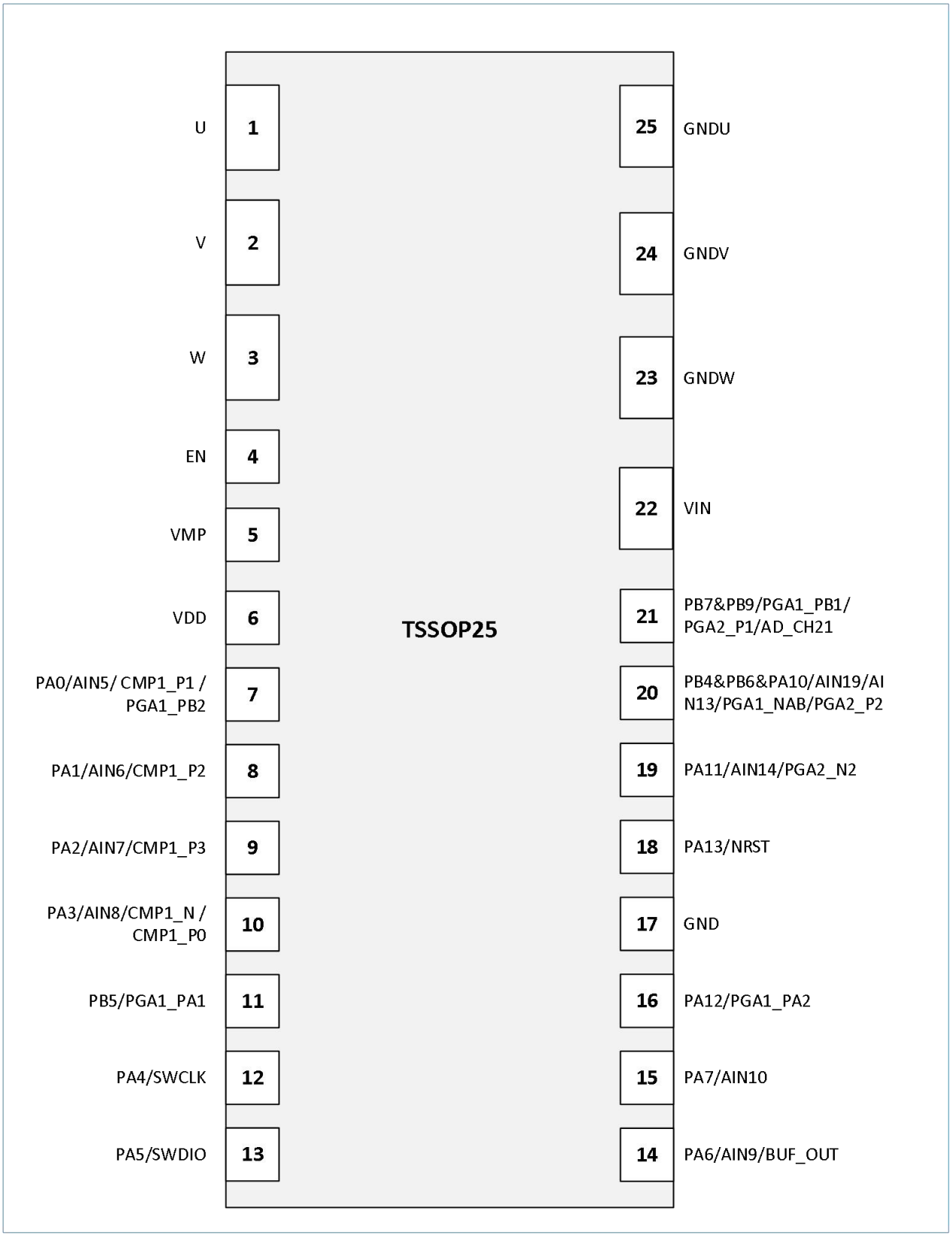


Figure 6- 1 TSSOP-25 Package

6.2 Pin Definition

Table 6-1 Pin Definition

Pin Number	Pin Name	Pin Type (1)	Default Pin Function after Power-On	Default Alternate Function (AF)	Pin Additional Functions
1	U	O	Phase U Output		
2	V	O	Phase V Output		
3	W	O	Phase W Output		
4	EN	I	Chip enable control pin. When EN = 1, the chip operates normally with LDO output active. When EN = 0, the chip enters low-power mode.		
7	PA0	I/O	PA0	RCC_CLK1 Hall_A UART1_TX (3)	AD_CH5 CMP1_P1 PGA1_PB2
8	PA1	I/O	PA1	RCC_MCO UTIOU1B Hall_B UART1_RX	AD_CH6 CMP1_P2
9	PA2	I/O	PA2	UBKI1 Hall_C ADC_IP_TEST_LV	AD_CH7 CMP1_P3
-	PA9	I/O	PA9	ATU_BKIN1 UART1_TX	AD_CH12
-	PA8	I/O	PA8	ATU_BKIN0 UART2_RX	AD_CH11
10	PA3	I/O	PA3	ATU_BKIN0 UBKI2 ADC_Trigo	AD_CH8 CMP1_N CMP1_P0
15	PA7	I/O	PA7	UTIOU1A UART2_TX I2C1_SDA CMP2_Out	AD_CH10
12	PA4(SWCLK)	I/O	SWCLK	UTIOU1A UART2_TX I2C1_SCL PWM_DIR	AD_CH13
13	PA5(SWDIO)	I/O	SWDIO	RCC_MCO UTIOU2A UART2_RX I2C1_SDA	AD_CH14
14	PA6	I/O	PA6	UTIOU1B UART2_RX I2C1_SCL CMP1_Out	AD_CH9 BUF_OUT0

Pin Number	Pin Name	Pin Type (1)	Default Pin Function after Power-On	Default Alternate Function (AF)	Pin Additional Functions
16	PA12	I/O	PA12	UTIOU2A CMP1_Out	PGA1_PA2 BUF_OUT1
19	PA11	I/O	PA11	UBKI1 ADC_Trigo	AD_CH14 PGA2_N2
18	PA13(NRST)	I/O	NRST	UTIOU2B UART1_TX ADC_Trigo	NRST
20	PB4&PB6&PA10	I/O	PB4 & PB6 & PA10	RCC_MCO ATU_BKIN1 UTIOU2A I2C1_SDA UTIOU1A	AD_CH19 PGA1_NA PGA1_PB1 AD_CH13 PGA2_P2
17	GND	S	GND		
11	PB5	I/O	PB5	ATU_BKIN0 UTIOU2B I2C1_SCL	AD_CH20 CMP2_P0 PGA1_PA1
21	PB7&PB9	I/O	PB7&PB9	UTIOU1B	PGA1_PB1 PGA2_P1 AD_CH21
6	VDD	S	The digital and analog power supplies on the chip are connected internally to LDO5V.		
5	VMP	PWR	LDO Input Power Supply		
22	VIN	PWR	Input Operating Power Supply		
23	GNDW	S	W Phase Ground		
24	GNDV	S	V Phase Ground		
25	GNDU	S	U Phase Ground		

(1). "I" represents input, "O" represents output, "I/O" represents input/output, "S" represents power supply.

(2). Pin alternate functions are listed in Table 6-2, “Alternate Function (AF).”

(3). Both UART1 and UART2 support swapping the TX and RX pin functions.

6.3 Pin Alternate Function (AF) Table

Table 6-2 Alternate Function (AF) Table

Pin	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	Hall_A	-	UART1_TX (1)	-	-	-	RCC_CLK1
PA1	-	Hall_B	UTIOU1B	UART1_RX	-	-	-	RCC_MCO
PA2	-	Hall_C	UBKI1	-	-	-	-	-
PA3	ATU_BKIN0	-	UBKI2	-	-	-	-	ADC_Trigo
PA4	SWCLK	-	UTIOU1A	UART2_TX	I2C1_SCL	-	-	PWM_DIR
PA5	SWDIO	-	UTIOU2A	UART2_RX	I2C1_SDA	-	-	RCC_MCO
PA6	-	-	UTIOU1B	UART2_RX	I2C1_SCL	-	-	CMP1_Out
PA7	-	-	UTIOU1A	UART2_TX	I2C1_SDA	-	-	CMP2_Out
PA8	ATU_BKIN0	-	-	UART2_RX	-	-	-	
PA9	ATU_BKIN1	-	-	UART1_TX	-	-	-	
PA10	-	-	-	-	-	-	-	-
PA11	-	-	UBKI1	-	-	-	-	ADC_Trigo
PA12	-	-	UTIOU2A	-	-	-	-	CMP1_Out
PA13	-	-	UTIOU2B	UART1_TX	-	-	-	ADC_Trigo
PB4	ATU_BKIN0	-	UTIOU2A	-	I2C1_SDA	-	-	RCC_MCO
PB5	ATU_BKIN1	-	UTIOU2B	-	I2C1_SCL	-	-	-
PB6	-	-	UTIOU1A	-	-	-	-	-
PB7	-	-	UTIOU1B	-	-	-	-	-
PB9	-	-	-	-	-	-	-	
PB10	PWM_IO0	-	UTIOU2A		-	-	-	-
PB11	PWM_IO1	-	UTIOU2B		-	-	-	-
PB12	PWM_IO2	-	-	UART1_RX	-	-	-	-
PB13	PWM_IO3	-	-	UART1_TX	-	-	-	-
PB14	PWM_IO4	-	-	UART2_RX	-	-	-	-
PB15	PWM_IO5	-	-	UART2_TX	-	-	-	RCC_CLK2

(1). The table above indicates that both UART1 and UART2 support TX and RX pin function swapping.

7 Typical Circuits

7.1 Typical Application Circuit

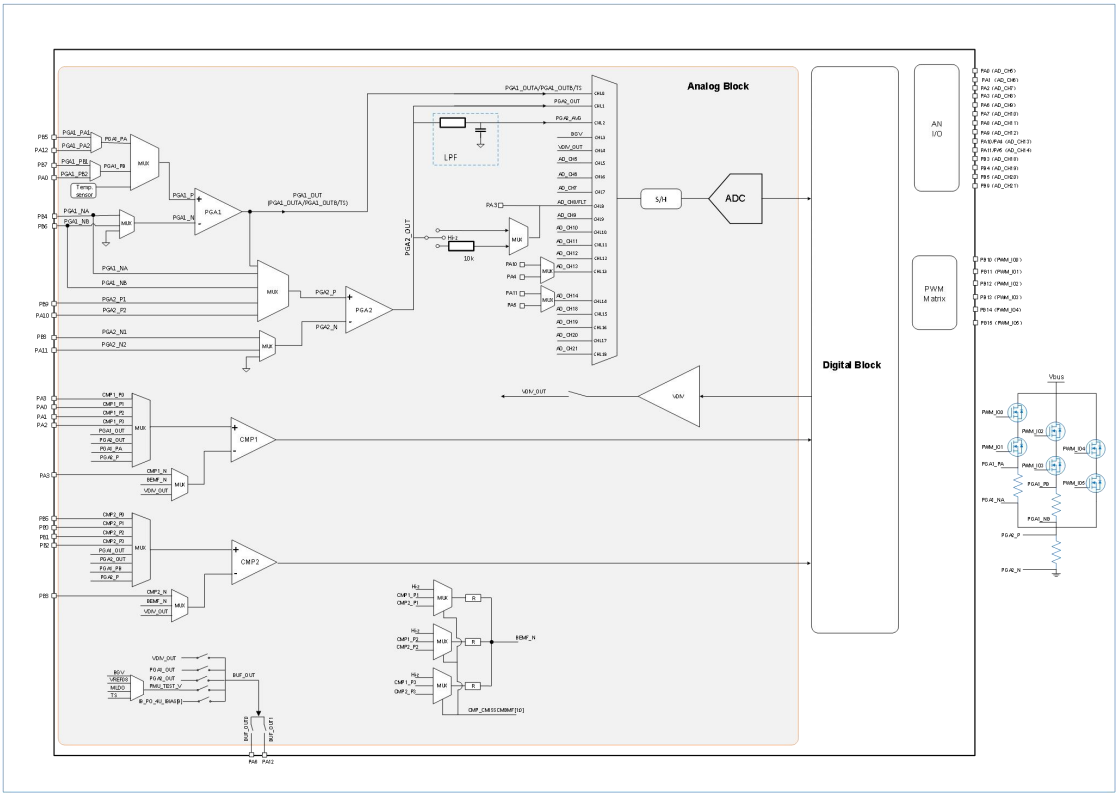


Figure 7-1 Typical Application Circuit

8 Package Parameter

8.1 Package Size

8.1.1 TSSOP-25 Package

Package Size is 9.70 mm x 4.40 mm for TSSOP-25.

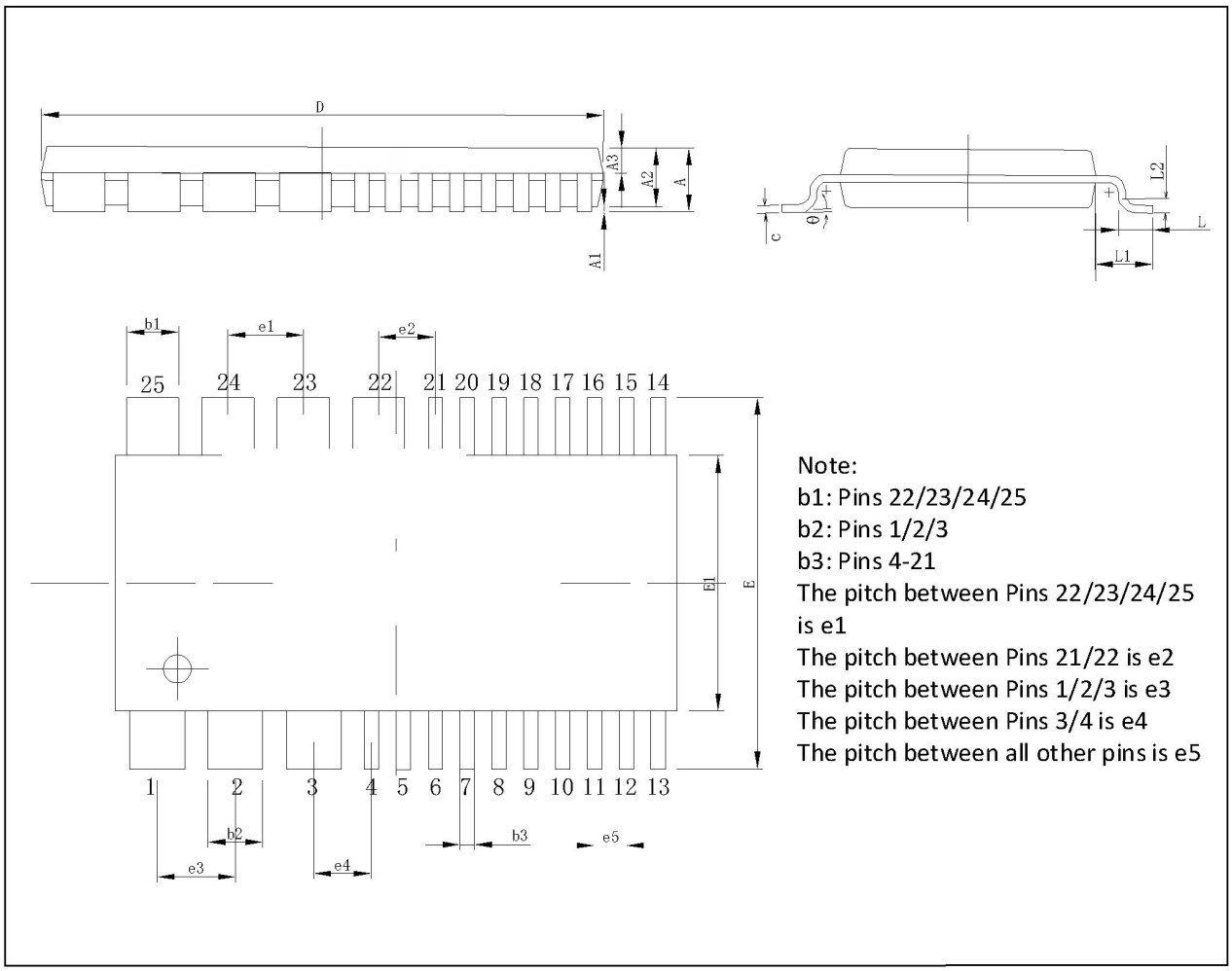


Figure 8-1 TSSOP-25 Package Size

Table 8-1 TSSOP-25 Package Size Parameter

Symbol	Minimum（mm）	Typical Value（mm）	Maximum（mm）
A	-	-	1.2
A1	0.03	0.08	0.12
A2	0.80	-	1.0
A3	0.39	0.44	0.49
b1	-	0.90	-
b2	-	0.95	-
b3	-	0.25	-
c	0.14	-	0.18

Symbol	Minimum（mm）	Typical Value（mm）	Maximum（mm）
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e1	1.3BSC		
e2	0.98BSC		
e3	1.35BSC		
e4	1.0BSC		
e5	0.55BSC		
L	0.45	0.60	0.75
L1	1.0BSC		
L2	0.25BSC		
θ	0	-	8°

9 Acronyms and Terminology

9.1 Acronyms

Acronyms	Full Name
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-Wakeup
CLU	Configurable Logic Unit
CRC	Cyclic Redundancy Check
CSS	Clock Security System
CTS	Clear to Send
DMA	Direct Memory Access
EMACC	Electric Motor Acceleration
EXTI	Extended Interrupts and Events Controller
GPIO	General Purpose Input Output
HSI	High-Speed Internal（Clock Signal）
HSE	High Speed External（Clock Signal）
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
IAP	In-Application Programming
ICP	In Circuit Programming
LSI	Low-Speed Internal（Clock Signal）
MCU	Microcontroller Unit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
OBL	Option Byte Loader
PDR	Power-Down Reset

Acronyms	Full Name
PLL	Phase Locked Loop
POR	Power-On Reset
PPM	Parts per Million
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computing
RTS	Request to Send
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USART	Universal Synchronous Asynchronous Receiver Transmitter
UART	Universal Asynchronous Receiver Transmitter
WWDG	Window Watchdog

9.2 Terminology

Name	Description
Byte	8-bit data length.
Half word	16-bit data or instruction length.
Option byte	MCU configuration bytes stored in Flash.
Word	32-bit data or instruction length.

10 Version History

Version	Date	Changes
Rev.1.0	2025-09-23	Initial release
Rev.2.0	2025-12-30	Updated key electrical and performance parameters.

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