PM30003V-0405BQ Datasheet

40V , 5A , High Density All in One Motor Driver

Version：Rev.1.3

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Contents

1 Introduction

The document is the datasheet for the PM30003V-0405 series.

Users can refer to the "PM30003V User Manual" for further understanding of the functionality of the PM30003V-0405 MCU.

2 Product Description

The PM30003V-0405 MCU utilizes an ARM® Cortex®-M0 core, with a maximum operating frequency of 48 MHz. It features built-in 16 KBytes of Flash and 4 KBytes of SRAM. By configuring the Flash controller registers, interrupt vectors can be remapped within the 16 KBytes space.

With the exception of power and ground pins, all pins of the PM30003V-0405 MCU can function as GPIO, peripheral IO, or external interrupt inputs. In applications with limited pin count, the MCU provides as many pin signals as possible.

The PM30003V-0405 MCU is equipped with multiple communication interfaces:

- **2 route high-speed (up to 6 Mbit/s) UART**
- **1 route high-speed (up to 16 Mbit/s) SPI**

SPI supports full-duplex or half-duplex communication with data lengths ranging from 4 to 16 bits, master/slave mode, TI mode, NSS pulse mode, and automatic CRC check.

- **1 route high-speed (up to 400 Kbit/s) I^2C**

I^2C supports transmission rates of 100/400 kbit/s, master/slave modes, multi-master modes, 7/10-bit addressing, and SMBus protocols. In the MCU halt mode Stop, data reception wake-up is supported.

The PM30003V-0405 MCU features a 16-bit advanced PWM timer (with 4 outputs of PWM, including 3 outputs with dead-time with complementary), a 16-bit general-purpose PWM timer (with 4 outputs of PWM), and a 16-bit basic timer (for timing CPU interrupts).

The PM30003V-0405 MCU has built-in analog circuits: a 12-bit 1 MSPS ADC, an up/down power-on reset circuit POR/PDR/BOR, and an internal reference voltage that is sampled by the ADC on-chip.

The PM30003V-0405 MCU supports a rich set of power consumption modes. In low power consumption mode, this series of MCUs can be automatically woken up by the internal low power consumption timer.

PM30003V-0405 has a built-in three-phase brushless gate driver that can operate at up to 36V to drive P+N structure MOSFET.

PM30003V-0405 has a built-in 3-way half-bridge P+N type MOS, which supports a lower RDS(ON).

PM30003V-0405 MCU operates within a temperature range of -40°C~+105°C and a supply voltage of 7V~24 V, which can meet the requirements of most application environments.

Due to its rich peripheral configuration, the PM30003V-0405 MCU is suitable for varies applications.

- **Motor drive and speed control**
- **UAV flight control and gimbal control**
- **Toy products**
- **Household appliances**
- **Intelligent robot**

2.1 Product Features

- **CPU Core**
  - **ARM® Cortex®-M0**
  - **Maximum clock frequency：48 MHz**
  - **24-bit SysTick Timer**
  - **Supports interrupt vector remapping (configured through the Flash controller's registers)**
- **Operating Voltage Range**
  - **7V ~ 24 V**
- **Operating Temperature Range**
  - **-40°C ~ +105°C**

- **Typical working current:**
  - Run working mode: 2.751 mA@48 MHz@5V
  - Sleep mode: 0.997 mA@48 MHz@5V
  - Stop mode: 373.354 μA@5V（LDO normal operation）
  - Low-power Stop mode: 6.876μA@5V（LDO low power comsuption）
- **16 KByte Flash（64 pages，each page 256 Byte；32-bit data read，32-bit data write）**
  - Flash has data security protection function, which can be set to read protection and write protection respectively
  - 4 KByte SRAM
- **CRC hardware unit**
- **Clock**
  - On-chip high-speed clock HSI: 48MHz
  - On-chip slow clock LSI: 60 kHz
  - GPIO external input clock: 32MHz
- **Reset**
  - Low-level external reset on the NRST pin
  - Reset the window watchdog event WWDG
  - Independent watchdog event IWDG reset
  - Power reset
  - Software reset SW reset
  - Low power management reset
- **GPIO port**
  - Support up to 10 GPIO ports
  - Each GPIO can be used as an external interrupt input
  - Built-in switchable pull-up and pull-down resistors
  - Support open-drain output
  - Output drive capability can be configured
- **Data communication interface**
  - 2-channel high-speed UART with a maximum speed of 6 Mbit/s
  - 1-channel high-speed up to 400 kbit/s I^2C: MCU supports data reception wake-up in Stop mode
  - 1 channel high-speed SPI up to 18 Mbit/s
- **Timer and PWM generator**
  - 1 x 16-bit advanced PWM timer with 4 PWM outputs, 3 complementary outputs with dead zone
  - 1 x 16-bit general-purpose PWM timer with 4 PWM outputs
  - 1 x 16-bit basic timer supporting CPU interrupt
  - 1 x automatic wake-up timer AWUT, which can be used in MCU stop mode
- **On-chip analog circuit**
  - 1 x 12-bit 1 MSPS ADC with up to 7 external analog input channels and 2 internal channels, supporting differential pair input
  - 1 x 5V/50mA LDO with 5% accuracy
  - 2-channel low-offset operational amplifier, supporting millivolt-level signal amplification on current detection resistors
  - 1 x upper/lower power reset circuit
  - 1 x under-voltage reset circuit
  - 1 x internal reference voltage Internal reference voltage is sampled by ADC on chip
- **Three-phase brushless grid driver**
  - Three-phase push-pull gate driver for P+N MOS

- Output 10V VGS for low-side NMOS use
- Input voltage V_{IN} undervoltage protection UVLO
- Built-in straight-through prevention function
- Built-in 500nS dead time
- High-end and low-end channel matching

◆ **MOSFET**
- N-channel：VDS =24V，ID =5A
- P-Channel：VDS =-24V，ID =-5A

◆ **CPU tracing and debugging**
- SWD debugging interface
- ARM® CoreSightTM Debug Component ROM-Table, DWT, BPU
- Customize DBGMCU debug controller low power mode simulation control, debug peripheral clock control, debug and trace interface allocation

◆ **ID identification**
- Each PM30003V-0405 chip provides a unique 96-bit ID

◆ **Meet AEC-Q100 requirements**

2.2 Device Overview

Table 2-1 PM30003V-0405 Series Feature

Product Feature		PM30003V-0405
GPIO		10
Package		TSSOP-25P
working voltage		7V ~ 24 V
Working power		50W
working temperature		-40°C~+105°C
Memory	Flash (Kbyte)	16
	SRAM (Kbyte)	4
CPU	kernel	Cortex®-M0
	working frequency	48MHz
Clock	Internal LSI	60KHz
	Internal HSI	48MHz
	External GPIO clock	32MHz
Timer	Advanced timer	1*（16-bit）：TIM1
	universal timer	1*（16-bit）：TIM2
	Basic timer	1*（16-bit）：TIM6
	System Tick Timer	1
	Automatic Wake-up Timer (AWUT)	1
	Independent Watchdog (IWDG)	1
	Window Watchdog (WWDG)	1
Communication Interface	UART	2
	I^2C	1
	SPI	1
ADC	Number of ADCs and external channels	1(7 external channels)
	Benchmark selection	Internal reference voltage
	ADC sampling rate	1MSPS(12-bit)
	ADC accuracy	12-bit
CRC		1
96-bit UID		1

3 Ordering Information

3.1 Ordering Information

Table 3-1 PM30003V-0405 Product Ordering Information

Order number	Marking ID	Package	Description
PM30003V-0405BQ	PM30003V 0405BYMDNN	TSSOP-25P	Halogen Free RoHS compliant in T&R, 2500pcs/Reel

3.2 Marking Information

Table 3-2 PM30003V-0405 Product Marking Information

Marking	Package	Definition
PM30003V 0405BYMDNN	TSSOP-25P	Product code : PM30003V, Voltage/Current/Package code : 0405B Y : Year code M : Month code D : Day code NN: Serial Number

4 Function Introduction

4.1 Block Diagram

The ARM® Cortex®-M0 processor is an embedded 32-bit RISC processor. It is a low-cost, low-power MCU platform that provides excellent computing performance and advanced interrupt system response. PM30003V-0405 has a built-in Cortex®-M0 core and is compatible with ARM tools and software.

The system architecture of the PM30003V-0405 MCU is illustrated in Figure 4-1

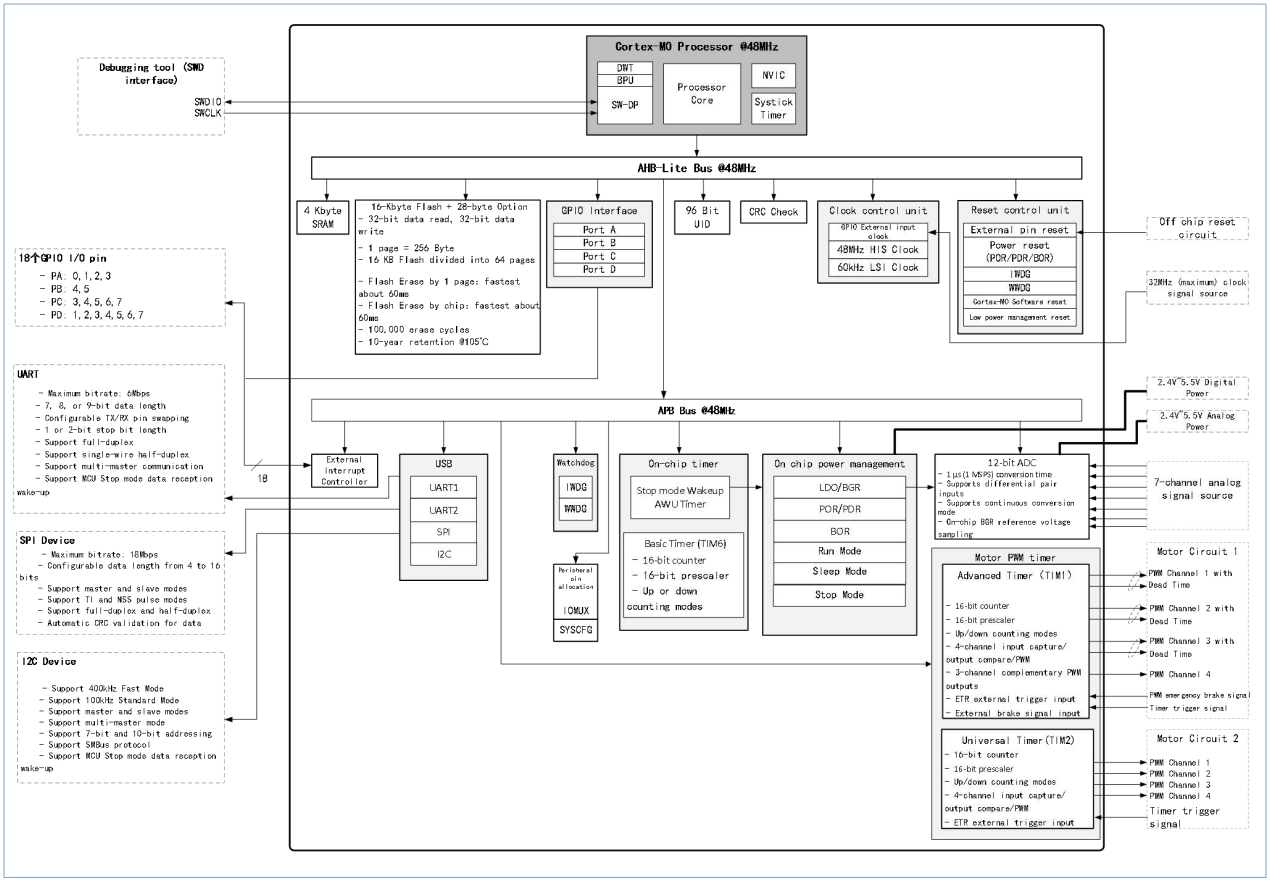
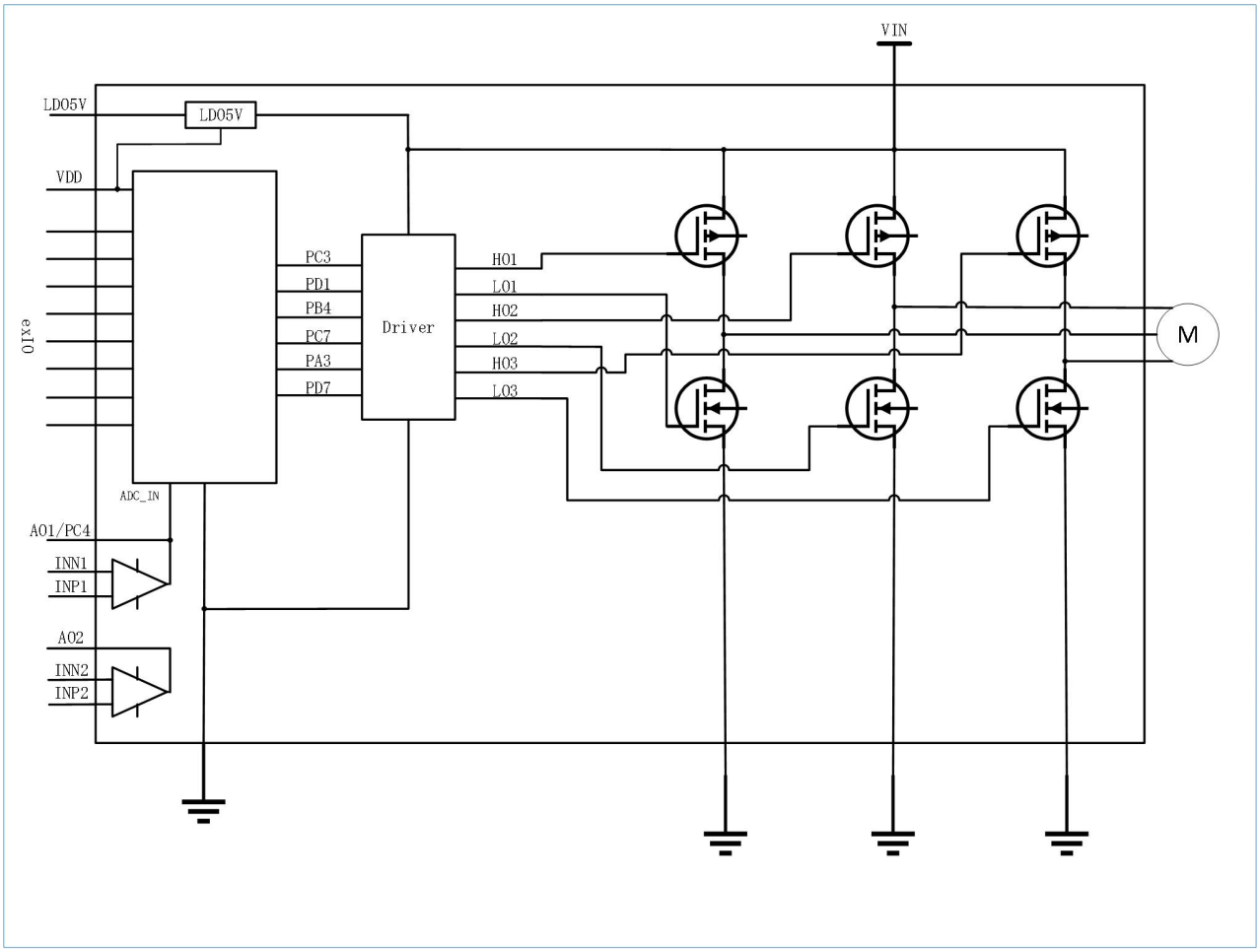


Figure 4- 1 PM30003V-0405 Block Diagram

4.2 System Block Diagram

PM30003V-0405 is a highly integrated chip that internally integrates an MCU, Driver, 5V LDO, and three sets of P+N MOS. The system block diagram illustrates the internal resources and connections of PM30003V-0405.



4.3 Memory Mapping Configuration

The memory map of the PM30003V-0405 MCU is illustrated in the following figure:

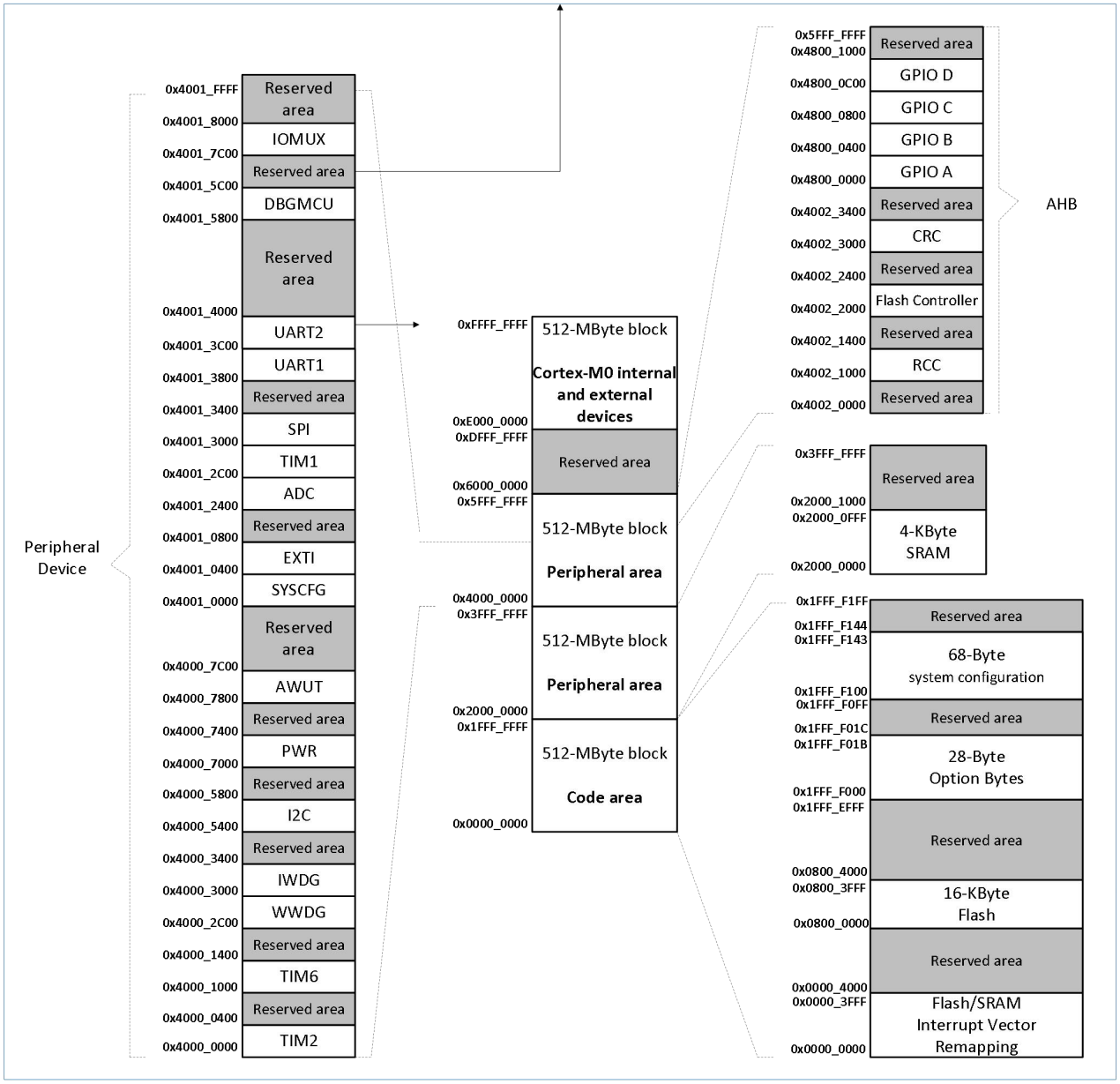


Figure 4- 2 PM30003V-0405 Memory Mapping

4.4 Memory

4.4.1 Flash

The chip integrates up to 16Kbyte of Flash memory, which is used to store programs and data.

By configuring the registers of the Flash controller, the remapping of interrupt vectors can be achieved.

4.4.2 SRAM

The chip integrates 4Kbyte SRAM inside, supporting word, halfword, and byte read and write access. The CPU can perform fast read and write access with zero wait cycles, which can meet the needs of most applications.

4.5 CRC calculation unit

Cyclic Redundancy Check (CRC) is used to verify the integrity of data transmission or data storage. An independent CRC hardware computing unit is integrated inside the device, which reduces the burden on user applications and provides accelerated processing capabilities.

The CRC calculation unit calculates the signature of the software during operation and compares it with the reference signature generated during linking and stored at a specified storage address.

4.6 Power Supply Plan

PM30003V-0405 has two sets of power supplies V_{IN} and LDO5V. V_{IN} provides input 7-24V and outputs 5V to the LDO5V pin, and supplies power to VDD/VDDA.

4.7 Power Monitor

The device integrates a power-on reset POR/power-down reset PDR circuit with an undervoltage reset BOR, which is turned off by default. This circuit is always in operation to ensure that the system works when the power supply exceeds 2.4V. When VDD is lower than the POR/PDR threshold, the device is placed in the reset state without having to use an external reset circuit.

4.8 Low power consumption mode

The device supports multiple power consumption modes, achieving an optimal balance between low power consumption, short start-up time, and multiple wake-up events.

- **Sleep Mode**

In sleep mode, only the CPU stops working, and all peripherals are in working state and can wake up the CPU when an interrupt/event occurs.

- **Stop Mode**

The lowest power consumption can be achieved in the halt mode while maintaining the contents of SRAM and registers without loss. In the shutdown mode, all clocks in the kernel domain are turned off, and the RC oscillator of the HSI is turned off. The MCU can be woken up from the halt mode by any signal configured as EXTI. The EXTI signal can be any external I/O port.

4.9 Reset

The device supports two reset modes: system reset and power reset.

4.9.1 System Reset

In addition to the reset flag bit in the RCC_CSR register of the clock controller and the registers in the backup area, system reset will reset all registers to their reset state.

Users can identify the source of the reset event by viewing the reset status flag bit in the RCC_CSR control status register.

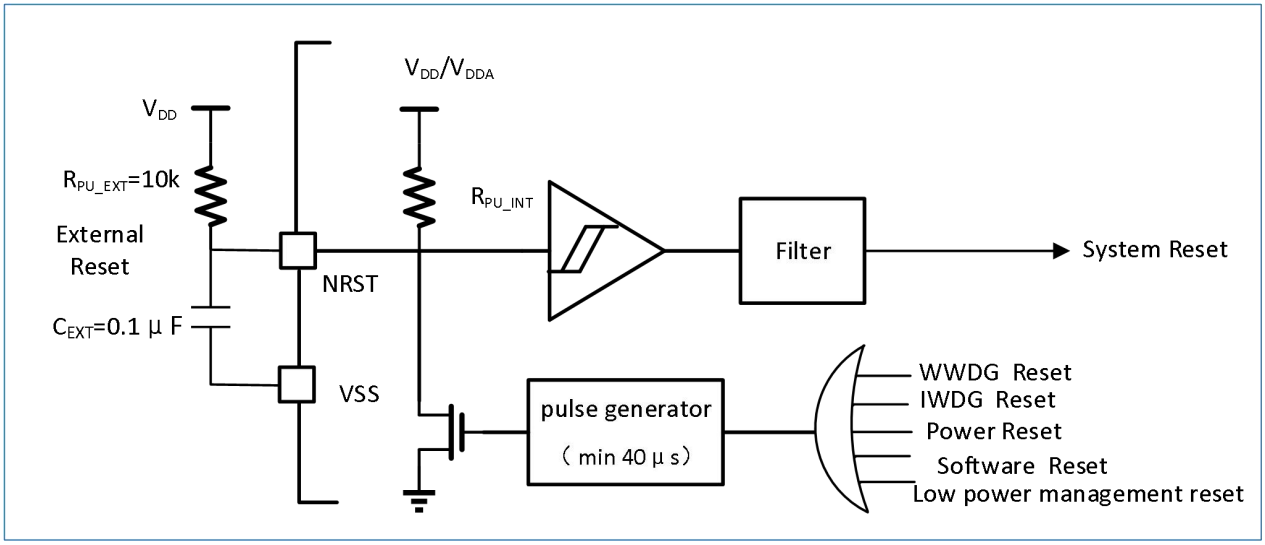


Figure 4-3 Reset Circuit

When any of the following events occurs, a system reset will be generated:

- **Low-level external reset on the NRST pin**
- **Window watchdog count termination WWDG reset**
- **Independent watchdog count termination IWDG reset**
- **Power reset**
- **Software Reset SW Reset: Software reset can be achieved by setting the SYSRESETREQ bit in the Cortex™-M0 interrupt application and reset control register to '1'.**
- **Low power management reset**

The reset source will eventually act on the NRST pin and remain low during the reset process. The reset entry vector is fixed at address 0x0000 0004. The reset signal inside the chip will be output on the NRST pin. The pulse generator ensures that each internal reset source has a minimum pulse delay of 40μs. When the NRST pin is pulled low to generate an external reset, it will generate a reset pulse.

4.9.2 Power reset

When any of the following events occurs, a power reset will occur:

- **Power-on/power-down reset POR/PDR**
- **Under-voltage reset BOR**

The device integrates a power-on reset POR/power-down reset PDR/under-voltage reset BOR circuit. The POR/PDR circuit is always in working state BOR is turned off by default to ensure the system works normally when the power supply exceeds 2.4 V. When VDD is less than the BOR/POR/PDR threshold, the MCU will be reset without the need for an external reset circuit.

4.10 Clock and clock tree

The following is the clock tree of the PM30003V-0405：

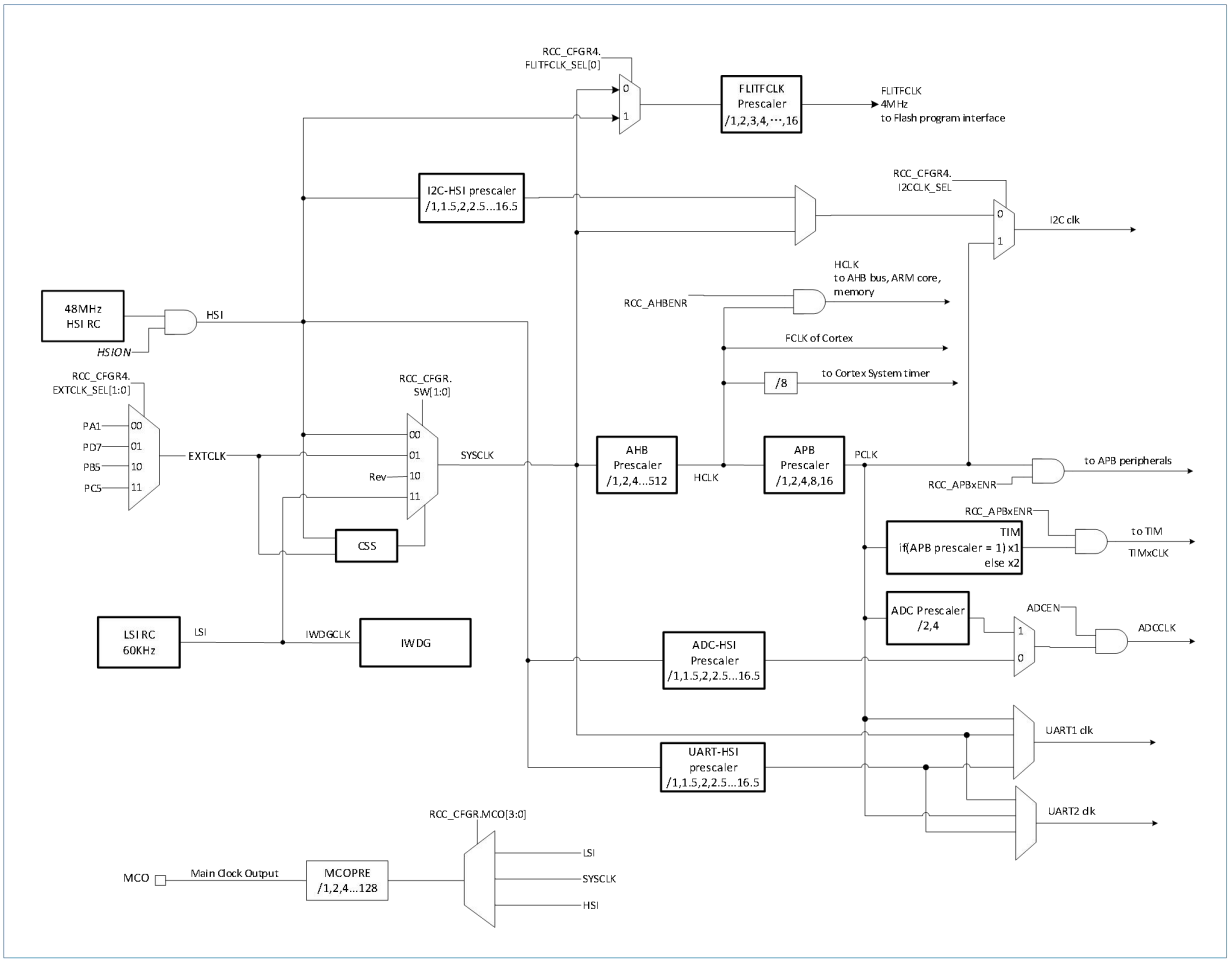


Figure 4-4 PM30003V-0405 Clock Tree

As shown in Figure 4-4, PM30003V-0405 supports multiple clock sources to drive system clocks:

- **Internal high-speed clock HSI: 48MHz**
- **Internal low-speed clock LSI: 60kHz**
- **GPIO external input clock: 32MHz maximum**

Each clock source can be turned on or off independently. When they are not in use, they can be turned off to reduce power consumption. There are multiple frequency dividers available for configuring the AHB and APB clock domains, with a maximum clock frequency of 48 MHz for both AHB and APB domains. The Cortex system timer is driven by the AHB clock HCLK, which can be directly driven by the AHB/8 clock frequency through the Cortex SysTick configuration bit.

All peripheral clocks are driven by their respective bus clock HCLK or PCLK, except for the following:

The clock for the flash programming interface, FLITFCLK, is driven by the HSI clock or SYSCLK, and is selected by software.

The I^2C clock is selected by software from one of the following clock sources:

- **SYSCLK**
- **HSI 48 MHz is divided by the I^2C-HSI frequency divider**
- **APB Clock（PCLK）**

The FCLK of Cortex is directly provided by the AHB clock HCLK.

AHB bus, ARM core, and memory are directly provided by the AHB clock HCLK.

The ADC clock is selected by software from one of the following clocks:

- **APB clock PCLK is divided by ADC frequency divider 2/4**

- **HSI 48 MHz is divided by ADC-HSI frequency divider**

The clock for UART1/UART2 is selected by software from one of the following clock sources:

- **PCLK**
- **SYSCLK**
- **HSI 48 MHz RC oscillator clock through UART-HSI divider clock**

The Timer clock is provided by the APB clock PCLK or APB clock PCLK2 multiplied by 2, and is set by software and executed by hardware.

The RCC divides the AHB clock HCLK8 and uses the result as the external clock for the Cortex system timer SysTick. By setting the SysTick control and status registers, you can select the HCLK/8 clock as the SysTick clock.

4.11 SYSCFG

The device has a set of configuration registers, and the main purpose of the system configuration registers is as follows:

- **Remapping of the system boot area.**
- **Manage the connection between external interrupts and GPIO.**
- **Managing the reliability characteristics of the system.**

4.12 GPIO

Each GPIO pin can be configured by software to output push-pull or open drain, input floating input, pull-up input or pull-down input, or other peripheral function ports. Most GPIO pins are shared with digital or analog peripherals. All GPIO pins have high current passing capability. The peripheral function of the I/O pin can be locked as needed to avoid accidental writing to the I/O register.

4.13 Interruptions and Events

4.13.1 NVIC

The device has a built-in nested vector interrupt controller NVIC, which can handle up to 22 maskable interrupt channels, excluding 16 interrupt lines for Cortex®-M0 and 4 interrupt priorities. This module provides flexible interrupt management with minimal interrupt latency.

- **The tightly coupled NVIC can achieve low-latency interrupt response processing**
- **Interrupt vector entry address directly enters the kernel**
- **Close-coupled NVIC interface**
- **Allow early processing of interrupts**
- **Handle late higher priority interrupts**
- **Support for breaking the tail link function**
- **Automatically save processor state**
- **Automatically resume when interrupted, without additional instruction overhead**

4.13.2 EXTI

The extended interrupt/event controller contains 11 edge detection interrupt lines for generating interrupt/event requests and waking up the system. Each interrupt line can be configured independently to select triggering events on the rising edge, falling edge, or both edges, and can be individually masked. The pending register is used to maintain the status of the interrupt request. EXTI can detect external interrupt line signals with pulse widths less than the internal clock cycle. According to whether the interrupt/event trigger edge can be configured, EXTI can be divided into two categories: configurable EXTI (abbreviated as configurable EXTI) and fixed EXTI (abbreviated as fixed EXTI). There can be up to 9 configurable interrupt lines.

- **EXTI 0 ~ EXTI 7 are connected to IO, and the remaining EXTI ports are connected to the following events:**
- **EXTI 8 connects to the AWD event of ADC**

- **EXTI 10 connected to I²C Wakeup event**
- **EXTI 11 connected to the Wakeup event of AWU**

EXTI8 and EXTI10 are fixed events without RTSR, FTSR, SWIER, and PR registers. They can only collect the rising edge of events in Stop mode to generate ERQ and IRQ signals to wake up the system. The corresponding interrupt control and status bits are stored in the peripheral module that generates the event source.

4.14 ADC

The ADC characteristics of the device are as follows:

- **There are only 9 channels in total. Among them, AIN0 ~ AIN6 are external channels connected to IO; AIN7 is an internal channel that connects to the internal PMU for power supply voltage calibration within the chip. AIN8 is an internal channel that connects to the internal reference voltage.**
- **Support differential input mode, AIN0 and AIN1, AIN2 and AIN3, AIN4 and AIN5 form three groups of differential inputs. When the ADC is configured for differential input mode, AIN7 and AIN8 are ADC channels for sampling internal PMU and reference voltage, and AIN6, AIN7, and AIN8 are not available.**
- **Only supports a sampling resolution of 12-bit ADC.**

4.15 Timer

PM30003V-0405 includes an advanced timer, a general timer, and a basic timer. The timer function is defined as shown in Table below.

Table 4- 1 Definition of Timer Function

Type	Timer Name	Counter Resolution	Counter Type	Prescaler Factor	DMA Request	Emergency Brake Input	Capture/Compare Channel	Complementary Output
Advanced timer	TIM1	16-bit	Increment, decrement, increment/decrement	1~65536	None	Yes	4	3
General Timer	TIM2	16-bit	Increment, Decrement, Increment/Decrement	1~65536	None	None	4	None
Basic Timer	TIM6	16-bit	Increment and Decrement	1~65536	None	None	None	None

4.15.1 Advanced Timer

The device integrates an advanced timer TIM1.

The advanced timer TIM1 can be used as a three-phase PWM generator with six channels, or as a complete general-purpose timer. Four independent channels can be used for:

- **Input capture**
- **Output comparison**
- **Generates PWM edge or center alignment patterns**
- **Single pulse output**
- **Complementary PWM output with programmable dead zone insertion function.**

When the advanced timer is configured as a 16-bit basic timer, it has the same function as the basic timer. When configured as a 16-bit PWM generator, it has full modulation capability from 0 to 100%. Due to the same internal structure and most functions as the general timer, the advanced timer can operate in conjunction with the general timer through the timer link function to provide synchronization or event link functions.

In debug mode, the counter can be frozen.

4.15.2 General Timer

The device integrates a 4-channel general-purpose timer TIM2.

The general-purpose timer can generate PWM outputs or serve as a simple time reference. TIM2 has a 16-bit auto-reload up/down counter and a 16-bit prescaler. In debug mode, this counter can be frozen.

TIM2 can work with advanced control timers through timer linking functions to provide synchronization or event linking capabilities and can handle quadrature incremental encoder signals and digital outputs from 1 to 3 Hall effect sensors.

4.15.3 Basic Timer

The device integrates a basic timer TIM6.

The basic timer has a built-in 16-bit counter and 16-bit prescaler, and supports increment or decrement counting methods. The basic timer is used to generate CPU timing interrupt requests. In debug mode, the counter can be frozen.

4.16 AWUT Timer

The device integrates an automatic wake-up AWUT timer. The AWUT timer is used to count time in the MCU stop mode and generate an interrupt to wake up the MCU. AWUT has a built-in ultra-low power 22-bit timer, and its working clock can be configured as a GPIO input clock or an on-chip slow clock LSI. The AWUT timer uses a countdown method.

4.17 Independent Watchdog（IWDG）

The independent watchdog is clocked by an internal independent RC oscillator LSI with a 12-bit down counter and an 8-bit prescaler. Since the RC oscillator is independent of the main clock, it can operate in a shutdown mode. It can be used as a watchdog to reset the device when a problem occurs, or as a free-running timer to provide timeout management for applications. It can be configured in hardware or software through the option byte. In debug mode, this counter can be frozen.

By configuring the IWDG_WINR register, the IWDG can operate in window mode.

4.18 Window Watchdog（WWDG）

The window watchdog has a 7-bit decrement counter inside. The counter can be set to free-running mode or used as a watchdog to reset the entire system in the event of a system crash. The window watchdog is driven by the main clock and has the function of early warning interruption. In debug mode, this counter can be frozen.

4.19 System Tick Timer

The System Tick timer is dedicated to the operating system and can be used as a standard decrement counter. It has the following characteristics.

- **24-bit down counter**
- **reload function**
  When the counter reaches 0, a maskable interrupt can be generated.
- **Programmable clock source**

4.20 I^2C Bus

A single I^2C bus interface, capable of operating in master and slave modes, supports both standard and fast modes. The I^2C interface supports 7-bit or 10-bit addressing, and supports dual slave address addressing when operating in 7-bit slave mode. The I^2C interface has a built-in hardware CRC generator/checker and supports SMBus V2.0/PMBus bus.

Table 4-2 I²C Characteristics

I²C Characteristics	I²C
Master/Slave Mode	Supported
Multi-host mode	Supported
Standard/fast mode	Supported
7/10-bit addressing mode	Supported
Broadcast call	Supported
Event management	Supported
Clock extension	Supported
Software reset	Supported
Digital and analog filters	Supported
SMBUS2.0	Supported
PMBUS1.1	Supported
Independent clock	Supported
Wake up from the Stop mode	Supported

4.21 Universal asynchronous receiver transmitter（UART）

The device has two universal asynchronous receiver transmitters UART1/UART2 built in. They provide hardware management for multiprocessor communication modes and single-wire half-duplex communication modes, with clock domains independent of the CPU clock.

Table 4-3 UART characteristics

UART Mode/Characteristics	UART1/2
Data word length	7/8/9 bits
Multi-processor communication	Supported
Single-wire half-duplex communication	Supported
Dual clock domain	Supported

4.22 Serial Peripheral Interface（SPI）

It has one SPI interface with a communication rate of up to 18 Mbit/s, supporting slave and master modes, full-duplex and half-duplex communication modes. SPI can use a 3-bit prescaler to generate 8 main mode frequencies, and each frame can be configured with 4-bit to 16-bit data. SPI supports CRC, TI mode, etc., and its characteristics are shown in Table below.

Table 4-4 SPI Characteristics

SPI Characteristics	SPI
Hardware CRC calculation	Supported
RX/TX FIFO	Supported
NSS pulse mode	Supported
TI mode	Supported

4.23 Operational Amplifier

The chip has two low offset operational amplifiers built in.

4.24 Built-in Driver

The chip has a built-in three-phase brushless gate driver for driving the P+N structure MOSFET. The built-in input voltage V_{IN} has an under-voltage protection UVLO function, which can effectively prevent the power tube from working at too low a voltage. At the same time, built-in pass-through prevention and dead time are used to prevent the driven high and low side MOSFETs from passing through, effectively protecting the power device.

4.25 Input and Output Truth Table

The input pins LINx and HINx control the output status of LOx and HOx. The following Table shows the logical relationship between input and output:

Table 4- 5 Input and Output Truth Table

LINx	HINx	LOx	HOx	Function
0	0	GND	V_{IN}	External NMOS and PMOS are turned off simultaneously
0	1	GND	V_{IN}-10V	The external NMOS is turned off and the PMOS is turned on
1	0	10V	V_{IN}	External NMOS is on, PMOS is off
1	1	GND	V_{IN}	External NMOS and PMOS are turned off simultaneously

4.25.1 Straight-through Prevention Function

The internal design is specifically designed to prevent the power tube from being directly connected to the protection circuit, effectively preventing damage to the power tube caused by interference with high- and low-side input signals.

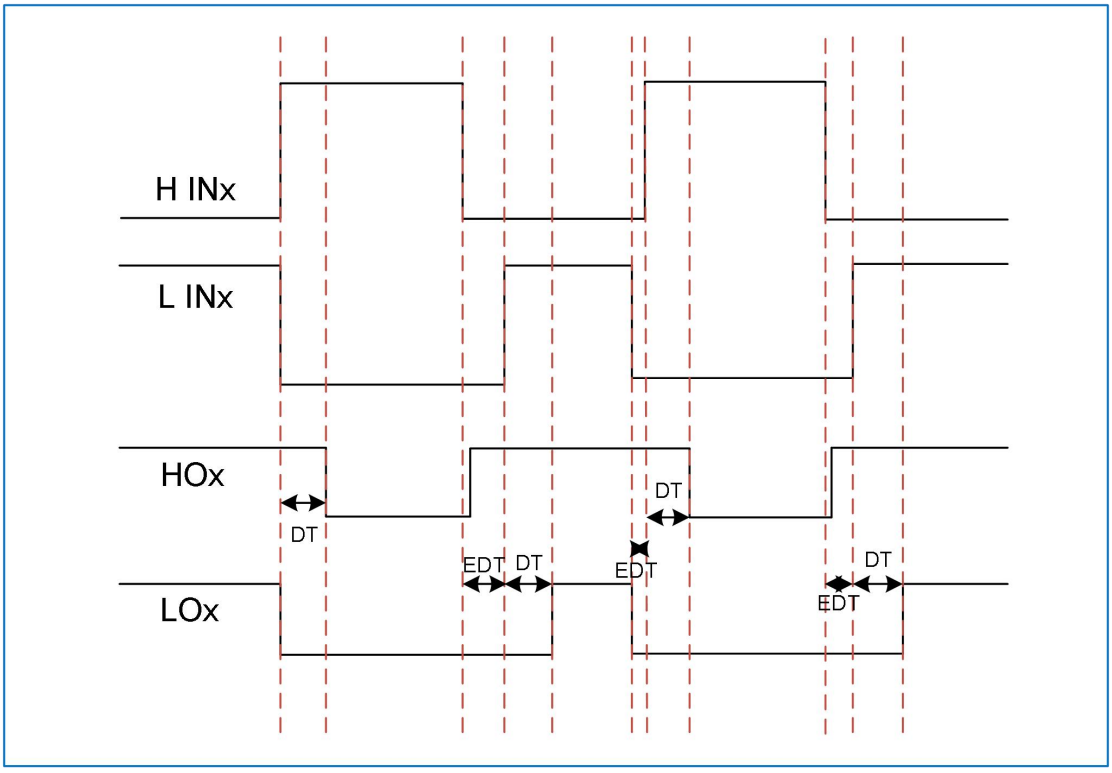


Figure 4- 5 Straight-through Prevention Function

4.25.2 Dead Zone Function

A fixed dead time protection circuit is set up inside. During the dead time, the high side is set to high level and the low side output is set to low level. The dead time must be set to ensure that one power tube is turned off before another power tube is turned on, effectively preventing the occurrence of direct connection between the upper and

lower power tubes. If the logic input has an external dead time EDT set, the dead time is equal to the external dead time EDT plus the internally set dead time DT.

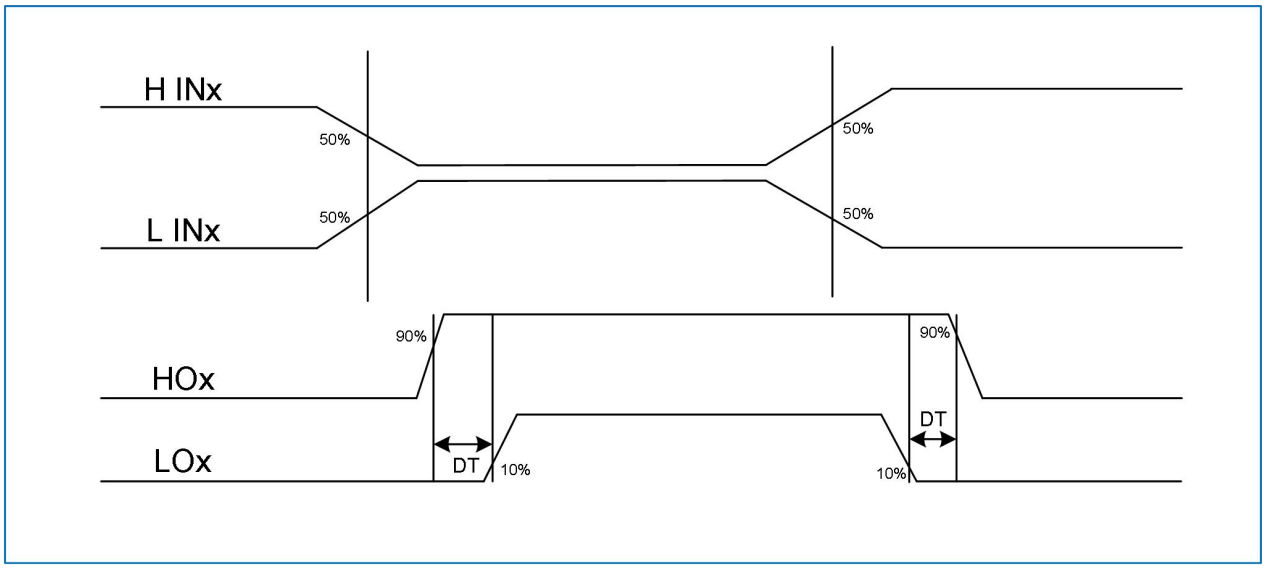


Figure 4- 6 Dead Time

4.26 LDO

The chip has a built-in 5V/50mA LDO.

4.27 MOSFET

The chip has 3-way P+N mode RDS(ON) smaller half-bridge MOS.

4.28 96-bit UID

The reference number provided by the 96-bit product unique identity UID is unique to any one of the PM30003V-0405 chips in any situation. The user cannot modify this identity identifier. According to different usages, the 96-bit UID can be read in units of byte 8 bits, half word 16 bits, or full word 32 bits. 96-bit UID is suitable for:

- **Used as a serial number, such as a USB character serial number or other terminal applications.**
- **It is used as a password. When writing flash memory, this UID is used in conjunction with software encryption and decryption algorithms to improve the security of the code within the flash memory.**
- **Used to activate the bootstrapping process with security mechanisms.**

4.29 Debugging Interface

The SWJ-DP interface embedded with ARM combines a single-wire debug interface, allowing for the connection of the serial single-wire debug interfaces SWDIO and SWCLK.

5 Electrical Characteristics

5.1 Power Supply

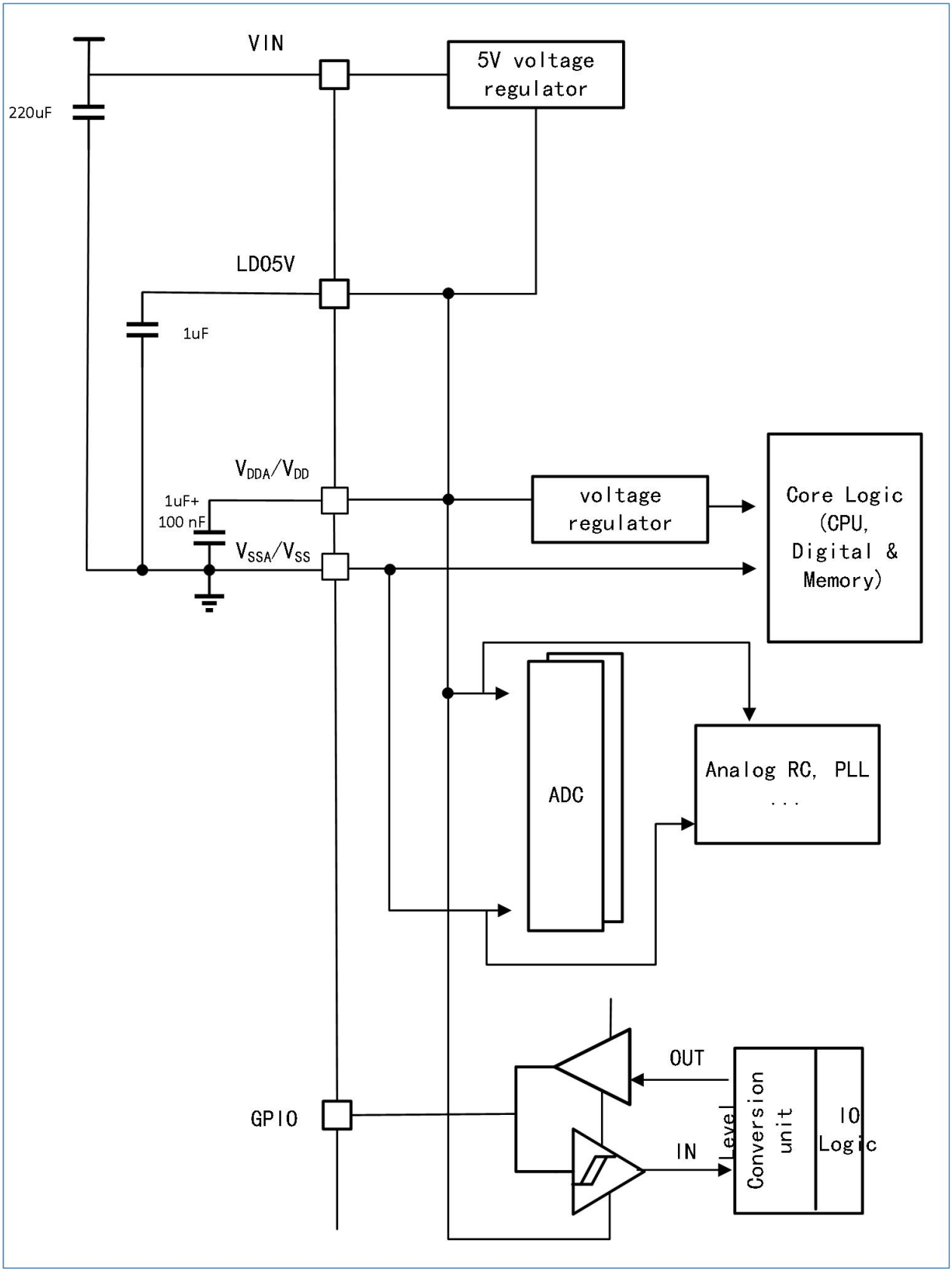


Figure 5-1 Power Supply Reference Circuit

5.2 Maximum Absolute Ratings

The maximum rated value is only a short-term pressure value.

Notes：

- Do not operate the chip at this value or any other conditions exceeding the recommended values.
- Refer to Tables 5-1 to 5-3 for the maximum rated values of the chip. Exceeding the maximum rated values may result in permanent damage to the chip.
- Operating for prolonged periods at maximum rated values may affect the chip's reliability.

5.2.1 Limit Voltage Characteristics

Table 5-1 Limit Voltage Characteristics

Symbol	Description	Minimum	Maximum	Unit
V_{IN}	Voltage Range	6	40	V
$V_{INP1,2}$	Low Offset Operational Amplifier Positive Input Voltage Rang	-0.3	V_{LDO5V}	
$V_{INN1,2}$	Low Offset Operational Amplifier Negative Input Voltage Range	-0.3	V_{LDO5V}	
ESD	HBM	-	-	
	ESD	-	-	

5.2.2 Extreme Current Characteristics

Table 5-2 Extreme Current Characteristic

Voltage Range	Voltage Range	Voltage Range	Voltage Range
I_{VIN}	Maximum current flowing through V_{IN}	5000	
I_{VDD}	Total current passing through V_{DD}/V_{DDA} power lines (supply current)(1)	105	mA
I_{VSS}	Total current passing through V_{SS} ground lines (drain current) (1)	105	
I_{IO}	Output sinking current on any I/O and control pin	30	
	Output pulling current on any I/O and control pin	30	
$I_{INJ(PIN)}$ (2)	Injection current on I/O pins (3)	-5/+0	
$\Sigma I_{INJ(PIN)}$	Total injection current on all I/O and control pins (4)	-25/+0	

(1). All power（V_{DD}，V_{DDA}）and ground（V_{SS}，V_{SSA}）pins must always be connected to an external power supply system within the allowable range.

(2). Reverse injection current can interfere with the analog performance of the device.

(3). When $V_{IN} > V_{DD}$,there is a forward injection current; When $V_{IN} < V_{SS}$,there is a reverse injection current. The absolute value of the injection current must not exceed the specified range.

(4). When several I/O pins have injection currents simultaneously, the maximum value of $\sum I_{INJ(PIN)}$ is the sum of the instantaneous absolute values of the forward and reverse injection currents.

5.2.3 Limit Temperature Characteristics

Table 5-3 Limit Temperature Characteristic

Symbol	Description	Minimum	Maximum	Unit
T_{STG}	Storage temperature range	-55	130	°C
T_J	Maximum junction temperature	-45	125	°C

5.3 Operating Parameters

5.3.1 Recommended Operating Conditions

Table 5-4 Recommended Operating Condition

Symbol	Description	Minimum	Typical Value	Maximum	Unit
V_{IN}	Power supply voltage range	7		24	V
I_{VIN}	V_{IN} operating current		3000		mA
$V_{LDO5Vout}$(1)	5V LDO output voltage range	4.5		5.5	V
$I_{LDO5Vout}$	5V LDO output current range			50	mA
$V_{AO1,2}$(2)	Low offset op-amp output voltage range	0		V_{LDO5V}	V
$V_{INP1,2}$(2)	Low offset op-amp positive input voltage range	0		V_{LDO5V}	V
$V_{INN1,2}$(2)	Negative input voltage range of low offset operational amplifier	0		V_{LDO5V}	V
f_{HCLK}	Internal APB Clock Frequency	-		48	MHz
f_{PCLK1}	Internal APB1 Clock Frequency	-		48	
T_A	Operating Temperature	-40		105	°C

(1). V_{DDA} and V_{DD} are Internally Connected.

5.3.2 On/Off Reset Characteristics

Table 5-5 On/Off Reset Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
$V_{POR/PDR}$ (1)	On/Off reset threshold	Falling edge	1.68	1.80	1.93	V
		Rising edge	1.85	1.96	2.07	V
$V_{PDRhyst}$	PDR hysteresis	-	140	160	170	mV
$t_{RSTTEMPO}$ (2)	Reset time	-	-	2	-	ms

(1) PDR and POR only monitor V_{DD}.

(2) Design guarantee.

5.3.3 Under-voltage Reset Characteristics

Table 5-6 Under-voltage Reset Characteristics

Symbol	Parameter	Condition (-40~105℃)	Minimum	Typical Value	Maximum	Unit
V_{BOR}(1)	BOR Detection Level Selection (V_{DD} Rising Edge)	V_{BOR1}	2.62	2.85	3.07	
		V_{BOR2}	3.04	3.21	3.53	
		V_{BOR3}	3.45	3.64	4.01	
		V_{BOR4}	3.89	4.04	4.46	
		V_{BOR5}	4.30	4.57	5.01	
		V_{BOR6}	4.80	5.03	5.49	
		V_{BOR7}	5.23	5.49	5.97	
	BOR Detection Level Selection (V_{DD} Falling Edge)	V_{BOR1}	2.46	2.59	2.83	
		V_{BOR2}	2.84	2.99	3.26	
		V_{BOR3}	3.24	3.40	3.70	
		V_{BOR4}	3.68	3.80	4.14	
		V_{BOR5}	4.06	4.19	4.58	
		V_{BOR6}	4.46	4.62	5.03	
		V_{BOR7}	4.84	5.05	5.48	
t_{BORRST}(2)	Effective Time	-	-	10	-	μs

(1) BOR only monitors V_{DD}.

(2) Design guarantee.

5.3.4 Internal Reference Voltage

Table 5-7 Internal Reference Voltage Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
V_{REFINT}	Internal reference voltage	-40 ~ 105°C	-	1.2	-	V

5.3.5 Operating Current Characteristics

Table 5-8 Operating current characteristics

Mode	Condition	Parameter	V_{DD}=5V			Unit
			-40°C	25°C	105°C	
Run Mode	SYSCLK = HSI48 MHz; All IOs are configured to high impedance state; Except for Flash, SRAM and RCC, all other peripherals are turned off;	Working current	2.704	2.751	2.782	mA

Mode	Condition	Parameter	V_{DD}=5V			Unit
			-40°C	25°C	105°C	
	APB clock enable; To retrieve values from Flash, Flash reads for 2 waiting cycles.					
Sleep Mode	SYSCLK= 48MHz; AHB/APB is turned off; Turn off the core clock; All IOs are configured to high impedance state; Except for Flash, SRAM and RCC, other peripherals are turned off; RAM and peripheral data are retained.	Working current	1.227	1.361	1.390	mA
		Wake up time	-	2.72	-	μs
	SYSCLK= 60kHz; All IOs are configured to high impedance state; Except for Flash, SRAM and RCC, all other peripherals are turned off; APB clock is prohibited; Get value from Flash, Flash reads 0 waiting cycles	Working current	0.875	0.997	1.014	mA
		Wake up time	-	1.63	-	ms
Stop Mode	All Core domain clocks stop; HSI and LSI oscillators are turned off; LDO operates in normal mode; All IOs are configured to high impedance state; All peripherals are turned off except for AWUT;	Working current	343.475	373.354	453.543	μA
		Wake up time	-	32.4	-	μs
Low-Power Stop Mode	All clocks stop; HSI and LSI oscillators are turned off; LDO operates in low power consumption mode; All IO configurations are set to high impedance state; All peripherals including AWUT are turned off;	Working current	5.705	6.876	27.260	μA
		Wake up time	-	125.5	-	μs

5.3.6 Internal High-speed HSI Clock Characteristics

Table 5- 9 HSI Clock Characteristics

Symbol	Parameter	Condition		Minimum	Typical Value	Maximum	Unit
f_{HSI}(1)	Clock frequency	-		-	48	-	MHz
DuCy $_{(HSI)}$ (1)	Duty cycle	-		45	-	55	%
ACC $_{(HSI)}$	Oscillator accuracy	After the user calibrates the RCC_CR register		-1	-	1	%
		Factory calibration	T_A= –40 ~ +105°C	-1.6	-	1.6	%
$T_{su\ (HSI)}$ (1)	Oscillator start time	$V_{SS} \le V_{IN} \le V_{DD}$		-	5	8	μs

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
$I_{DD\ (HSI)}$ (1)	Power consumption of oscillator	-	-	70	85	μA

(1) Design guarantee.

5.3.7 Internal Low-speed LSI Clock Characteristics

Table 5-10 LSI Clock Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
f_{LSI}	Clock frequency	-	-	60	-	kHz
$T_{su\ (LSI)}$ (1)	Oscillator start time	$V_{SS} \le V_{IN} \le V_{DD}$	-	50	150	μs
$I_{DD\ (LSI)}$ (1)	Power consumption of oscillator	-	-	0.2	-	μA

(1) Design guarantee.

5.3.8 GPIO External clock input characteristics

Table 5-11 GPIO External clock input characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
f_{GPIO_ext}	User external clock source frequency	-	0	-	32	MHz
DuCy $_{(HSE)}$ (1)	Duty cycle	-	45	-	55	%

(1) Design guarantee.

5.3.9 Flash Memory Characteristics

Table 5-12 Flash Memory Characteristics

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit
T_{PROG}	Half-word write time	-	20	-	μs
T_{ERASE}	Page erase time	30	60	80	ms
	Chip erase time	30	60	80	ms
I_{DDPROG}	Half-word write current	-	-	5	mA
$I_{DDERASE}$	Page/chip erase current	-	-	2	mA
I_{DDREAD}	Read current @24MH	-	2	3	mA
	Read current @1MHz	-	0.25	0.4	mA
N_{END}	Write/erase endurance	100	-	-	k times
t_{RET}	Data retention time	10	-	-	years

5.3.10 IO Input Pin Characteristics

Table 5-13 IO Input Pin Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
V_{IH}	Input High Level	-	0.65*V_{DD}	-	-	V
V_{IL}	Input Low Level	-	-	-	0.2*V_{DD}	V
V_{IHhys}	Input High Level	V_{DD}=5V	2.31	-	-	V
V_{ILhys}	Input Low Level	V_{DD}=5V	-	-	2.23	V
V_{hys}	Schmitt Trigger Hysteresis Voltage	V_{DD}=5V	80	-	-	mV
I_{lkg}	Input Leakage Current	V_{DD}=5V； 0<V_{IN}<5V	-	5	-	nA
		V_{DD}=3.3V； V_{IN}=5V	-	5	-	nA
R_{PU}	Pull-up Resistor	-	-	33	-	KΩ
R_{PD}	Pull-down Resistor	-	-	33	-	KΩ
C_{IO}(1)	I/O Pin Capacitance	-	-	-	10	pF

(1) Design guarantee.

5.3.11 IO Output Pin Characteristics

Table 5-14 IO Output Pin Characteristics

Symbol	Parameter	Condition	Minimum	Typical Value	Maximum	Unit
V_{OH}	Output High Level	2.4V ≤ V_{DD} ≤5.5V	0.8*V_{DD}			V
V_{OL}	Output Low Level	2.4V ≤ V_{DD} ≤5.5V			0.2* V_{DD}	V

Table 5-15 IO Output Driver Pin Characteristics

Driver gear	V_{DD}=3.3V		V_{DD}=5V		Unit
	Inject current	Pull-up current	Inject current	Pull-up current	
Level1	4.17	5.24	7.86	17.83	mA
Level2	16.86	13.64	28.29	45.89	mA
Level3	23.73	16.78	39.82	59.93	mA

5.3.12 NRST Reset Pin Characteristics

The NRST pin integrates a pull-up resistor inside, and the peripheral application circuit can be connected to any circuit or an external RC circuit.

Table 5-16 NRST Pin Input Characteristics

Symbol	Parameter	Minimum	Typical Value	Maximum	Unit
T_{Noise}	Low-level is ignored	-	-	80	ns

5.3.13 TIM Counter Characteristics

Table 5-17 TIM Pin Input Characteristics (1)

Symbol	Parameter	Minimum	Maximum	Unit
F_{EXT}	External clock frequency for Timer	-	$f_{TIMxCLK}/2$	MHz

(1). Design guarantee, $f_{TIMxCLK}$ = 48MHz.

5.3.14 ADC Characteristics

Table 5-18 ADC Characteristics

Program	Description	Condition	Minimum	Typical Value	Maximum	Unit
V_{DDA}	Analog supply voltage when ADC is on	-	2.4	5	5.5	V
VREFP	Positive reference voltage	-	2.4	5	5.5	V
VREFN	Negative reference voltage	-	0	0	0	V
f_{ADC}	ADC clock frequency	-	0.3	12	28	MHz
f_S (1)	sampling frequency	f_{ADC} = 12 MHz	-	1	-	MHz
f_{TRIG} (1)	External trigger frequency	f_{ADC} = 12 MHz	-	-	706	kHz
			17	-	-	Cycles
V_{AIN}	Conversion voltage range	-	VREFN	-	VREFP	V
R_{AIN} (1)	External input impedance	Please refer to Table 5-19 for details				kΩ
R_{ADC} (1)	Sampling switch resistance	-	-	-	2	kΩ
C_{ADC} (1)	sample-and-hold capacitor	-	-	5	-	pF
JitterADC	ADC trigger conversion jitter	-	-	1	-	Cycles
t_S (1)	Sampling time	f_{ADC} = 12 MHz	1.5	-	239	Cycles
t_{CONV} (1)	The total conversion time includes the sampling time	f_{ADC} = 12 MHz 12bit resolution	14	-	252	Cycles

(1) Design guarantee.

(2) The specified values only include the ADC timing. It does not include the delay of register access.
The calculation formula for the maximum input impedance RAIN needs to satisfy:

$$\mathbf{R}_{AIN} < \frac{Ts}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

Among them, the value of N resolution is 12.

The allowable error is less than 1/4 LSB Least Significant Bit, LSB.

Table 5-19 Maximum Input Impedance（fADC = 12 MHz）

Sampling Period Ts（Cycles）	Sampling Time t_S（μs）	Maximum Input Impedance（kΩ）
1.5	0.13	0.58
7.5	0.63	10.88
13.5	1.13	21.19
28.5	2.38	46.95
41.5	3.46	69.28
55.5	4.63	93.32
71.5	5.96	120.80
239.5	19.96	409.34

Table 5-20 ADC Accuracy

Symbol	Parameter	Test Conditions	Typical Value	Maximum	Unit
ET	Total unadjustable error (1)	V_{DD}=V_{DDA}=5V, f_{ADC} = 12 MHz,	-	3	LSB
EO	Offset error (2)		-	1	
EG	Gain error (3)		-	1	
ED	Differential linear error (4)		-	4	
EL	Integral linear error (5)		-	2	

(1). Total non-adjustable error: the maximum deviation between the actual transfer curve and the ideal transfer curve.

(2). Offset error: The deviation between the first actual conversion and the first ideal conversion.

(3). Gain error: The deviation between the last ideal transition and the last actual transition.

(4). Differential linear error: the maximum deviation between the actual step and the ideal step.

(5). Integral linear error: The maximum deviation between any actual transition and the end point correlation line.

Explain：

- ADC accuracy and negative injection current: Avoid injecting negative current on any standard non-robust analog input pin, as this can significantly reduce the accuracy of performing conversions on another analog input pin. It is recommended to add a Schottky diode pin to the standard analog pin that may inject negative current to ground.
- Better ADC performance can be achieved within a limited range of V_{DDA}, frequency, and temperature.
- The data is based on characterization results and has not been tested in production.

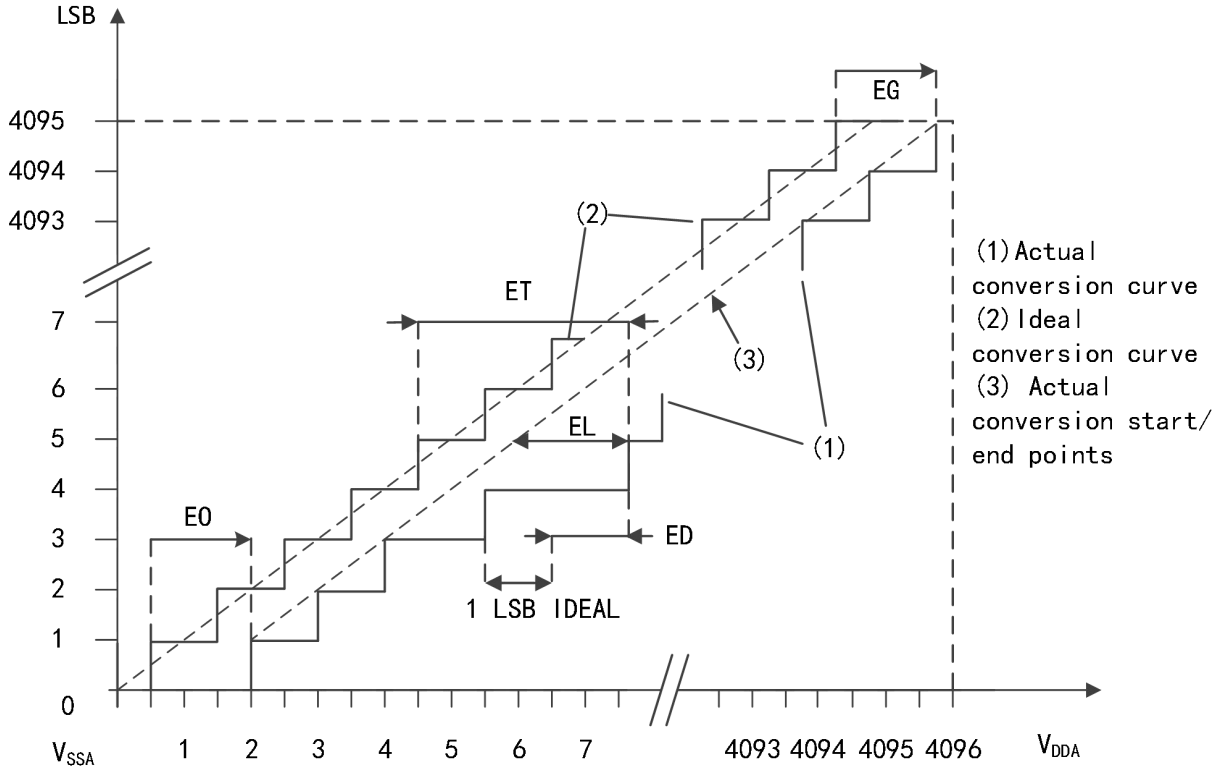


Figure 5-1 ADC Accuracy Characteristics

Explain：

For the parameter descriptions shown in Table 5-20, please refer to Table 5-20.

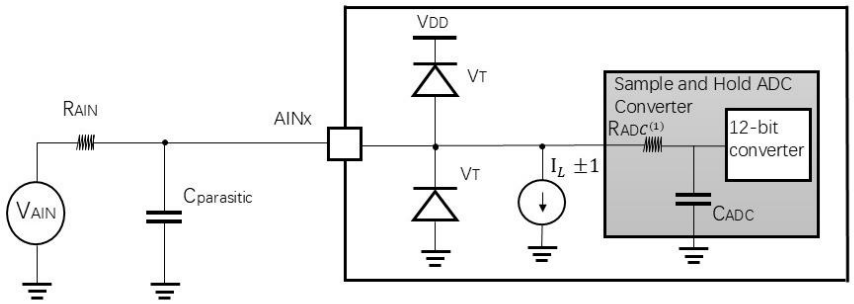


Figure 5-2 Typical Connection Diagram of ADC

(1). The ADC characteristics of RADC and CADC values are shown in Table 5-24.

$C_{parasitic}$ equals PCB capacitance depending on soldering and PCB layout quality plus pad capacitance of approximately 7 pF. A too high tangential value will reduce the conversion accuracy. To compensate for this, fADC should be minimized.

Recommendations for PCB design for ADC sampling: power decoupling should be carried out according to Figure 5-1. To ensure the accuracy of ADC conversion, it is recommended to use ceramic capacitors with a capacitance of 10 nF and place them as close to the chip as possible.

5.3.15 Three-phase Gate Driver Characteristics

Table 5-21 Three-phase Gate Driver Characteristics

Parameter	Definition	Minimum	Typical Value	Maximum	Unit
t_{DT}	Dead time	300	500	800	nS
T_{OTP}	Overheat protection threshold, turn off the entire chip		160		℃
T_{OTPHYS}	Overheat protection hysteresis		20		℃

5.3.16 Operational Amplifier Characteristics

Table 5-22 Operational Amplifier Characteristics

Parameter	Definition	Minimum	Typical Value	Maximum	Unit
V_{OP}	Operational amplifier operating voltage		5		V
V_{OFFSET}	Offset voltage		3	7	mV
VC_{RANGE}	Input common-mode voltage range	0		V_{OP}-0.2	V
I_{IN}	Input bias current			1	uA
I_{SOURCE}	Output sourcing current	1000			uA
I_{SINK}	Output sinking current	1000			uA
V_{SW}	Output voltage swing	0		V_{OP}	V
Slew rate	Rising edge		8.5		V/us
	Falling edge		5		V/us
Av	Open-loop achievement		10		Kv/V
BW	Bandwidth		6		MHZ

5.3.17 N-MOS Electrical Characteristics

Table 5-23 N-MOS Electrical Characteristics

Symbol	Description	Condition	Minimum	Typical Value	Maximum	Unit
Cut-off characteristics						
BVDSS	Drain-source breakdown voltage	VGS =0V, ID =250μA	40	-	-	V
IDSS	Leakage current with gate-source short	VDS =40V, VGS =0V	-	-	1	μA
IGSS	Gate current with drain-source short	VDS =0V, VGS=±20V	-	-	±100	nA
Conduction characteristics						
VGS(th)	Gate-source threshold voltage	VDS =VGS, ID=250μA	1.1	1.5	2.0	V
RDS(ON)	Drain-source on-state resistance	VGS=7V,ID=0.5A	-	15	-	mΩ

5.3.18 P-MOS Electrical Characteristics

Table 5-24 N-MOS Electrical Characteristics

Symbol	Description	Condition	Minimum	Typical Value	Maximum	Unit
Cut-off characteristics						
BVDSS	drain-source breakdown voltage	VGS =0V, ID =-250μA	-40	-	-	V
IDSS	drain current in gate-source short circuit	VDS =-40V, VGS =0V	-	-	-1	μA
IGSS	Gate current with drain-source short circuit	VDS =0V, VGS=±20V	-	-	±100	nA
Conduction characteristics						
VGS(th)	gate-source threshold voltage	VDS =VGS, ID=-250μA	-1.0	-1.5	-2.0	V
RDS(ON)	drain-source on-state resistance	VGS=7V,ID=-0.5A	-	36	-	mΩ

6 Pin Definition

PM30003V-0405 MCU uses TSSOP-25P package, with the following pin definitions.

6.1 TSSOP-25P Package

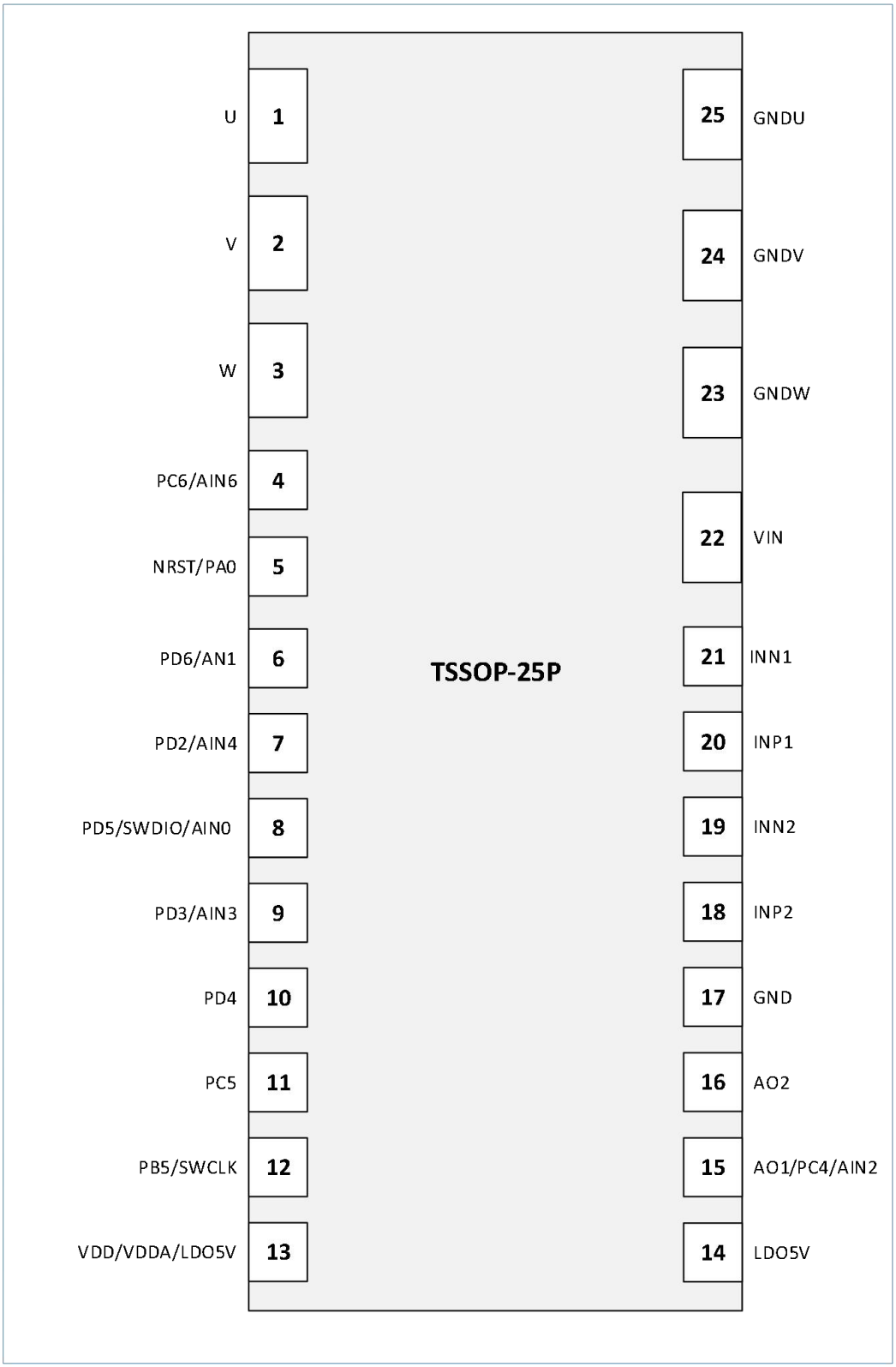


Figure 6- 1 TSSOP-25P Package

6.2 Pin Definition

Table 6-1 TSSOP-25P Package Pin Definition

"I" represents input, "O" represents output, "I/O" represents input/output, "S" represents power supply.

Pin Number	Pin Name	Pin Type (1)	Support Tolerant	Default Pin Function after Power-On	Default Multiplexed Pin Function (AF0)
1	U	O		Phase U Output	
2	V	O		Phase V Output	
3	W	O		Phase W Output	
4	PC6/AIN6	I/O		PC6	-
5	NRST/PA0	I/O		NRST	-
6	PD6/AIN1	I/O		PD6	-
7	PD2/AIN4 (2)	I/O		PD2	-
8	PD5/SWDIO/AIN0 (2)	I/O		SWDIO	SWDIO
9	PD3/AIN3 (2)	I/O		PD3	-
10	PD4	I/O		PD4	I^2C_SMBA
11	PC5/EXTCLK4	I/O		PC4/ PC5	I^2C_SDA
12	PB5/SWCLK/EXTCLK3	I/O		SWCLK	SWCLK_I^2C_SDA(3)
13	VDD/VDDA/LDO5V	S		The digital power supply on the chip is connected to the analog power supply, and internally connected to the LDO5V	
14	LDO5V	O		5V LDO output, with an external 1uF capacitor to ground	
15	AO1/PC4/AIN2(2)	I/O		Channel 1: Output of low-offset operational amplifier, simulating the input of channel 2	
16	AO2	O		Channel 2 output of low offset op-amp	
17	VSS/VSSA	S		Connect the digital ground and analog ground on the chip	
18	INP2	I		Positive input of low offset op-amp in channel 2	
19	INN2	I		Channel 2 Negative input of low offset op-amp	
20	INP1	I		Positive input of low offset op-amp in channel 1	
21	INN1	I		Channel 1 negative input of low offset op-amp	
22	V_{IN}	PWR		Input working power supply, connect an external 1uF capacitor to ground	
23	GNDW	S		W Phase Ground	
24	GNDV	S		V Phase Ground	
25	GNDU	S		U Phase Ground	

(1). AIN0 ~ AIN4 have ADC analog input function.

(2). PB5 requires additional configuration register to select SWCLK or I^2C_SDA.

6.3 Pin Multiplexing (AF) Function Table

Table 6-2 Pin Multiplexing Function Table

Pin Name	AF0 (I²C/SWD)	AF1 (UART1)	AF2 (SPI)	AF3 (TIM1)	AF4 (TIM2)	AF5 (RCC)	AF6 (UART2)	AF7 (ADC)
PA0	I²C_SMBA	UART1_TX	SPI_NSS	TIM1_BKIN	TIM2_CH3	-	UART2_TX	ADC_ETR
PA1	I²C_SCL	UART1_TX	SPI_SCK	TIM1_CH1N	TIM2_ETR	-	UART2_TX	ADC_ETR
PA2	I²C_SMBA	UART1_RX	SPI_SCK	TIM1_CH2N	TIM2_CH4	-	UART2_RX	ADC_ETR
PA3	I²C_SDA	UART1_TX	SPI_NSS	TIM1_CH3N	TIM2_CH3	RCC_MCO	UART2_TX	ADC_ETR
PB4	I²C_SCL	UART1_RX	SPI_MISO	TIM1_CH2N	TIM2_ETR	-	UART2_RX	ADC_ETR
PB5	SWCLK/I²C_SDA (1)	UART1_RX	SPI_NSS	TIM1_BKIN	TIM2_CH2	-	UART2_RX	ADC_ETR
PC3	I²C_SCL	UART1_TX	SPI_MOSI	TIM1_CH3/TIM1_CH1N (1)	TIM2_CH1	RCC_MCO	UART2_TX	ADC_ETR
PC4	I²C_SDA	UART1_RX	SPI_MISO	TIM1_CH4/TIM1_CH2N (1)	TIM2_CH4	-	UART2_RX	ADC_ETR
PC5	I²C_SDA	UART1_TX	SPI_SCK	TIM1_ETR	TIM2_CH1	-	UART2_TX	ADC_ETR
PC6	I²C_SCL	UART1_RX	SPI_MOSI	TIM1_CH1	TIM2_CH3	-	UART2_RX	ADC_ETR
PC7	I²C_SCL	UART1_RX	SPI_MISO	TIM1_CH2	TIM2_ETR	-	UART2_RX	ADC_ETR
PD1	I²C_SMBA	UART1_TX	SPI_MOSI	TIM1_CH1	TIM2_CH4	-	UART2_TX	ADC_ETR
PD2	I²C_SDA	UART1_TX	SPI_MOSI	TIM1_CH2	TIM2_CH3	-	UART2_TX	ADC_ETR
PD3	I²C_SCL	UART1_RX	SPI_SCK	TIM1_CH3	TIM2_CH2	-	UART2_RX	ADC_ETR
PD4	I²C_SMBA	UART1_TX	SPI_MOSI	TIM1_CH4	TIM2_CH1	RCC_MCO	UART2_TX	ADC_ETR
PD5	SWDIO	UART1_TX	SPI_MISO	TIM1_ETR	TIM2_ETR	RCC_MCO	UART2_TX	ADC_ETR
PD6	I²C_SMBA	UART1_RX	SPI_MISO	TIM1_CH2	TIM2_CH2	RCC_MCO	UART2_RX	ADC_ETR
PD7	I²C_SMBA	UART1_RX	SPI_NSS	TIM1_CH3/TIM1_BKIN (1)	TIM2_CH1	RCC_MCO	UART2_RX	ADC_ETR

(1). Additional configuration of the IOMUX register is required to select: PC3 as TIM1's CH3 or CH1N, and PC4 as TIM1's CH4 or CH2N; PB5 is used as SWCLK or I²C_SDA; PD7 is used as CH3 or BKIN of TIM1; For more information, see the IOMUX section of the user manual.

7 Package Parameter

7.1 Package Size

7.1.1 TSSOP-25P Package

Package Size is 9.70 mm x 4.40 mm for TSSOP-25P.

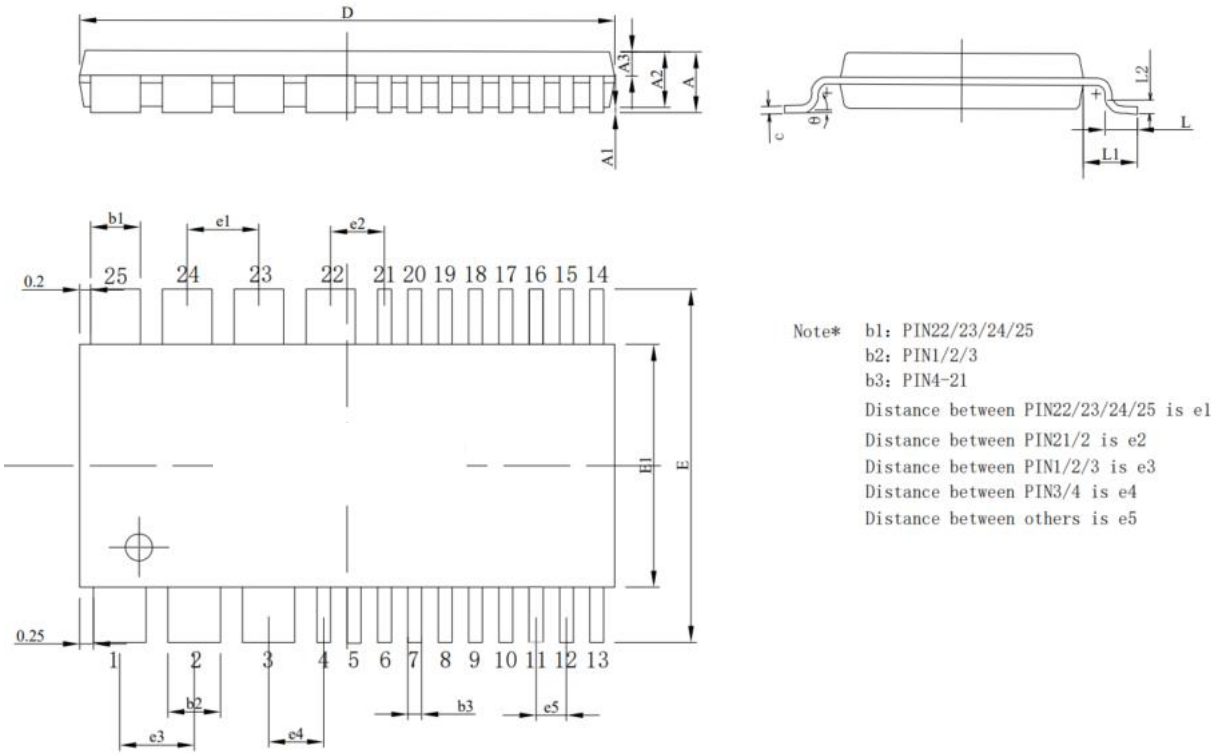


Figure 7-1 TSSOP-25P Package Size

Table 7-1 TSSOP-25P Package Size Parameter

Symbol	Minimum（mm）	Typical Value（mm）	Maximum（mm）
A	-	-	1.2
A1	0.03	0.08	0.12
A2	0.80	-	1.0
A3	0.39	0.44	0.49
b1	-	0.90	-
b2	-	0.95	-
b3	-	0.25	-
c	0.14	-	0.18
D	9.60	9.70	9.80
E	6.20	6.40	6.60
E1	4.30	4.40	4.50

Symbol	Minimum（mm）	Typical Value（mm）	Maximum（mm）
e1		1.3BSC	
e2		0.98BSC	
e3		1.35BSC	
e4		1.0BSC	
e5		0.55BSC	
L	0.45	0.60	0.75
L1		1.0BSC	
L2		0.25BSC	
θ	0	-	8°

8 Acronyms

Acronyms	Full Name
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
APB	Advanced Peripheral Bus
AWU	Auto-Wakeup
CLU	Configurable Logic Unit
CRC	Cyclic Redundancy Check
CSS	Clock Security System
CTS	Clear to Send
DMA	Direct Memory Access
EMACC	Electric Motor Acceleration
EXTI	Extended Interrupts and Events Controller
GPIO	General Purpose Input Output
HSE	High Speed External（Clock Signal）
I^2C	Inter-Integrated Circuit
I2S	Inter-IC Sound
IWDG	Independent Watchdog
LSI	Low-Speed Internal（Clock Signal）
MCU	Microcontroller Unit
MSPS	Million Samples Per Second
NVIC	Nested Vectored Interrupt Controller
PDR	Power-Down Reset
PLL	Phase Locked Loop
POR	Power-On Reset
PPM	Parts per Million
PWM	Pulse Width Modulation
RCC	Reset and Clock Control
RISC	Reduced Instruction Set Computing
RTS	Request to Send
SPI	Serial Peripheral Interface

Acronyms	Full Name
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
USART	Universal Synchronous Asynchronous Receiver Transmitter
UART	Universal Asynchronous Receiver Transmitter
WWDG	Window Watchdog

9 Version History

Version	Date	Changes
Rev.1.0	2025-06-20	Initial release
Rev.1.1	2025-07-15	Modified: Section 8 "Acronyms" (removed Description in Chinese) Added: Section 9 "Version History"
Rev.1.2	2025-07-18	Package naming update
Rev.1.3	2025-08-08	Added "Meet AEC-Q100 requirements" in Section 2 Product name updated to PM30003V-0405BQ

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