PJ60221 Datasheet

Dual Gate Driver

Version：Rev.1.1

Release Date：2025-12-24

MetaWells Co., Ltd.

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General Description

The PJ60221 N-Channel FET Gate Driver is used for controlling a delayed turn on and ramping slew rate (1.3V/ms, typ) of the source voltage on N-Channel FET switches from a CMOS logic level input. The PJ60221 integrates a charge pump internally, significantly reducing static power consumption. The quiescent current <5μA (typ) in standby state. Intended as a supporting control element for switched voltage rails in energy efficient, advanced power management systems, the PJ60221 also integrates circuits to discharge opened switched voltage rails. Furthermore, the PJ60221 is equipped with a built-in Power Good module to monitor whether the external N-FET is working properly.

Features

- 5V ±5% Power supply
- PJ60221 Drain Voltage Range 1.0V to 20V
- Internal Gate Voltage Charge Pump
- Controlled Turn on Delay
- Controlled Load Discharge Rate
- Controlled Turn on Slew Rate
- Stable Slew Rate(±2% Typ.) over Temperature
- DFN2*2-8 Package
- Pb-Free/Halogen-Free/RoHS compliant

Applications

- Power Rail Switches
- Hot Plugging Applications
- Soft Switching
- Personal computers and Servers
- Data Communications Equipment

Ordering Information

Ordering Information

Order number	Marking ID	Package	MSL	Description
PJ60221QW	A5W	DFN2X2-8	Level-3	Halogen free RoHS compliant in T/R,3,000 pcs/Reel

Marking Information

Marking	Package	Definition
A5W	DFN2X2-8	A5: Product code W: Week Code

Typical Application

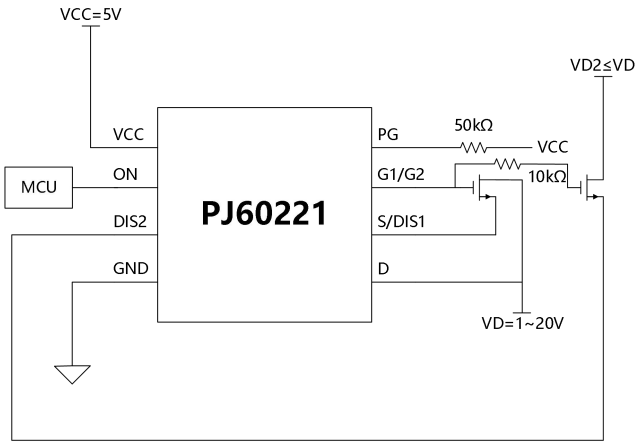


Figure 1. Typical Application Circuit

Pin Configuration

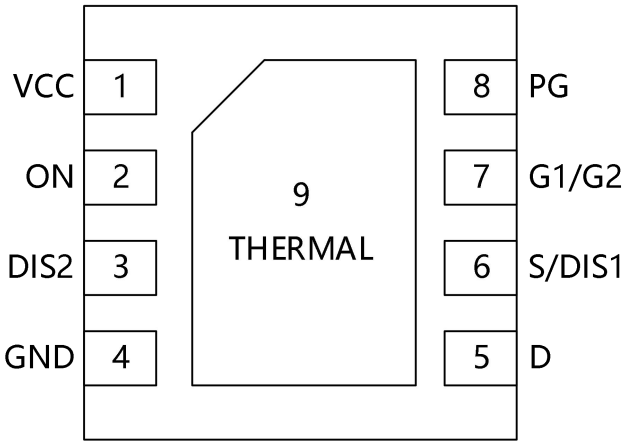


Figure 2. DFN2*2-8 package with exposed thermal pad (TOP VIEW; NOT TO SCALE)

Functional Pin Description

Pin			Description
Name	Num	Type(1)	
1	VCC	P	Supply Voltage
2	ON	I	CMOS Logic Level. High True
3	DIS2	O	Discharge Connection for Load2
4	GND	G	Ground
5	D	I	FET Drain Connection
6	S1/DIS1	I/O	Source Connection, Discharge Connection for Load1
7	G1/G2	O	FET Gate Drive for FET1, FET2
8	PG	O	CMOS Power Good Signal.
9	Exposed thermal pad	G	Ground

(1). A = Analog Pin ; P = Power Pin ; D = Digital Pin ; I = Input Pin ; O = Output Pin ; G = GND Pin

Absolute Maximum Ratings

Parameter	Min	Max	Unit
V_D, V_G V_{S1} or V_{DIS2} to GND	-0.3	32.0	V
Voltage at Logic Input pins	-0.3	6.5	V
Current at input pin	-1.0	1.0	mA
Storage temperature	−65	150	°C
Junction temperature		150	°C

(1). Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature(T_A)	−40	25	125	°C
Continuous Supply Voltage (V_{CC})	4.75	5.0	5.25	V
Junction Temperature (T_J)	−40		125	°C

Handling Ratings

Parameter	Description	Rating	Unit
HBM	Human Body Model ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
CDM	Charged Device Model ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±750	V
Latch-Up	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±100	mA

Thermal Resistance

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Item(1)(2)	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	50	°C/W
θ_{JC_Top}	Junction-to-case (top) thermal resistance	55	°C/W

(1). The package thermal impedance is calculated in accordance to JESD 51-7.

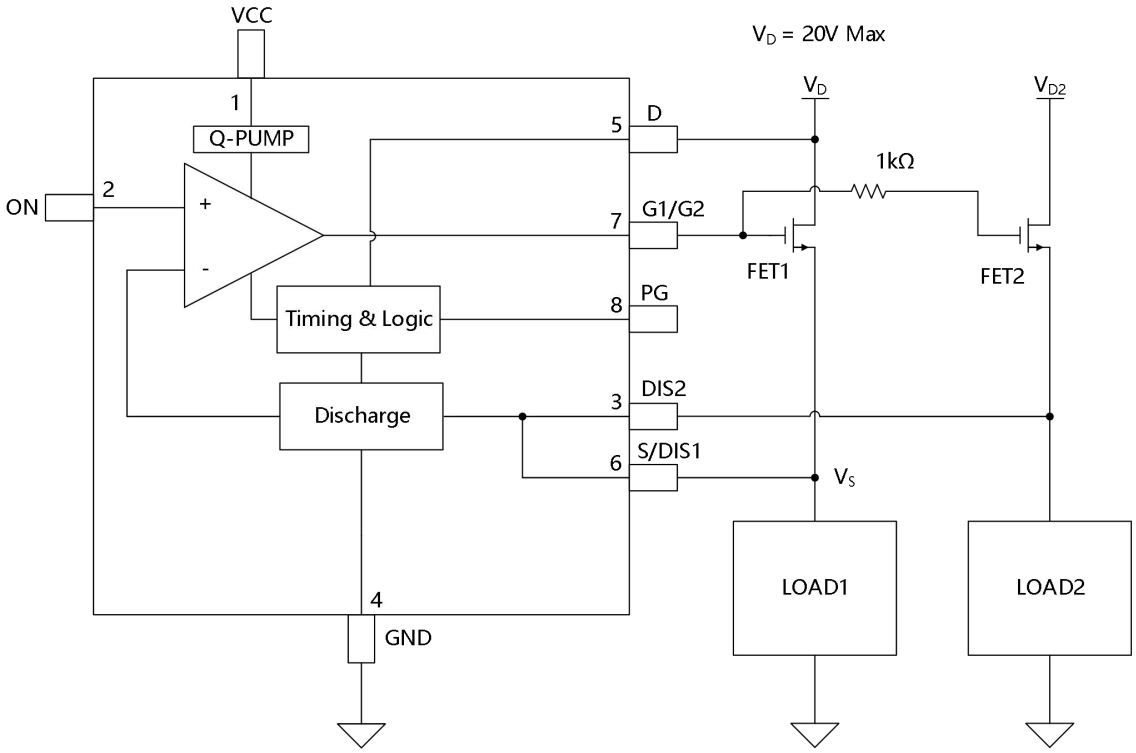
(2). Thermal Resistances were simulated on a 4-layer, JEDEC board.

Electrical Characteristics

V_{CC} = 5.0V, T_A = −40°C to +125°C for minimum and maximum specifications, and T_A = 25°C for typical specifications, unless otherwise noted.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Supply Voltage	V_{CC}		4.75	5.0	5.25	V
Quiescent Current	I_Q	V_G not ramping FET = ON		15.0	26.0	µA
		V_G not ramping FET = OFF		0.01	1.0	µA
		V_G not ramping FET = OFF to ON		200	400	µA
FET Drain Voltage	V_D		1.0		20	V
Gate - Source Voltage	V_{GS}	V_D = 20V	8.0	9.5	11.0	V
FET Gate Capacitance	C_G		500		18000	pF
Ramp Delay Range	T_{DELAY}	C_{GS} = 500pF, V_S = 0.5V	0.16	0.40	0.56	ms
		C_{GS} = 18000pF, V_S = 0.5V	0.3	1	1.5	ms
FET Turn on Slew Rate	T_{SLEW}	T_A = 0°C to +85°C	0.65	1.30	1.78	V/ms
		T_A = −40°C to +125°C	0.57	1.30	1.88	V/ms
Internal Discharge Resistor	$R_{DISCHARGE1}$	Nominal discharge time of ~100ms 10mA max rate	250	400	550	Ω
	$R_{DISCHARGE2}$		750	1300	2000	
HIGH – Level input voltage	V_{IH}	ON, SHDN# (200mV Hysteresis)	2.4		5.5	V
LOW – Level input voltage	V_{IL}	ON, SHDN# (200mV Hysteresis)			0.4	V
HIGH – Level output voltage	V_{OH}	PG	4.0		5.5	V
LOW – Level output voltage	V_{OL}	PG			0.4	V
Logic LOW – Level output	I_{OL_LOGIC}	PG Sink Current	2.0	3.0	4.0	mA
Gate Drive Sink Current	I_{G_OL}	V_G = 5V	400			µA
Gate Drive Source Current	I_{G_OH}		32			µA
Drain Pin Current	I_{D_IH}	V_D = 20V in Standby, ON = 5V		4.6	8.0	µA
Source Pin Current Quiescent	I_{S_IH}	V_S = 20V			<1.0	µA

Functional Block Diagram



The highest V_D being switched must be at FET1 and pin 5 of PJ60221

Figure 3. Functional Block Diagram

Product Overview

The PJ60221 N-Channel FET Gate Driver is used for controlling a delayed turn on and ramping slew rate of the source voltage on N-Channel FET switches from a CMOS logic level input. Intended as a supporting control element for switched voltage rails in energy efficient, advanced power management systems, the PJ60221 also integrates circuits to discharge opened switched voltage rails. The gate driver is available in a variety of configurations supporting a range of turn-on slew rates from 0.80 V/ms up to 4 V/ms which, depending on load supplying source voltages in the range of 1.0 V to 20 V results in ramp times from 200 μs up to over 20 ms (see Application Circuit). Delays until the ramp begins are source voltage independent and range from 250 μs to 5 ms. A power good condition is output to indicate that the ramp-up slew of the source voltage is finished. Additionally, an internal discharge circuit provides a controlled path to remove charge from open power rails. The PJ60221 gate drive is packaged in an 8 pin DFN package.

When used with external N-Channel FETs, the PJ60221 supports low transient, energy efficient switching of high current loads at source voltages ranging from 1.0 V to 20 V.

Typical Application Circuit

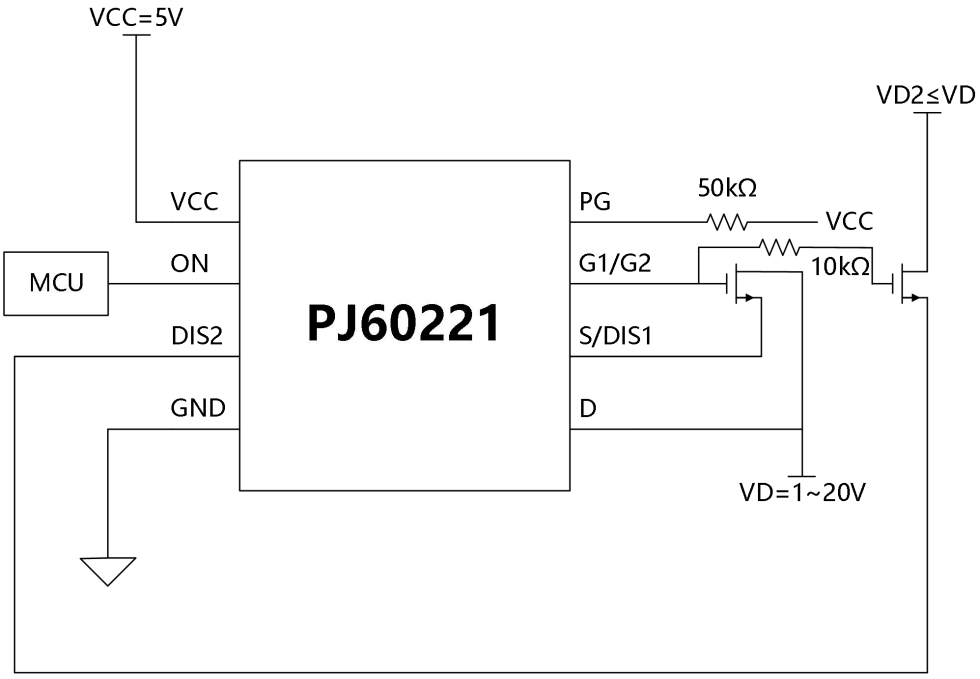


Figure 4. Typical Application Circuit

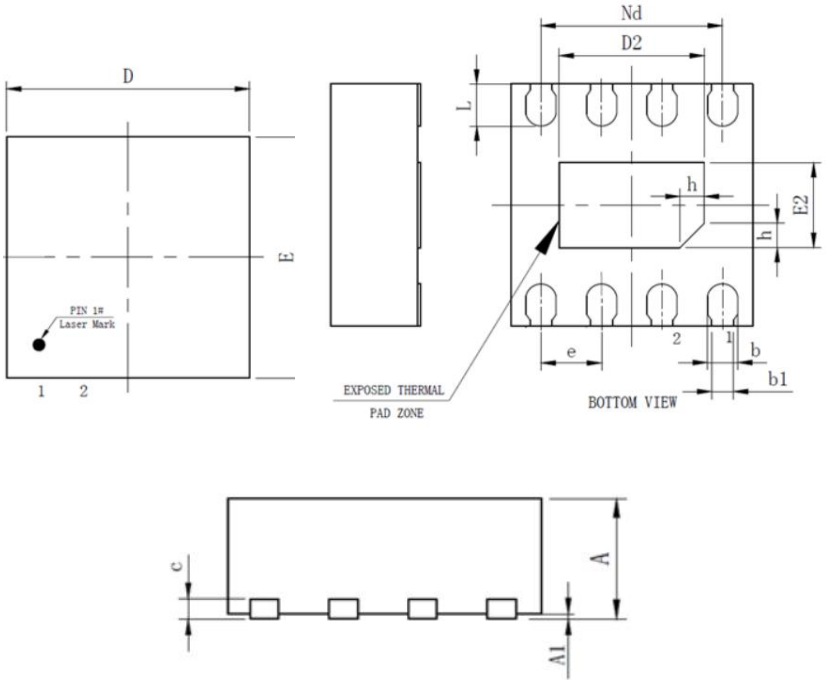
Application Information

In a typical application, de-asserting ON (low) or asserting the low true Shut Down signal (SHDN#) turns off the external power N-FET. SHDN# is provided as an asynchronous override to the ON signal. When the FET is turned off, the voltage at the load is discharged through a resistor (typically 1300 ohms) internal to the PJ60221 with the discharge current limited to a maximum of 10mA. When ON is asserted (high), gate voltage is not applied to the gate of the external power N-FET until after T_{DELAY} then the gate source (V_{GS}) voltage is ramped up to 9.3 V above the source voltage V_S at a slew rate determined by the internal slew rate control element internal to the PJ60221. Monotonic rise of V_S is maintained even as I_D increases dramatically after the load device turn on threshold voltage is reached. After the source voltage has ramped up to its maximum steady state value, the Open Drain PG (Power Good) signal is asserted. PG may be used as the ON control of a second PJ60221 thereby providing power on sequence control of a number of switched power rails, or used in a 'wired and' with other PG signals to indicate all switched power rails are in a power good condition.

The devices will not operate if V_{CC} is below 3.5 V.

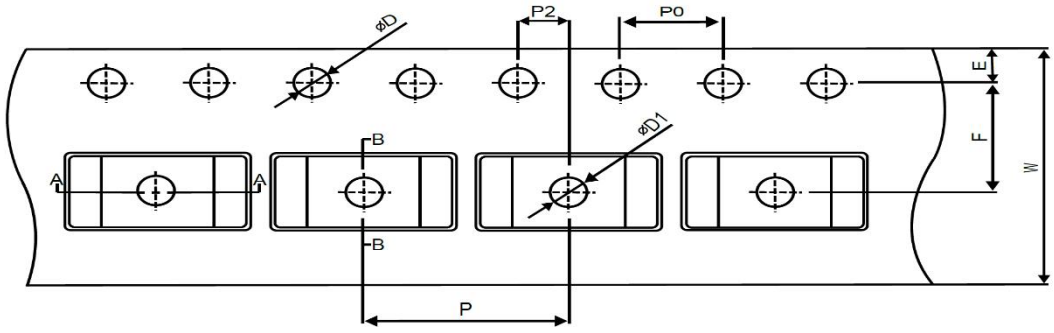
The waveforms shown illustrate the monotonic rise of the source voltage of a FET as gate voltage is controlled to accommodate for variations in load current as the voltage is applied.

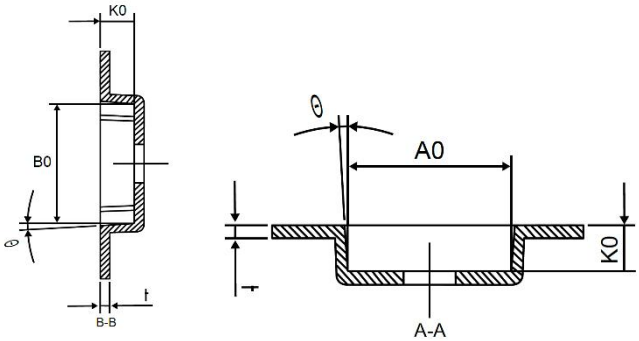
Package Outline Dimensions

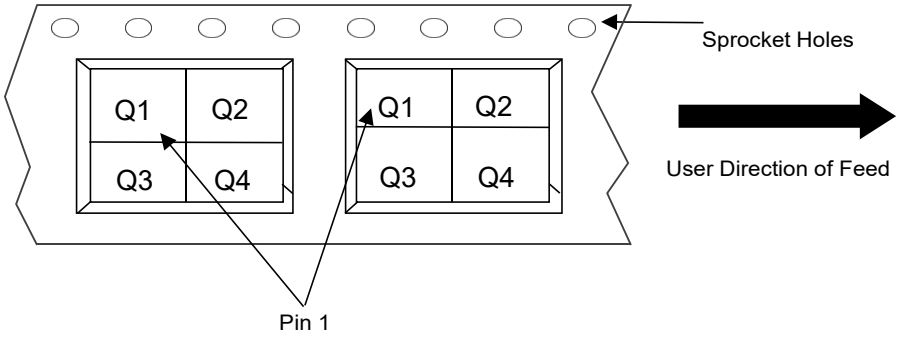


Dimension in mm			
Symbol	**Min**	**Nom**	**Max**
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.18	0.25	0.30
b1		0.18REF	
c	0.18	0.20	0.25
D	1.90	2.00	2.10
D2	1.10	1.20	1.30
e		0.50BSC	
Nd		1.50BSC	
E	1.90	2.00	2.10
E2	0.60	0.70	0.80
L	0.30	0.35	0.40
h	0.15	0.20	0.25

Packing Information







Package Type	A0 (mm)	B0 (mm)	K0 (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant	Quantity
DFN2x2-8	2.15	2.15	0.88	4.00	4.00	8.00	Q1	3000

Version History

Version	Date	Changes
Rev.1.0	2025-10-29	Initial release
Rev.1.1	2025-12-24	1. Added MSL information: Level 3. 2. Changed Pin1 orientation: from Q3 to Q1.

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