PJ91923 Datasheet

Piezo Haptic Driver with Digital Front End

Version：Rev.1.0

Release Date：2026-03-05

MetaWells Co., Ltd.

www.metawells.com

General Description

The PJ91923 is a single-chip piezo actuator driver with energy recovery. It can drive actuators with waveforms up to 190 Vpk-pk while operating from a 2.3 to 5.5 V supply voltage. Its low power and small size make it ideal for applications requiring minimal power consumption. The PJ91923 features high-resolution piezo sensing capabilities allowing haptic feedback to be automatically played when detection conditions are met.

The PJ91923 differential driver achieves low distortion waveforms and quiet actuator operation. All settings are adjustable through the digital front end to reduce the BOM. Data and configuration parameters are easily communicated to the PJ91923 through its two wire I2C interface. A flexible deep FIFO enables the streaming of digital waveform data for playback or the transmission of burst data for more bandwidth efficiency. The PJ91923 also integrates 1.5 kB of RAM waveform memory to generate waveforms with minimal communication bandwidth.

A dedicated SYNC pin can synchronize multiple PJ91923 controllers to simultaneously drive multiple actuators within 2μs. In addition to SYNC synchronization, PJ91923 can also support CLK_SYNC synchronization. This function synchronizes the clock, and multiple chips share the same clock.

With a typical start-up time of less than 200μs, the PJ91923 latency is negligible in most systems.

Various safety systems protect the PJ91923 from damage in case of a fault.

Features

- High-Voltage Low Power Piezo Driver
  - Drive 100nF at 190V_{PP} and 200Hz with 490mW
  - Drives Capacitive Loads up to 1000nF
  - Energy Recovery
  - Differential Output
  - Small Solution Footprint, QFN & WLCSP
- Low Quiescent Current: SHUTDOWN; SLEEP; IDLE; IDLE mode Current only 90uA
- Multiple operating modes: AUTOPLAY; SENSEPLAY; DIRECTPLAY; FIFOPLAY; SRAMPLAY
- Wide Supply Voltage Range of 2.3V to 5.5V
- Advanced Piezo Sensing Capabilities
  - 8.8 mV Sensing Resolution
  - Interrupt Generation
  - Automatic Triggering of Haptic Feedback
- Integrated Digital Front End with I2C
  - 1024 sample Internal FIFO Interface
  - 1.8 V Digital I/O Supply
  - Supports Continuous Waveforms Playback
  - State Retention in SLEEP Mode
- Fast Start Up Time less than 200 μs
- Multi-Actuator Synchronization; address selection; Power-on-Reset
- ESD verification pass, latch up verification pass

Applications

- Electronic Cooling
- Portable Computers, Keyboards and Mice
- Gaming Controllers, Wearables

Ordering Information

Ordering Information

Order number	Marking ID	Package	Description
PJ91923QW	91923 YMDNN	QFN4X4-24	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel
PJ91923WS	A2 W	CSP 2.1mmx1.7mm-20	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel

Note:

(1) MetaWells can meet RoHS 2.0/REACH requirement. So most package types MetaWells offers only states halogen free, instead of lead free.

Marking Information

Marking	Package	Definition
91923 YMDNN	QFN4X4-24	91923 : Product code YMDNN : Y : Year code M : Month code D : Day code NN : Serial Number
A2 W	CSP 2.1mmx1.7mm-20	A2 : Product code W : Week code

Typical Application

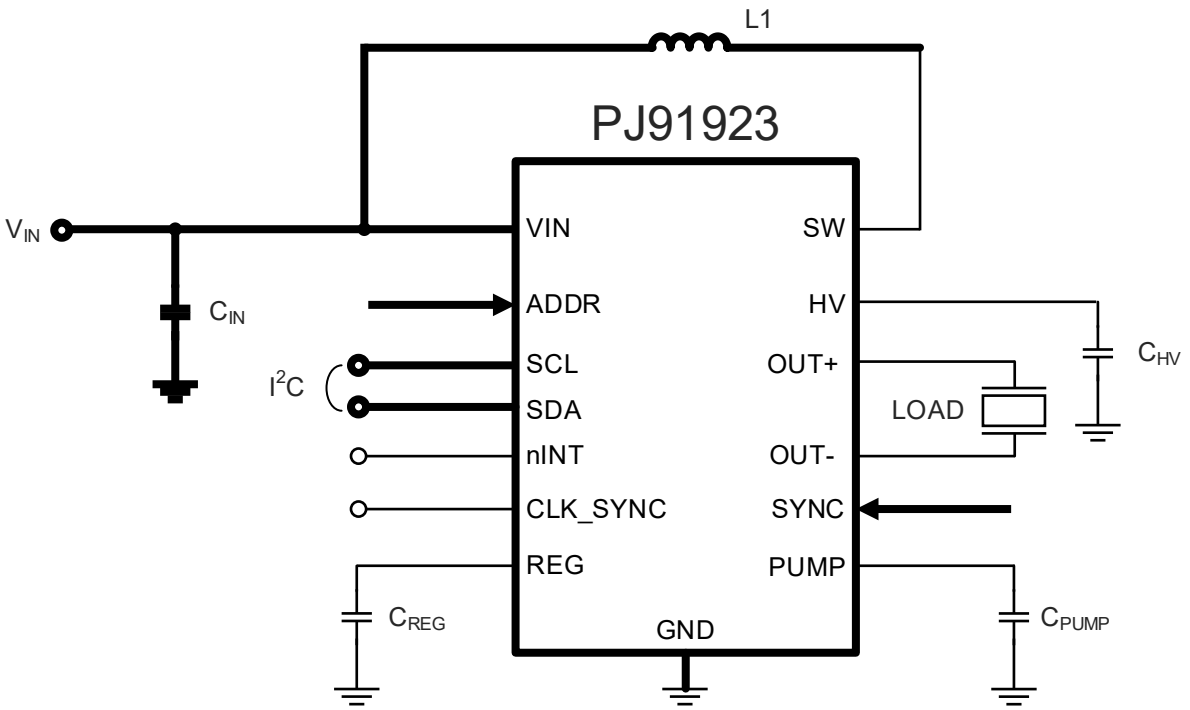


Figure 1. Typical Application Circuit

Pin Configuration

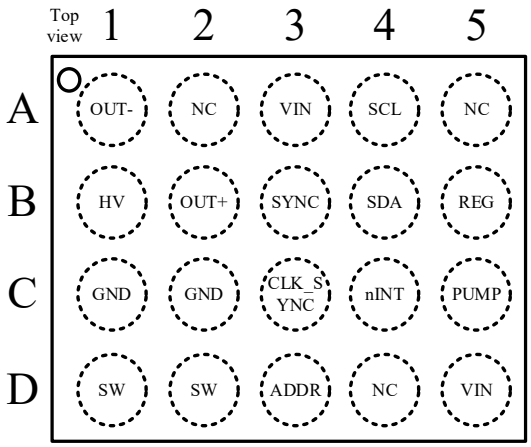


Figure 2. CSP 2.1mm*1.7mm 20B package (TOP VIEW; NOT TO SCALE)

Pin Description

Table 1. CSP 20B Pin Function Descriptions

Pin No.	Pin Name	Type(1)	Description
A1	OUT-	O	Negative Differential Output
A2	NC	-	No connect
A3	VIN	P	Main Power Supply
A4	SCL	I	I2C clock
A5	NC	-	No connect
B1	HV	P	High-Voltage Output
B2	OUT+	O	Positive Differential Output
B3	SYNC	I/O	Synchronization pin
B4	SDA	I/O	I2C data
B5	REG	P	Internal 1.8 V Regulator Output
C1	GND	P	Ground
C2	GND	P	Ground
C3	CLK_SYNC	I/O	CLK Synchronization Pin, Can Be Set to Either Master or Slave Mode
C4	nINT	O	Interrupt or Alarm Out Pin
C5	PUMP	P	Internal 2.2 V Regulator Output Analog Power
D1	SW	P	Internal Power Converter Switch Pin
D2	SW	P	Internal Power Converter Switch Pin
D3	ADDR	I	IIC Slave Address.
D4	NC	-	No connect
D5	VIN	P	Main Power Supply

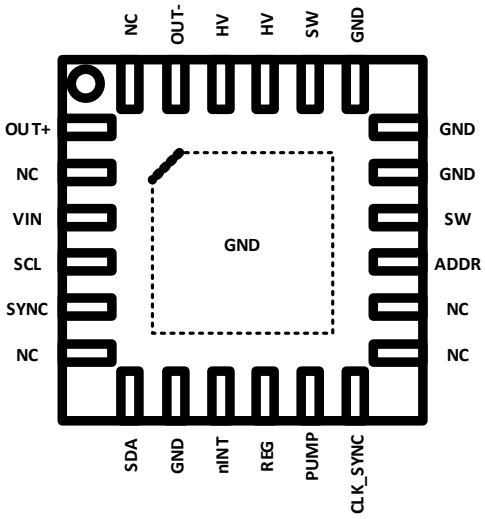


Figure 3. QFN 4mm*4mm 24 package with exposed thermal pad (TOP VIEW; NOT TO SCALE)

Table 2. QFN24 Pin Function Descriptions

Pin No.	Pin Name	Type(1)	Description
1	OUT+	O	Positive Differential Output(O)
2	NC	-	No connect
3	VIN	P	Main Power Supply （=VIN）
4	SCL	I	I2C clock
5	SYNC	I/O	Synchronization pin Open Drain
6	NC	-	No connect
7	SDA	I/O	I2C data
8	GND	P	Supply Ground
9	nINT	O	Interrupt or Alarm Out Pin
10	REG	P	Internal 1.8 V Regulator Output
11	PUMP	P	Internal 2.2 V Regulator Output Analog Power
12	CLK_SYNC	I/O	CLK Synchronization Pin, Can Be Set to Either Master or Slave Mode(I/O)
13	NC	-	No connect
14	NC	-	No connect
15	ADDR	I	IIC Slave Address.
16	SW	P	Internal Power Converter Switch Pin
17	GND	P	Supply Ground
18	GND	P	Supply Ground
19	GND	P	Supply Ground
20	SW	P	Internal Power Converter Switch Pin
21	HV	P	High-Voltage Output
22	HV	P	High-Voltage Output
23	OUT-	P	Negative Differential Output
24	NC	-	No connect
25	GND	P	Supply Ground

(1) Legend: A = Analog Pin; P = Power Pin; D = Digital Pin; I = Input Pin; O = Output Pin.

Absolute Maximum Ratings

Parameter	Min	Max	Units
Voltage at pins HV, OUT+, OUT-, SW	-0.3	110	V
Voltage at pins REG, CLK_SYNC	-0.3	3.6	V
Voltage at all other pins	-0.3	7	V
Junction temperature	-40	150	°C
Storage temperature	-65	150	°C

(1) Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Operating Temperature	-40		125	°C
Continuous Supply Voltage (V_{IN})	2.3		5.5	V
Load Capacitance			1000	nF
Inductance	10	47	68	μH
Output frequency	1		1000	Hz
Junction Temperature (T_J)	-40		125	°C

Electrostatic Discharge (ESD)

Parameter	Description	Rating	Units
HBM	Human Body Model ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
CDM	Charged Device Mode ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±500	V
Latch-Up	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification,Class: I	±200	mA

Thermal Resistance

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Item(1) (2)	Description	Value		Unit
		QFN4*4_24	CSP20B	
θ_{JA}	Junction-to-ambient thermal resistance	35.5	51.6	°C/W
θ_{JC_Top}	Junction-to-case (top) thermal resistance	24.7	0.3	°C/W

(1) The package thermal impedance is calculated in accordance to JESD 51-7.

(2) Thermal Resistances were simulated on a 4-layer, JEDEC board.

Electrical Characteristics

V_{IN} = 3.6 V, T_J = −40°C to +125°C for minimum and maximum specifications, and T_J = 25°C of PJ91923QW for typical specifications, unless otherwise noted.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Voltage at REG pin	V_{REG}		1.62		1.98	V
Digital low-level input voltage	V_{IL}	SDA, SCL, GPIO & SYNC pins			0.5	V
Digital high-level input voltage	V_{IH}		1.26			V
Digital low-level output voltage	V_{OL}				0.4	V
Digital high-level output voltage	V_{OH}		1.26			V
Full-scale output voltage	$V_{OUT(FS)}$	QFN_24	185	190	195	V_{PK_PK}
		CSP_20B	186	190	194	
VIN Quiescent current	I_{Q_VIN}	SHUTDOWN Mode		1.3	2.7	µA
		SLEEP Mode, QFN-24		5	120	µA
		SLEEP Mode, CSP20B		5	50	µA
		IDLE Mode		90	200	µA
Maximum Inductor Current(1)	I_{L_MAX}			1000		mA
Average VIN supply current during operation(2)	$I_{VIN,AVG}$	V_{IN} = 5 V f_{OUT} = DC V_{OUT} = 95 V C_{LOAD} = 100 nF		14		mA
		V_{IN} = 3.6 V f_{OUT} = 200 Hz V_{OUT} = 190 Vpk-pk C_{LOAD}= 10 nF		17.8		mA
Total Harmonic Distortion + Noise	THD+N	f_{OUT} = 250 Hz V_{OUT} = 190 Vpk-pk C_{LOAD} = 100 nF		1		%
Programmable FIFO playback rate(1)	fs-FIFO	PLAY_SRATE[15:0]=0x0000	970	1024	1080	ksps
		PLAY_SRATE[15:0]=0xFFFF		0.015		ksps
Piezo Sensing Resolution	PSR	CONFIG.GAINS=0x1		8.8		mV
		CONFIG.GAINS=0x0		46		mV
Start-up Time	tstart	Time from SLEEP mode to haptic waveform playback			200	µs
Sensing Detection to Haptic Feedback Latency	DHL	Time from sensing detection event to automatic playback		30		µs
Full scale input range of ADC(1)		ADC_Gain=0	-0.35		18	V
		ADC_Gain=1	-0.35		100	V
ADC Offset error(3)	ADC V_{OS}		-4		4	lsb
ADC Gain error	ADC GE		-2		2	%
ADC Differential nonlinearity	ADC DNL		-1.5		1.5	lsb
ADC Integral nonlinearity	ADC INL		-2		2	lsb
ADC Effective number of bits	ADC ENOB			10		bit
ADC Sampling Frequency	f_{SMPL}			10		kSps
DAC Offset error(3)	DAC V_{OS}		-1		1	lsb

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DAC Gain error	DAC GE	OUT Vpk=190, QFN_24	-2.5		2.5	%
		OUT Vpk=190, CSP_20B	-2		2	%
DAC Differential nonlinearity	DAC DNL		-1.5		1.5	lsb
DAC Integral nonlinearity	DAC INL		-2.0		2.0	lsb

(1) This parameter is related to the device part. See Ordering Information for more details.

(2) This parameter is strongly correlated to the DCR of the inductor, which was tested on PA4342.473ANLT.

(3) These characteristics is guaranteed by design.

Typical Performance Characteristics

Typical performance characteristics for the following conditions: T_A = 25°C, V_{IN} = 3.6 V, C_L = 100 nF,V_{OUT} = 190 Vpk-pk and f_{OUT} = 200 Hz (unless otherwise noted).

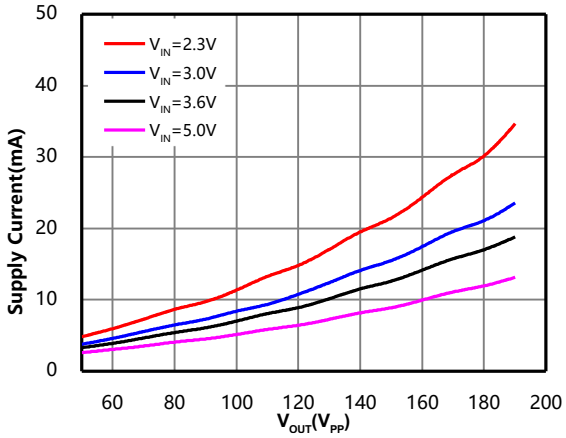


Figure 4. Supply Current vs Output Voltage

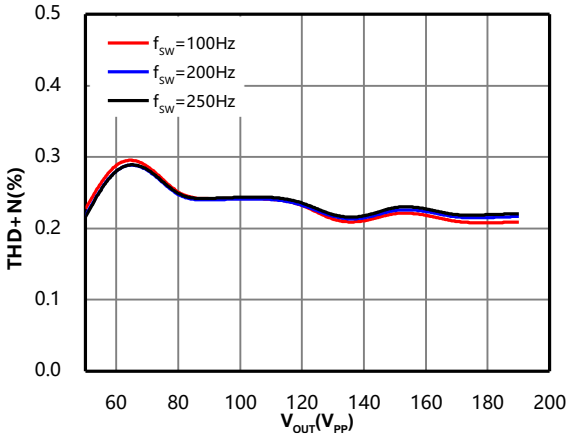


Figure 7. Total Harmonic Distortion + Noise vs Output Voltage

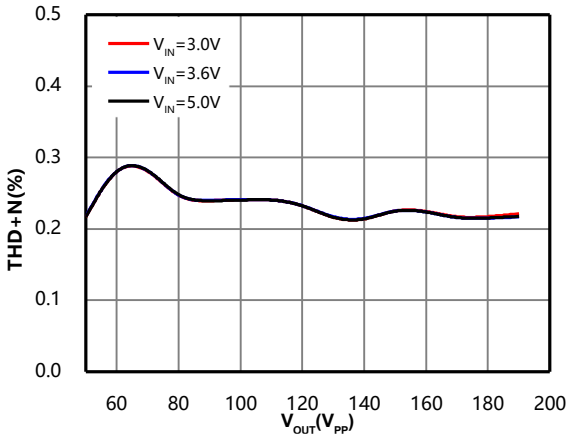


Figure 5. Total Harmonic Distortion + Noise vs Output Voltage

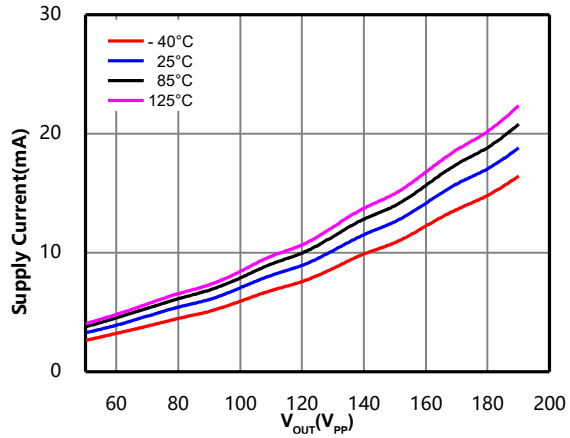


Figure 8. Supply Current vs Output Voltage

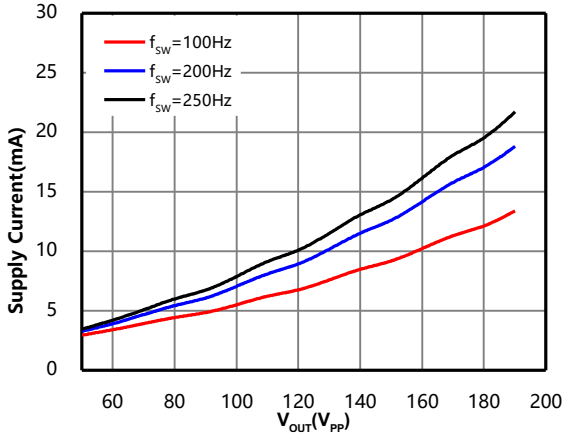


Figure 6. Supply Current vs Output Voltage

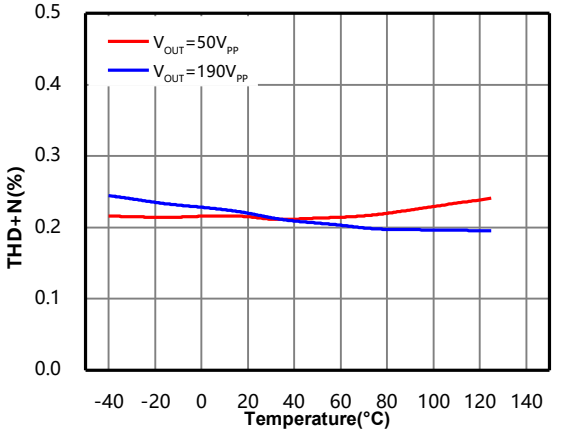


Figure 9. Total Harmonic Distortion + Noise vs Temperature

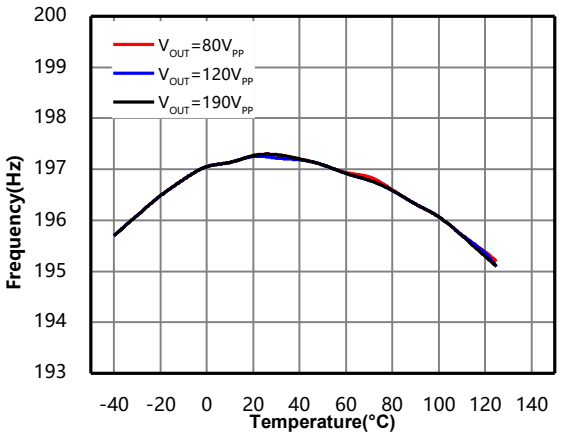


Figure 10. Output Frequency vs Temperature

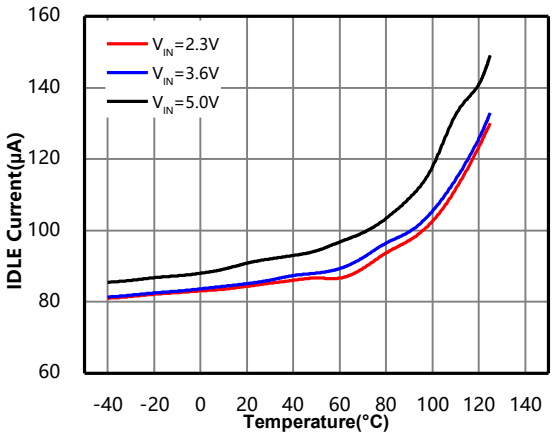
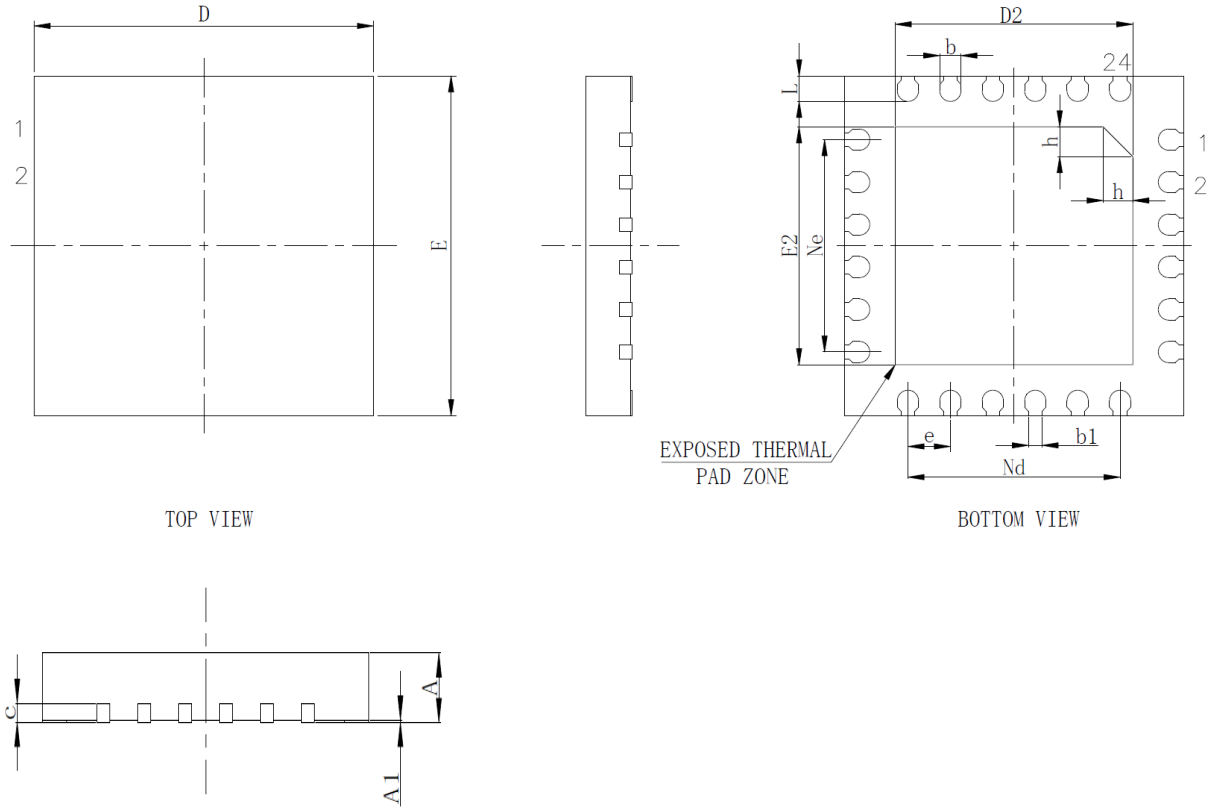


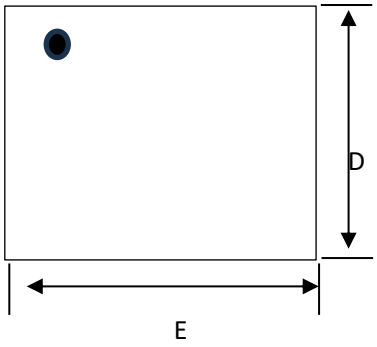
Figure 11. Quiescent Current in IDLE Mode vs Temperature

Package Outline Dimension-QFN4X4-24

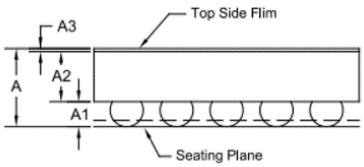


Symbol	Millimeter		
	Min.	Nom.	Max.
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1		0.16REF	
c	0.10	0.15	0.20
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e		0.50BSC	
Ne		2.50BSC	
Nd		2.50BSC	
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40

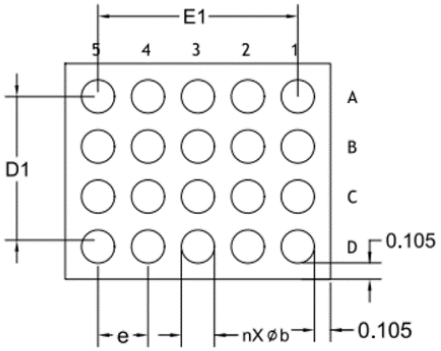
Package Outline Dimension-CSP 20



TOP VIEW



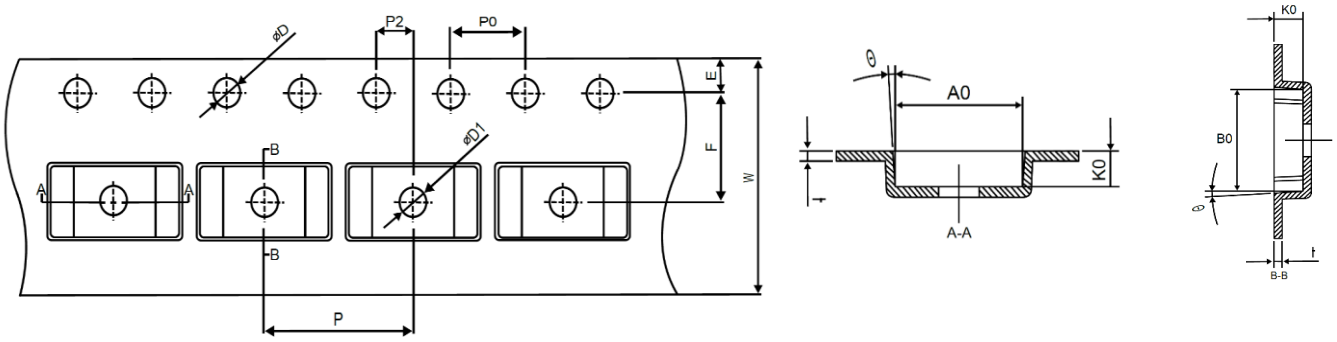
SIDE VIEW

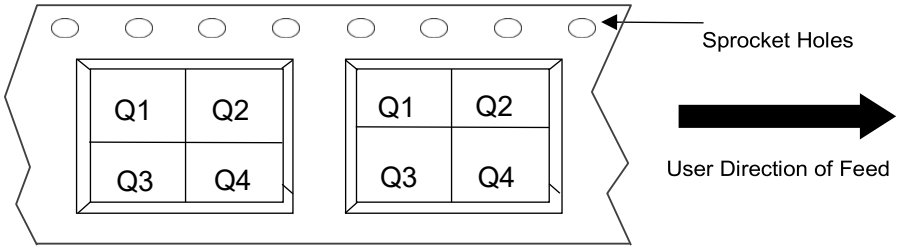


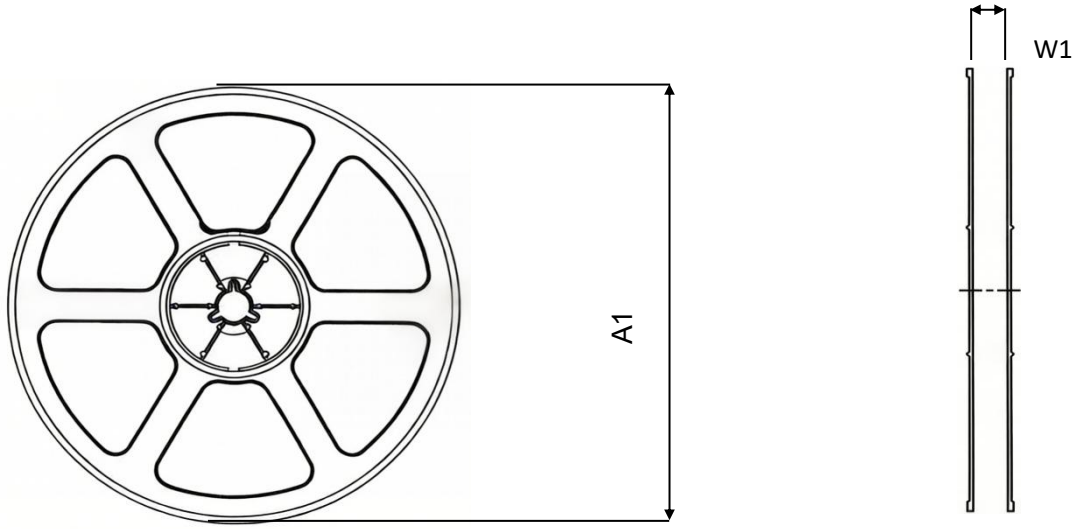
BOTTOM VIEW

Symbol	Millimeter		
	Min.	Nom.	Max.
A	0.595	0.625	0.655
A1	0.180	0.200	0.220
A2	0.387	0.400	0.413
A3	0.20	0.25	0.30
D1	1.1	1.2	1.3
E1	1.5	1.6	1.7
b	0.245	0.265	0.285
D	1.75	1.77	1.79
E	2.15	2.17	2.19
e	0.4BSC		

Packing information







Package Type	E (mm)	F (mm)	P2 (mm)	D (mm)	D1 (mm)	P0 (mm)	W (mm)	W1 (mm)	P (mm)	A0 (mm)	A1 (mm)	B0 (mm)	K0 (mm)	t (mm)	Pin1 Quadrant	Quantity
QFN4*4-24	1.75	5.50	2.00	1.55	1.50	4.00	12.00	12.80	8.00	4.25	329	4.25	0.95	0.30	Q1	3000
CSP 20B 2.1mm × 1.7mm	1.75	3.50	2.00	1.55	0.50	4.00	8.00	9.50	4.00	1.95	178	2.30	0.75	0.20	Q2	3000

(1) All dimensions are nominal.

Version History

Version	Date	Changes
Rev.1.0	2026-03-05	Initial release

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