PJ20950A Datasheet

5.5V, 450mA, High PSRR And Ultra Low Noise LDO In a Tiny Package

Version：Rev.1.0

Release Date：2026-01-13

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www.metawells.com

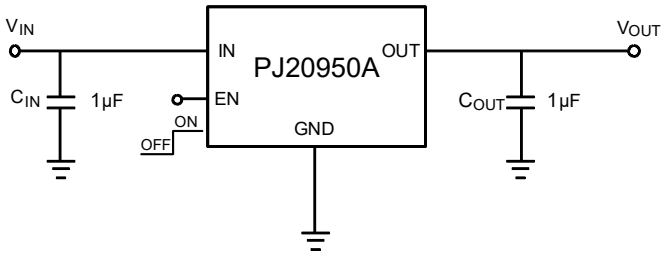
General Description

The PJ20950A series is a 450 mA, ultra-high PSRR, ultra-low noise, high-accuracy, and low dropout CMOS linear regulator with high ripple rejection. The device is ideal for radio frequency and analog circuits for its low quiescent current consumption and fast line and load transient performance. The PJ20950A operates over an input voltage range of 1.65 V to 5.5 V and supports fixed output voltage from 1 V to 3.3 V.

The PJ20950A is designed to work with a 1 µF input and a 1 µF output ceramic capacitor, allowing for a small overall solution size. A precision band-gap and error amplifier provide high accuracy of ±1% (max) at 25°C.

The device is available in SOT23-5, DFN1x1-4 and WLCSP-4 (0.65 mm x 0.65 mm x 0.33 mm, pitch 0.35 mm) packages.

Simplified Schematic



Features

- Operating input voltage range : 1.65 V to 5.5 V
- Fixed output voltage range : 1 V to 3.3 V
- Output current : 450 mA
- Ultra high PSRR : Typ. 95 dB at f = 1 kHz
- Ultra low noise : 10 μV_{RMS}
- Ultra low quiescent current : 18 µA (Typ.)
- Dropout voltage : 180 mV (Typ.) at 450 mA
- High output voltage tolerance : ±1%
- Stable with ceramic capacitors 1 µF
- Build-in Quick output discharge function
- Over-Current protection
- Thermal shutdown protection
- Available in small SOT23-5, DFN1x1-4 and WLCSP0.65x0.65-4 packages

Applications

- Smartphones
- Battery powered equipment
- Tablets
- IP Cameras, image sensors and camcorders
- RF, PLL, VCO and clock power supply
- Portable medical equipment

Ordering Information

Ordering Information

Order PN	Marking ID	Package	Description
PJ20950A-xxS5	AA DNN	SOT23-5	With Output Discharge Halogen free RoHS compliant in T/R,3,000 pcs/Reel
PJ20950A-xxQZ1	A W	DFN1x1-4	With Output Discharge Halogen free RoHS compliant in T/R,10,000 pcs/Reel
PJ20950A-xxWS	AA W	WLCSP0.65x0.65-4	With Output Discharge Halogen free RoHS compliant in T/R,5,000 pcs/Reel

Note:

(1) MetaWells can meet RoHS 2.0/REACH requirement. So most package types MetaWells offers only states halogen free, instead of lead free.

Marking Information

Marking ID	Package	Definition
AA DNN	SOT23-5	AA : Product code (Ref. Note 1) DNN: D: Day code; NN: Serial Number
A W	DFN1x1-4	A : Product code +Dot code (Ref. Note 2) W: Week cod
AA W	DFN2x2-6	AA : Product code (Ref. Note 3) W: Week code

Note 1

SOT23-5								
Voltage	1.0V	1.2V	1.5V	1.8V	2.5V	2.8V	3.0V	3.3V
Options code "xx"	10	12	15	18	25	28	30	33
PJ20950A-xxS5 Marking	B2	B3	B4	B5	B6	B7	B8	B9

Note 2

DFN1X1-4								
Voltage	1.0V	1.2V	1.5V	1.8V	2.5V	2.8V	3.0V	3.3V
Options code "xx"	10	12	15	18	25	28	30	33
PJ20950A-xxQZ1 Marking	G	G	G	H	H	H	H	J
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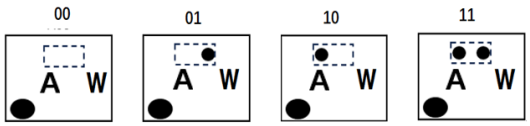
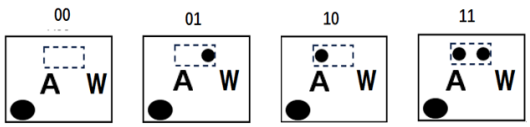
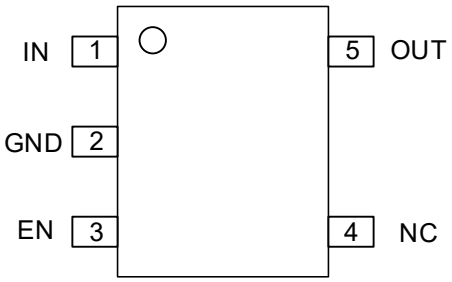
Dot								

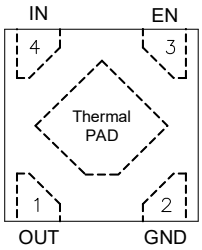
Note 3

WLCSP0.65x0.65-4								
Voltage	1.0V	1.2V	1.5V	1.8V	2.5V	2.8V	3.0V	3.3V
Options code "xx"	10	12	15	18	25	28	30	33
PJ20950A-xxWS Marking	A	A	A	A	B	B	B	B
Dot Code	00	10	01	11	00	10	01	11
Dot								

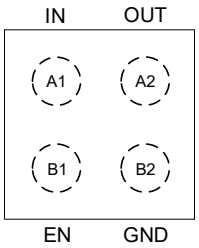
Pin Configuration



SOT23-5



DFN1x1-4



WLCSP0.65x0.65-4

Pin Assignment (Top View)

Pin Description

Number	Name	Description
OUT	O/P	Regulated output voltage. The output should be bypassed with a small 1 µF ceramic capacitor.
EN	I	Enable Pin. This pin has an internal pull-down resistor. A logic low reduces the supply current to less than 1 µA. Connect to logic “High” for normal operation.
GND	G	Power supply ground.
IN	I/P	Input voltage pin.
Thermal PAD	G	No connection

(1) I – Input; O – Output; P – Power; G – Ground.

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

Symbol	Parameter		Min	Max	Units
V_{IN}	Input voltage		-0.3	6.0	V
V_{OUT}	Output voltage		-0.3	6.0	V
V_{CE}	Chip enable input voltage		-0.3	6.0	V
I_{SC}	Output short circuit duration		Unlimited		s
T_L	Lead temperature range		260		°C
$T_{J(MAX)}$	Maximum junction temperature			150	°C
T_{STG}	Storage temperature range		-55	150	°C
$R_{\theta JA}$	Junction-to-ambient thermal resistance	SOT23-5	218		°C/W
		DFN1x1-4	198.1		°C/W
		WLCSP-4	108		°C/W

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Handling Ratings

Parameter	Definition	Min	Max	Units
ESD(1)	Human Body Model (HBM) ESD stress voltage(2)	-4	4	kV
	Charged Device Model (CDM)	-2	2	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. MetaWells does not recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter		Min	Typ	Max	Units
V_{IN}	Operating input voltage range	1.65		5.5	V
T_A	Operating ambient temperature	-40		125	°C

Electrical Characteristics

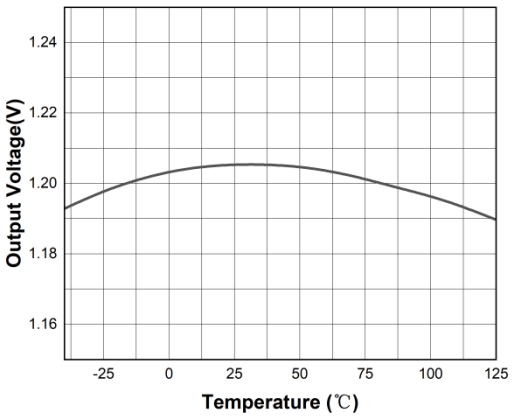
V_{IN} = $V_{OUT(NOM)}$ + 1 V; I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1 µF, V_{EN} = 1.0 V. T_A = -40°C to 125°C, unless otherwise noted. Typical value is tested at T_A = +25°C.

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_{IN}	Input voltage			1.65		5.5	V
$V_{OUT(ACCURACY)}$	Output voltage accuracy	V_{IN} =$V_{OUT(NOM)}$ + 1 V, I_{OUT}=1 mA, T_A = 25°C, V_{OUT} < 2 V		-20		+20	mV
		V_{IN} =$V_{OUT(NOM)}$ + 1 V, I_{OUT}=1 mA, T_A = 25°C, V_{OUT} ≥ 2 V		-1		+1	%
$Line_{REG}$	Line regulation	$V_{OUT(NOM)}$ +1 V < V_{IN} ≤ 5.5 V, T_A = 25°C				6	mV
$Load_{REG}$	Load regulation	I_{OUT} = 1 mA to 450 mA, T_A = 25°C	SOT23-5			36	mV
			DFN1x1-4			30	mV
			WLCSP-4		2		mV
V_{DO}	Dropout voltage	I_{OUT} = 450 mA, T_A = 25°C, SOT23-5	$V_{OUT(NOM)}$ = 1.8 V		300	370	mV
			$V_{OUT(NOM)}$ = 2.0 V		250	320	
			$V_{OUT(NOM)}$ = 2.5 V		210	260	
			$V_{OUT(NOM)}$ = 2.8 V		200	250	
			$V_{OUT(NOM)}$ = 3.0 V		180	225	
			$V_{OUT(NOM)}$ = 3.3 V		170	215	
V_{DO}	Dropout voltage	I_{OUT} = 450 mA, T_A = 25°C, DFN1x1-4	$V_{OUT(NOM)}$ = 1.8 V		270	335	mV
			$V_{OUT(NOM)}$ = 2.0 V		215	285	
			$V_{OUT(NOM)}$ = 2.5 V		185	225	
			$V_{OUT(NOM)}$ = 2.8 V		170	210	
			$V_{OUT(NOM)}$ = 3.0 V		155	190	
			$V_{OUT(NOM)}$ = 3.3 V		145	180	
V_{DO}	Dropout voltage	I_{OUT} = 450 mA, T_A = 25°C, WLCSP-4	$V_{OUT(NOM)}$ = 1.8 V		235	300	mV
			$V_{OUT(NOM)}$ = 2.0 V		180	250	
			$V_{OUT(NOM)}$ = 2.5 V		150	190	
			$V_{OUT(NOM)}$ = 2.8 V		135	175	
			$V_{OUT(NOM)}$ = 3.0 V		120	150	
			$V_{OUT(NOM)}$ = 3.3 V		110	145	
I_{CL}	Output current limit	V_{OUT} = 90% $V_{OUT(NOM)}$		450	700		mA
I_{SC}	Short circuit current	V_{OUT} = 0 V			180		mA
I_Q	Quiescent current	I_{OUT}=0 mA, T_A = 25°C			18	25	µA
I_{DIS}	Shutdown current	V_{EN} ≤ 0.4 V, V_{IN} = 4.8 V, T_A = 25°C			0.01	1	µA
V_{ENH}	EN pin threshold voltage	EN logic high voltage		1			V
V_{ENL}	EN pin threshold voltage	EN logic low voltage				0.4	V
I_{EN}	EN pull-down current	V_{EN} = 4.8 V, T_A = 25°C			0.1	0.5	µA

Symbol	Parameter	Condition		Min	Typ	Max	Unit
PSRR	Power supply rejection ratio	I_{OUT} = 10 mA	f = 100 Hz		91		dB
			f = 1 kHz		95		
			f = 10 kHz		75		
			f = 100 kHz		55		
			f = 1 MHz		56		
V_{NOISE}	Output noise voltage	f = 10 Hz to 100 kHz	I_{OUT} = 1 mA		14		µVrms
			I_{OUT} = 450 mA		10		
R_{DIS}	Active output discharge resistance	V_{EN} < 0.4 V			100		Ω
t_{ON}	Turn on time	C_{OUT} = 1 µF, from assertion of V_{EN} to V_{OUT} = 95% $V_{OUT(NOM)}$			250		µS
$Tran_{LINE}$	Line transient	V_{IN} = ($V_{OUT(NOM)}$ + 1 V) to ($V_{OUT(NOM)}$ + 1.6 V) in 30 µs, I_{OUT} = 1 mA		-1			mV
		V_{IN} = ($V_{OUT(NOM)}$ + 1.6 V) to ($V_{OUT(NOM)}$ + 1 V) in 30 µs, I_{OUT} = 1 mA				+1	
$Tran_{LOAD}$	Load transient	I_{OUT} = 1 mA to 450 mA in 10 µs		-40			mV
		I_{OUT} = 450 mA to 1 mA in 10 µs				+40	
T_{SDH}	Thermal shutdown threshold	Temperature rising			160		°C
T_{SDL}		Temperature falling			140		°C

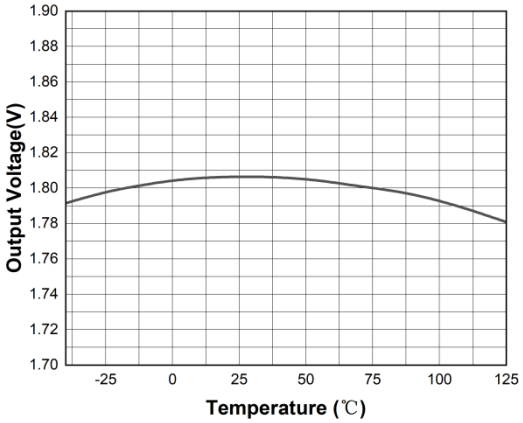
(1) Specifications subject to change without notice.

Typical Performance Characteristic



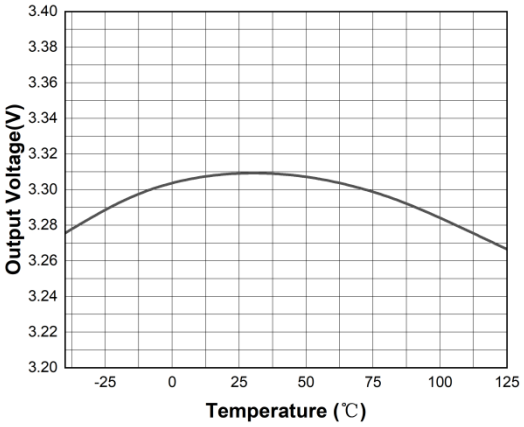
V_{OUT} = 1.2 V, C_{IN} = C_{OUT} = 1 uF, I_{OUT} = 1 mA

Figure-1. Output Voltage vs Temperature



V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 1 uF, I_{OUT} = 1 mA

Figure-2. Output Voltage vs Temperature



V_{OUT} = 3.3 V, C_{IN} = C_{OUT} = 1 uF, I_{OUT} = 1 mA

Figure-3. Output Voltage vs Temperature

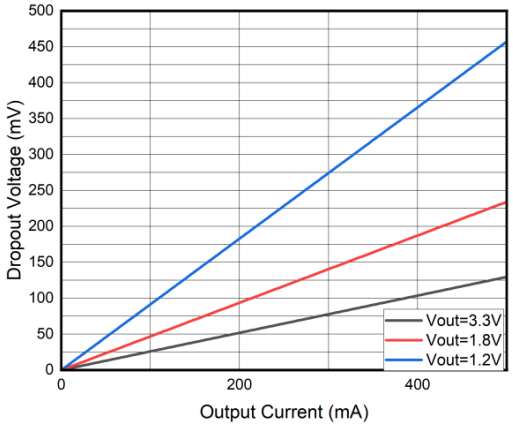
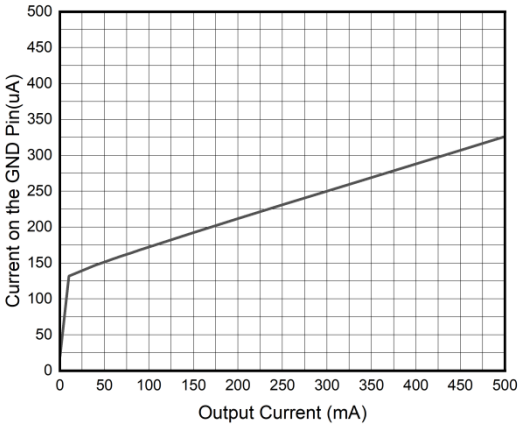
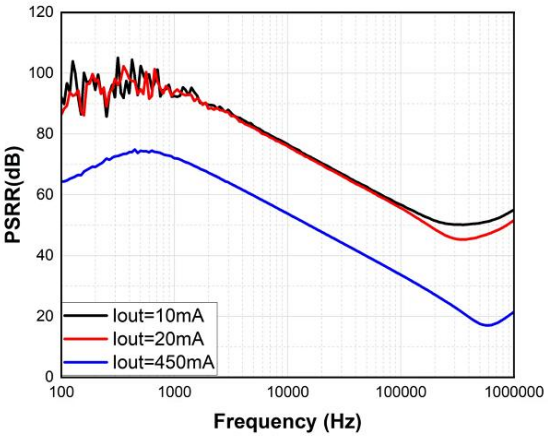


Figure-4. Dropout Voltage vs Output Current



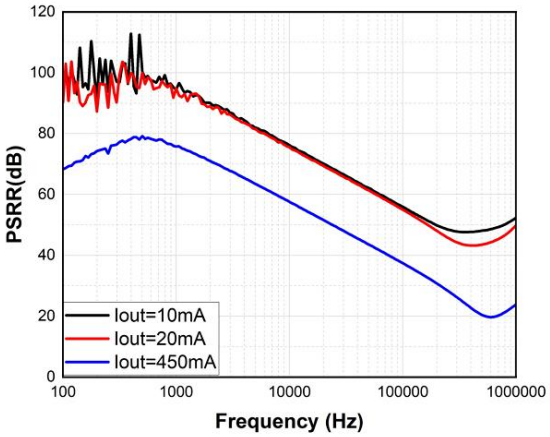
C_{OUT} = 1 uF, V_{IN} = 2.2 V, V_{OUT} = 1.2 V

Figure-5. Current on the GND Pin vs Output Current



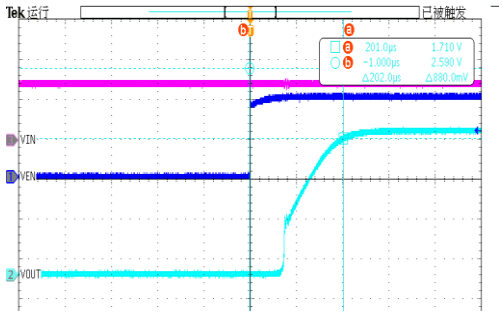
V_{IN} = 2.8 V + 200 mV_{P-P}, V_{OUT} = 1.8 V, C_{OUT} = 1 uF

Figure-6.PSRR vs Frequency



V_{IN} = 4.3 V + 200 mV_{P-P}, V_{OUT} = 3.3 V, C_{OUT} = 1 uF

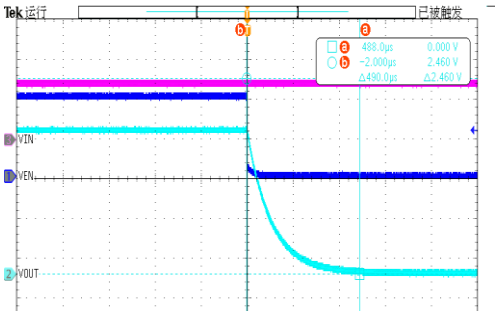
Figure-7. PSRR vs Frequency



V_{IN} = 2.8 V, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} =1 uF, I_L = 1 mA

From assertion of V_{EN} to V_{OUT} = 95% $V_{OUT(NOM)}$

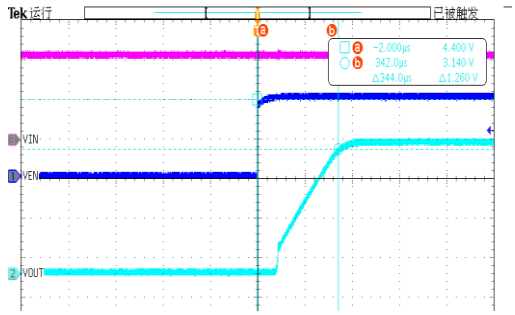
Figure-8. Turn On Time



V_{IN} = 2.8 V, V_{OUT} = 1.8 V, C_{IN} = C_{OUT} = 1 uF, I_L = 1 mA

From assertion of V_{EN} to V_{OUT} = 0

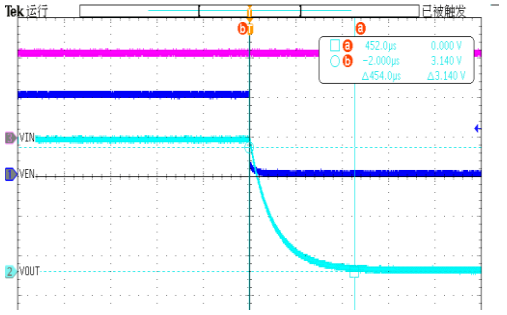
Figure-9. Turn Off Time



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{IN} = C_{OUT} = 1 uF, I_L = 1 mA

From assertion of V_{EN} to V_{OUT} = 95% $V_{OUT(NOM)}$

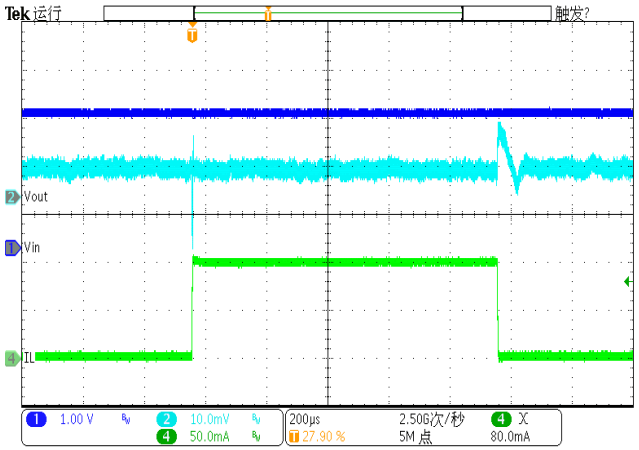
Figure-10. Turn On Time



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{IN} = C_{OUT} = 1 uF, I_L = 1 mA

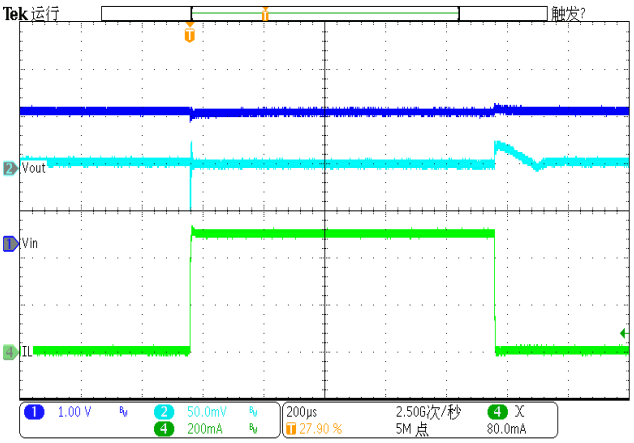
From assertion of V_{EN} to V_{OUT} = 0

Figure-11. Turn Off Time



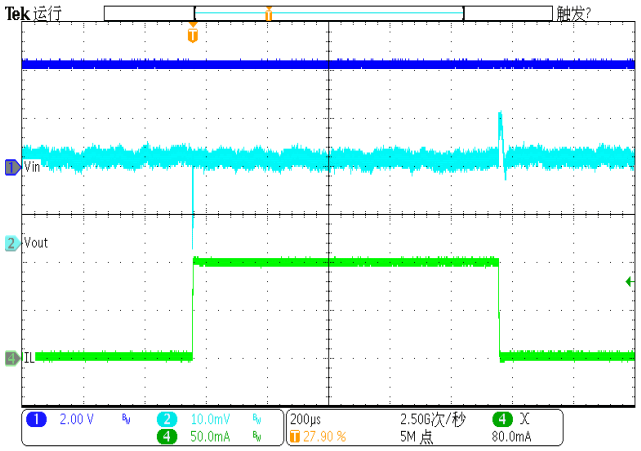
V_{IN} = 2.8 V, V_{OUT} = 1.8 V, C_{OUT} = 1 uF, I_{OUT} = 1 mA to 100 mA

Figure-12. Load Transient Response



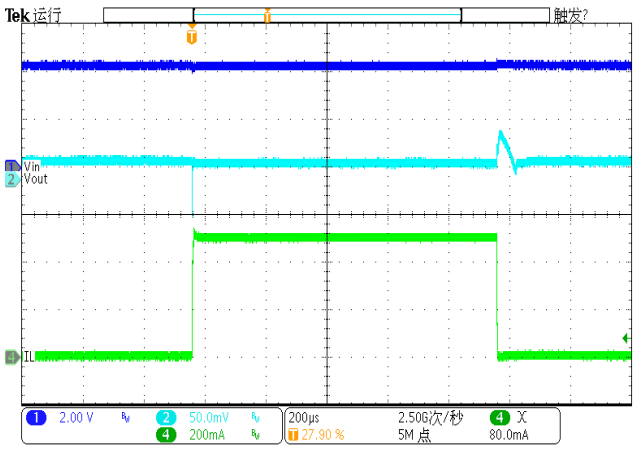
V_{IN} = 2.8 V, V_{OUT} = 1.8 V, C_{OUT} = 1 uF, I_{OUT} = 1 mA to 500 mA

Figure-13. Load Transient Response



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 1 uF, I_{OUT} = 1 mA to 100 mA

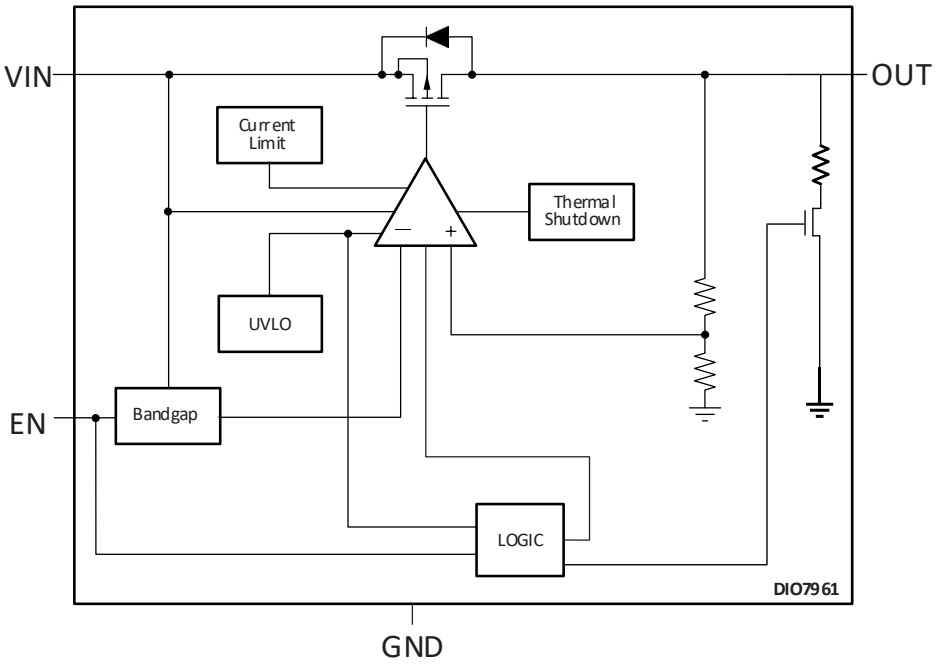
Figure-14. Load Transient Response



V_{IN} = 4.3 V, V_{OUT} = 3.3 V, C_{OUT} = 1 uF, I_{OUT} = 1 mA to 500 mA

Figure-15. Load Transient Response

Functional Block Diagram



Application Information

Overview

The PJ20950A series of LDO linear regulators are ultra-high PSRR and low noise devices with excellent line and load transient performance. These LDOs are designed for power-sensitive applications. A precision bandgap and error amplifier provide overall 1% accuracy. Low output noise, very high PSRR, and low dropout voltage make this device ideal for most battery-operated handheld equipment. The PJ20950A is fully protected in case of current overload, output short circuit, and overheating.

Input Capacitor Selection (C_{IN})

The PJ20950A is specifically designed to work with a standard ceramic input capacitor. An Input capacitor connected as close as possible is necessary to ensure device stability. The X7R or X5R capacitor should be used because of its minimal variation in values and equivalent series resistance (ESR) over temperature. The value of the input capacitor should be 1 µF or larger to ensure the optimum dynamic performance. As far as unwanted AC signals or noise modulated onto constant input voltage are concerned, this capacitor will provide a low impedance path for them. Use ceramic capacitors for the best because they have low ESR and ESL. The input capacitor has no ESR restrictions as long as it can limit the influence of input trace inductance and source resistance during sudden load current changes.

Output Capacitor Selection (C_{OUT})

The PJ20950A requires an output capacitance. The value of the input capacitor should be 1 µF or larger for stability. Use X5R-type or X7R-type ceramic capacitor because of its minimal variation in values and ESR over temperature.

An output capacitor with a maximum value of ESR less than 2 ohms is for the best though there are no requirements for the minimum ESR of the capacitor. With larger output capacitors and lower ESR, one can expect better load transient response or high frequency PSRR, which is why tantalum capacitors on the output is a good option. Low temperatures increase the equivalent series resistance of tantalum capacitors.

Enable Operation

The PJ20950A uses the EN pin to enable or disable its device and discharge function. If the EN pin voltage is pulled below 0.4 V, the device is guaranteed to be disabled. The active discharge transistor in the devices with the active discharge feature is activated and the output voltage V_{OUT} is pulled to GND through an internal circuitry with an effective resistance of about 100 ohms.

If the EN pin voltage is higher than 1.0 V the device is guaranteed to be enabled. The internal active discharge circuitry is switched off and the desired output voltage is available at the output pin. The EN pin should be connected directly to the input pin when there is no need for the EN function.

Output Current Limit

The PJ20950A internal current limit helps to protect the regulator during fault conditions. Output Current is internally limited within the IC to a typical 700 mA.

During the current limit, the output sources a fixed amount of current that is largely independent of the output voltage. In such a case, the output voltage is not regulated, and $V_{OUT} = I_{CL} \times R_{LOAD}$. The PMOS pass transistor dissipates $(V_{IN} – V_{OUT}) \times I_{CL}$ until the thermal shutdown is triggered and the device turns off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between the current limit and thermal shutdown.

The PMOS pass element in the PJ20950A has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

Thermal Shutdown

When the chip temperature exceeds the Thermal Shutdown point (T_{SD} = 160°C typical), the device goes to the disabled state and the output voltage is not delivered until the die temperature decrease to 140°C.

The Thermal Shutdown feature protects from a catastrophic device failure at accidental overheating. Using this protection in place of proper heat sinking is not recommended.

Dropout Voltage

The PJ20950A uses a PMOS pass transistor to achieve low dropout. When $(V_{IN} – V_{OUT})$ is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} scales approximately with output current because the PMOS device behaves as a resistor in dropout.

Power Dissipation and Heat Sinking

The design and layout of the board determine how much power can be dissipated by the device. A part's junction temperature rise is affected by how the mounting pads are configured on the PCB, the material of the PCB, and the ambient temperature. The maximum power dissipation the PJ20950A device can handle is given by Equation (1).

$$P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}} \quad (1)$$

The power dissipated by the PJ20950A device for given application conditions can be calculated from the following Equation (2).

$$P_D \approx V_{IN} \times I_{GND} + I_{OUT} \times (V_{IN} - V_{OUT}) \quad (2)$$

Reverse Current

Reverse current flows through the body diode on the pass element instead of the normal conducting channel in the case that $V_{OUT} > V_{IN}$. Excessive reverse current can damage this device, which is why the device may require additional external protection when there could be an extended reverse current condition.

Power Supply Rejection Ratio

The PJ20950A features a very high Power Supply Rejection ratio to meet the requirements of RF and analog circuits. By the selection of the C_{OUT} capacitor and proper PCB layout, the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned.

Turn−On Time

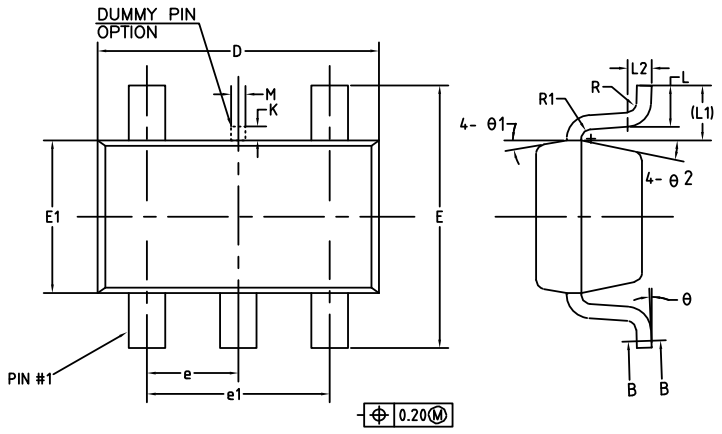
The turn−on time is defined as the time period from EN activation to the point in which V_{OUT} will reach 98% of its nominal value. The time is dependent on various application conditions such as $V_{OUT(NOM)}$, C_{OUT}, T_A.

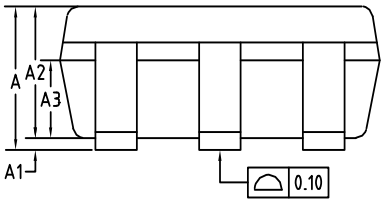
PCB Layout Recommendations

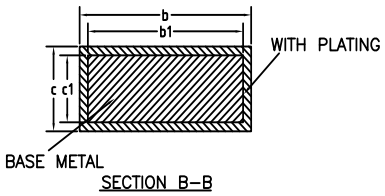
An optimal layout can greatly improve transient performance, PSRR, and noise. C_{IN} and C_{OUT} capacitors should be placed near device pins and PCB traces should be widely spaced for excellent performance. Place ground return connections to the input and output capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. For better power dissipation and lower device temperatures, tie the exposed pad to the GND pin.

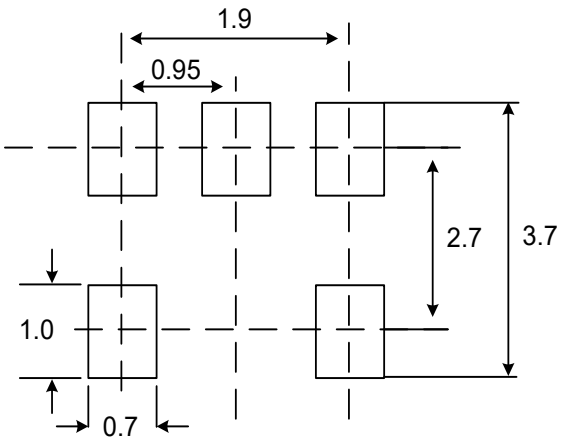
Package Outline Dimension – SOT23-5

SOT23-5 Unit (mm)







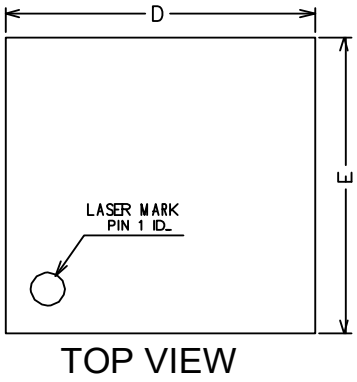


RECOMMENDED LAND PATTERN

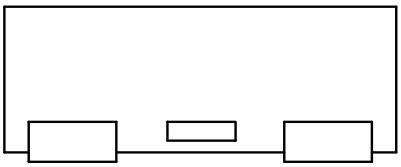
Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Typ**	**Max**
A	-	-	1.25
A1	0	-	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	-	0.45
b1	0.35	0.38	0.41
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e 1	1.80	1.90	2.00
K	0	-	0.25
L	0.30	0.40	0.60
L1		0.59 REF	
L2		0.25 BSC	
M	0.10	0.15	0.25
R	0.05	-	0.20
R1	0.05	-	0.20
θ	0°	-	8°
θ1	8°	10°	12°
θ2	10°	12°	14°

Package Outline Dimension – DFN1x1-4

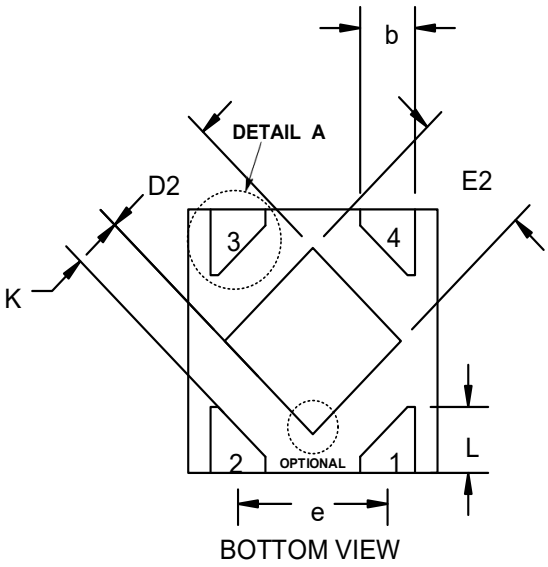
DFN1x1-4 Unit (mm)



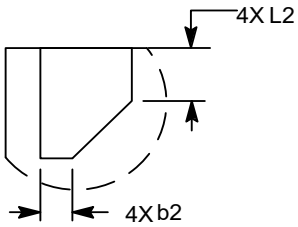
TOP VIEW



SIDE VIEW

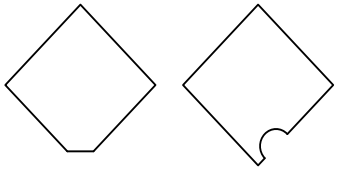


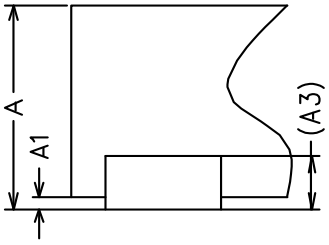
BOTTOM VIEW

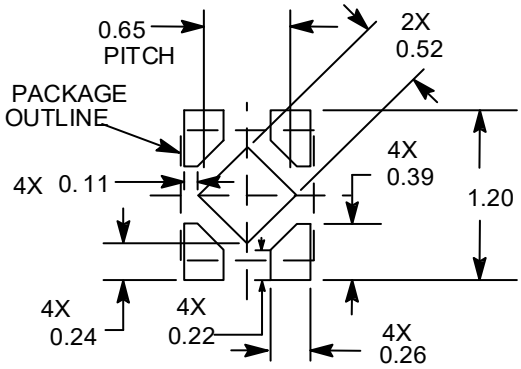


DETAIL A

Two options:





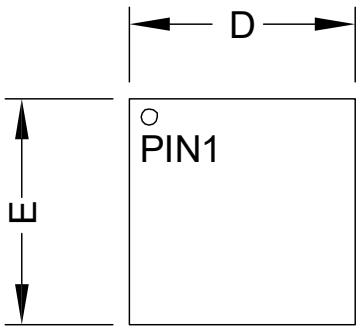


RECOMMENDED LAND PATTERN (Unit: mm)

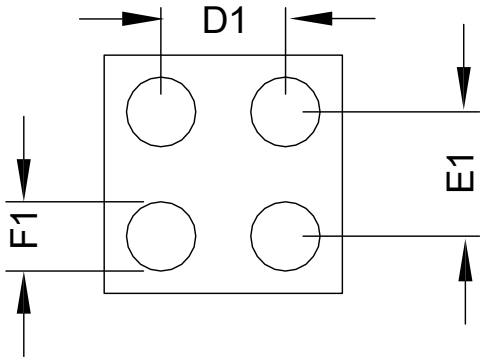
Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.34	0.37	0.40
A1	0	0.02	0.05
A3		0.10 REF	
b	0.17	0.22	0.27
D	0.95	1.00	1.05
E	0.95	1.00	1.05
D2	0.43	0.48	0.53
E2	0.43	0.48	0.53
L	0.20	0.25	0.30
e	0.60	0.65	0.70
K	0.15	-	-
L2	0.07	0.12	0.17
b2	0.02	-	0.12

Package Outline Dimension – WLCSP0.65x0.65-4

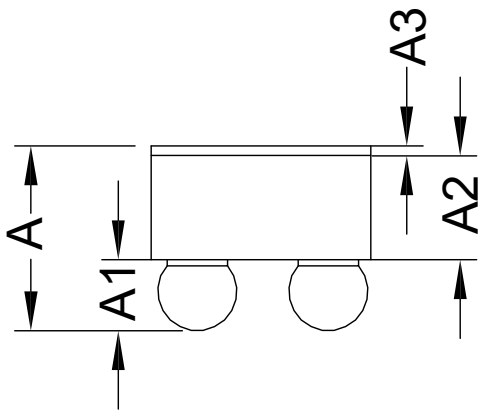
WLCSP0.65x0.65-4 Unit (mm)



TOP VIEW
Ball Down



BOTTOM VIEW
Ball Up



SIDE VIEW

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.270	0.300	0.330
A1	0.050	0.060	0.070
A2	0.200	0.215	0.230
A3	0.020	0.025	0.030
D	0.620	0.645	0.670
E	0.620	0.645	0.670
F1	0.189	0.195	0.201
D1	0.350 BSC.		
E1	0.350 BSC.		

Version History

Version	Date	Changes
Rev.1.0	2026-01-13	Initial release

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