PJ20703A Datasheet

5.5V, 300mA, Ultra Low Noise And Ultra Low I_Q LDO In a Tiny Package

Version：Rev.1.0

Release Date：2025-12-10

MetaWells Co., Ltd.

www.MetaWells.com

General Description

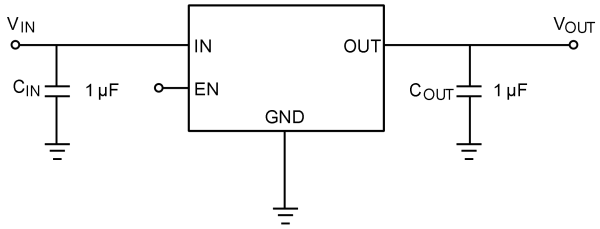
The PJ20703A ultra-low quiescent current regulator features low dropout voltage and low current in the standby mode. With less than 500 nA quiescent current at no load, the PJ20703A is ideally suited for standby micro-control-unit systems, especially for always-on applications like portable, and other battery-operated systems. The PJ20703A retains all the features that are common to low dropout regulators including a low dropout PMOS pass device, short circuit protection, and thermal shutdown.

The PJ20703A has a 5.5 V maximum operating voltage limit, a -40°C to 125°C operating temperature range, and ±2% output voltage tolerance.

Features

- Operating input voltage range : 2.5 V to 5.5 V
- Output voltage range : 1.2 V to 5.0 V
- Output current : 300 mA
- Ultra-low quiescent current : 300 nA (Typ.)
- Dropout voltage : 500 mV (Typ.) at I_{OUT} = 300 mA
- PSRR : 60 dB at 1 kHz, I_{OUT} = 10 mA
- Output voltage tolerance : ±2%
- Stable with ceramic capacitors 1 µF
- Internal Short-Circuit Current Limit
- Internal Thermal Overload Protection
- Integrated output auto-discharge
- Available in DFN1x1-4 and SOT23-5 packages
- These devices are Pb−Free, halogen Free/BFR free, and are RoHS compliant

Simplified Schematic



Applications

- Portable, Battery Powered Equipment
- Ultra Low Power Microcontroller
- Notebook computers

Ordering Information

Ordering Information

Order number	Marking ID	Option	Package	Description
PJ20703A-xxS5	AABDNN	With Output Discharge	SOT23-5	Halogen Free in T/R, 3000 pcs/Reel
PJ20703A-xxQZ1	A W		DFN1x1-4	Halogen Free in T/R, 10000 pcs/Reel

Output Voltage Options							
Option Code "xx"	12	18	25	0.1 V / Step	28	33	50
Voltage	1.2 V	1.8 V	2.5 V		2.8 V	3.3 V	5.0 V

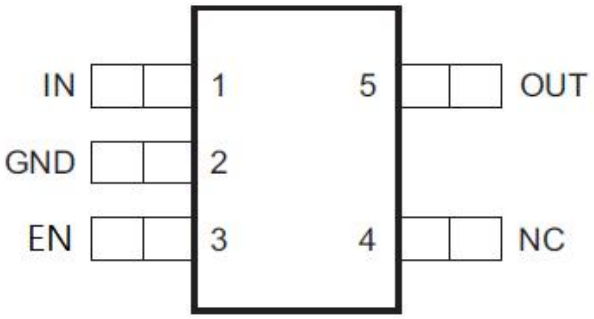
Note:

(1) MetaWells can meet RoHS 2.0/REACH requirement. So most package types MetaWells offers only states halogen free, instead of lead free.

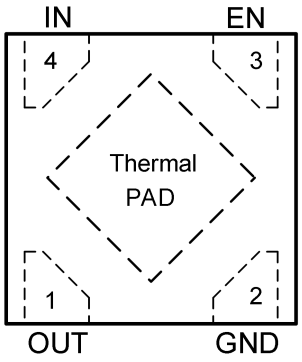
Marking Information

Marking	Package	Definition
AABDNN	SOT23-5	AA: Product code B: Version D: Day code NN: Serial No
A W	DFN1x1-4	A: Product code W: Week code

Pin Configuration



SOT23-5



DFN1x1-4

Pin Assignment (Top View)

Pin Description

Terminal Name	I/O(1)	Description
OUT	O/P	Output voltage pin.
EN	I	Enable pin. This pin has an internal pull-down current source. Connect to logic “High” for normal operation.
GND	G	Power supply ground.
IN	I/P	Input voltage pin.

(1) I – Input; O – Output; P – Power; G – Ground.

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

Parameter			Min	Max	Units
Voltage range at terminals	IN, OUT, EN		-0.3	6.5	V
I_{OUT}	Output Current		300		mA
T_L	Lead temperature range (Soldering, 10 sec)		300		°C
$T_{J(MAX)}$	Maximum junction temperature			150	°C
T_{STG}	Storage temperature range		-65	150	°C
$R_{\theta JA}$	Junction-to-ambient thermal resistance	DFN1x1-4	226		°C/W
		SOT23-5	218.1		°C/W

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Handling Ratings

Parameter	Description	Min	Max	Units
ESD(1)	Human Body Model (HBM) ESD stress voltage(2)	-2	2	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. MetaWells does not recommend exceeding them or designing to Absolute Maximum Ratings.

Parameter		Min	Typ	Max	Units
V_{IN}	Operating input voltage range	2.5		5.5	V
T_J	Operating junction temperature range	-40		125	°C

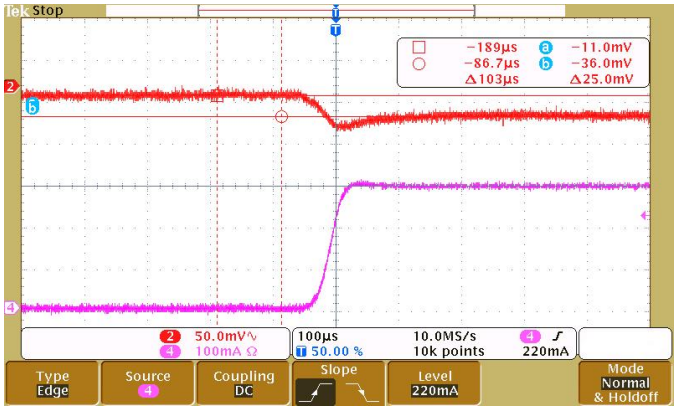
Electrical Characteristics

V_{IN} = V_{OUT} + 1 V, I_{OUT} = 1 mA, C_{IN} = C_{OUT} = 1.0 μF. Typical value is tested at T_A = +25°C, unless otherwise noted.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Input voltage		2.5		5.5	V
V_{OUT}	Output voltage	T_A = 25°C	1.2		5.0	V
△V_{OUT}	Output Voltage Accuracy	V_{IN} = 5 V	-2		+2	%
$Line_{REG}$	Line regulation	V_{IN} = V_{OUT} + 1 V to 5.5 V		0.6	1.5	%
$Load_{REG}$	Load regulation	I_{OUT} = 1 mA to 150 mA			2.5	%
		I_{OUT} = 1 mA to 300 mA			3	%
I_{CL}	Output current limit		360	560		mA
I_Q	Quiescent current	No load		300	500	nA
I_{STB}	Standby current	V_{EN} = 0 V, T_A = 25°C		0.1	0.5	μA
V_{ENH}	EN pin threshold voltage	EN logic high voltage	0.6			V
V_{ENL}	EN pin threshold voltage	EN logic low voltage			0.2	V
PSRR	Power supply rejection rate	f = 1 kHz, I_{OUT} = 10 mA		60		dB
R_{LOW}	Active output discharge resistance	V_{IN} = 5.5 V, V_{EN} = 0 V		1.5		kΩ
T_{SD}	Thermal shutdown temperature	Temperature increasing from T_A = 25°C		150		°C
T_{SDH}	Thermal shutdown hysteresis	Temperature falling from T_{SD}		20		°C

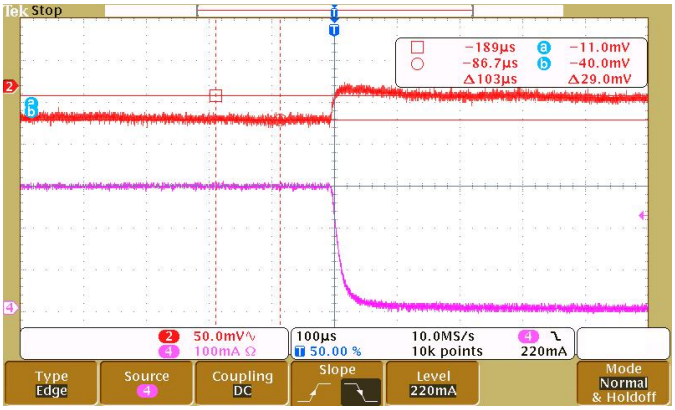
Typical Performance Characteristics

V_{IN} = V_{OUT} + 1 V, I_{OUT} = 1 mA, V_{OUT} = 3.3 V, C_{IN} = C_{OUT} = 1.0 µF. Typical value is tested at T_A = +25°C, unless otherwise noted.



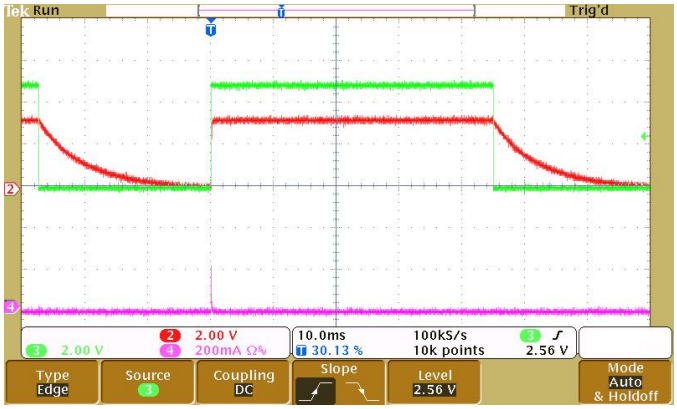
CH2 : V_{OUT}, CH4 : I_{OUT}

Figure 1. Load Transient (1 mA to 300 mA)



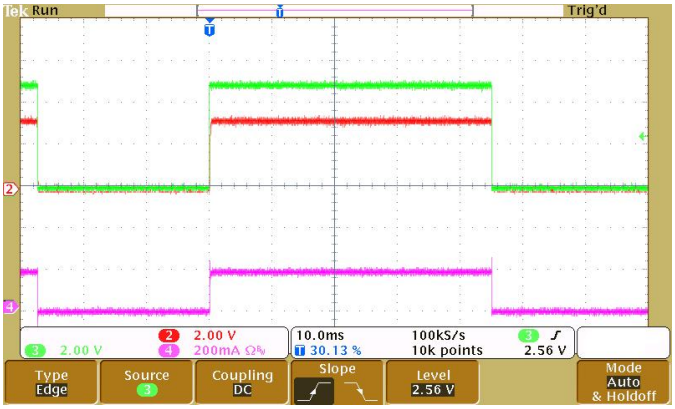
CH2 : V_{OUT}, CH4 : I_{OUT}

Figure 2. Load Transient (300 mA to 1 mA)



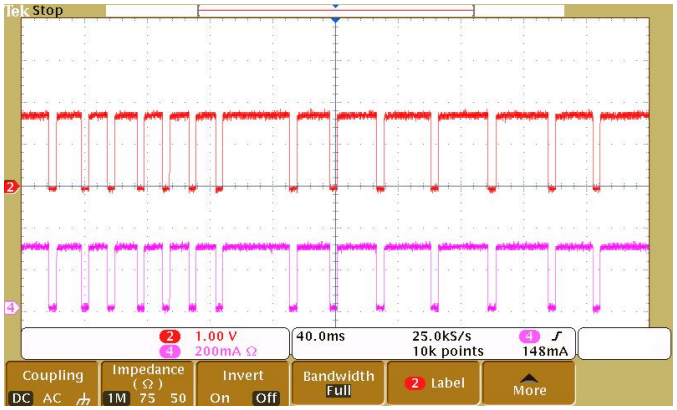
CH2 : V_{OUT}, CH3 : EN, CH4 : I_{OUT}

Figure 3. EN Start-up (no load)



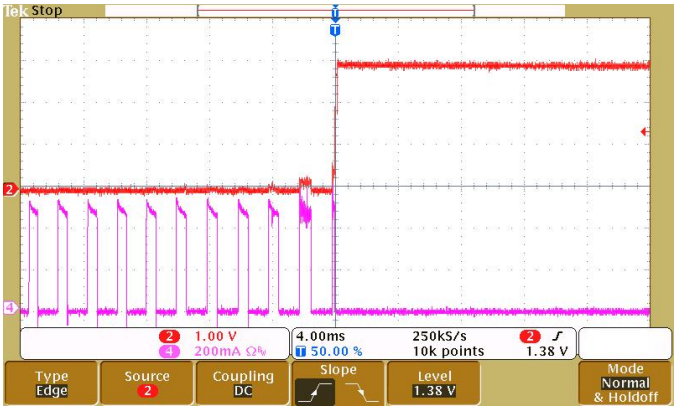
CH2 : V_{OUT}, CH3 : EN, CH4 : I_{OUT}

Figure 4. EN Start-up (200 mA load)



CH2 : V_{OUT}, CH4 : I_{OUT}

Figure 5. V_{IN} = 5 V, V_{OUT} = 1.8 V, heavy load OTP



CH2 : V_{OUT}, CH4 : I_{OUT}

Figure 6. V_{OUT} short to GND and release

V_{IN} = V_{OUT} + 1 V, I_{OUT} = 1 mA, V_{OUT} = 3.3 V, C_{IN} = C_{OUT} = 1.0 µF, Typical value is tested at T_A = +25°C, unless otherwise noted.

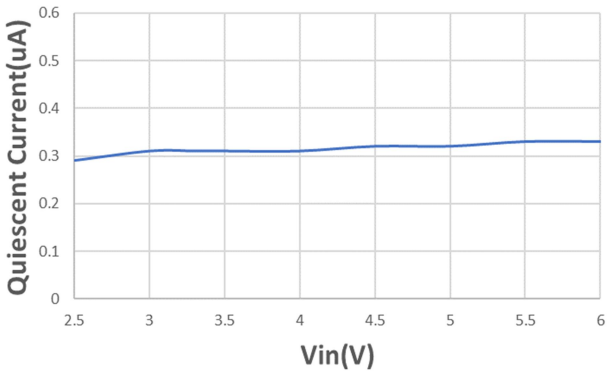


Figure 7. I_Q vs V_{IN} (I_{OUT} = 0 mA)

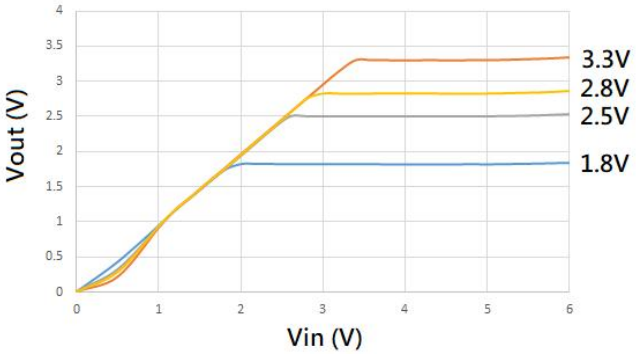


Figure 8. V_{OUT} vs V_{IN} (I_{OUT} = 1 mA)

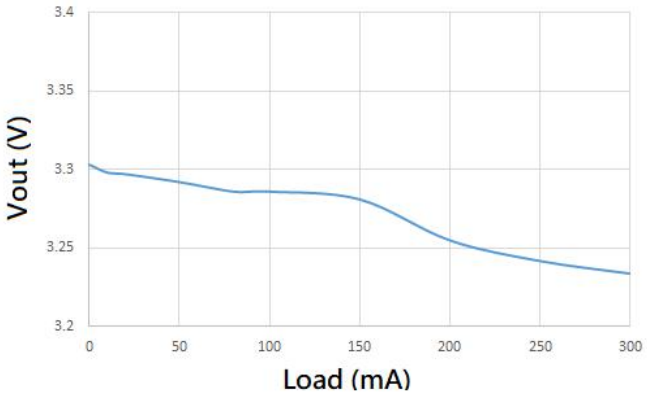


Figure 9. V_{OUT} vs Load

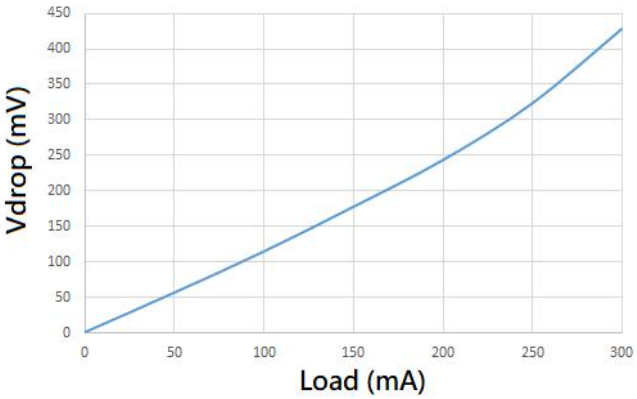


Figure 10. V_{DROP} vs Load

Functional Block Diagram

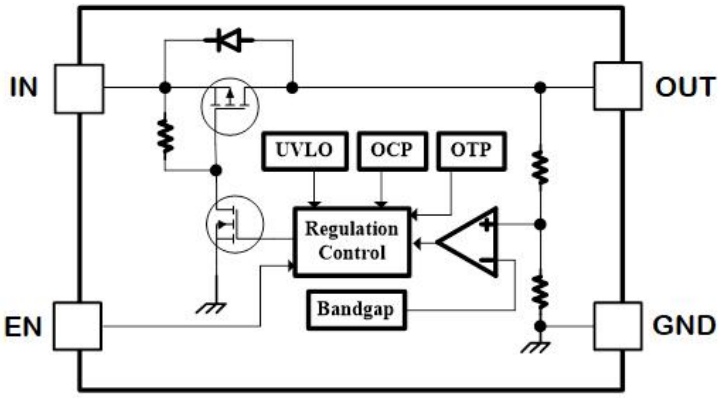


Figure 11. PJ20703A Function Block

Operation Information

Basic Operation

The PJ20703A is a high performance positive low dropout (LDO) regulator designed for applications requiring low dropout voltage, low noise and low quiescent current that can supply up to 300mA output current. The input voltage range is from 2.5 V to 5.5 V.

The PJ20703A features a precise 2% output regulation. The output voltage is available from 1.2 V to 5.0 V in 100 mV steps.

The minimum required output capacitance for stable operation is 1uF (X5R or X7R) effective capacitance after consideration of the temperature and voltage coefficient of the capacitor.

Enable and Shutdown Operation

The PJ20703A goes into shutdown mode when the EN pin is in a logic low condition. In this condition, the pass transistor, error amplifier, and bandgap are all turned off, reducing the supply current to only 0.1 μA (max.). If the shutdown mode is not required, the EN pin can be directly tied to V_{IN} pin to keep the LDO on.

Over-Temperature Protection (OTP)

The over-temperature protection function will turn off the P-MOSFET when the junction temperature exceeds 150°C (typ.). Once the junction temperature cools down by approximately 20°C (typ.), the regulator will automatically resume operation.

Current-limit Protection

The PJ20703A provides current limit function to prevent the device from damages during overload or shorted-circuit condition. This current is detected by an internal sensing transistor.

Error Amplifier

The Error Amplifier compares the internal reference voltage with the output feedback voltage from the internal divider, and controls the Gate voltage of P-MOSFET to support good line regulation and load regulation at output voltage.

Output Automatic Discharge

The PJ20703A output employs an internal 1.5 kΩ (typ.) pull-down resistance to discharge the output when the EN pin is low, and the device is disabled.

Application Information

Overview

Like any low dropout linear regulator, the PJ20703A's external input and output capacitors must be properly selected for stability and performance. Use a 1 μF (X5R or X7R) or larger input capacitor and place it close to the IC's V_{IN} and GND pins. Any output capacitor meeting the minimum 1 mΩ ESR (Equivalent Series Resistance) and effective capacitance larger than 1 μF (X5R or X7R) requirement may be used. Place the output capacitor close to the IC's V_{OUT} and GND pins. Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

Current Limit

The PJ20703A contains an independent current limiter, which monitors and controls the pass transistor's gate voltage, limiting the output current to 0.56 A (typ.). The output can be shorted to ground indefinitely without damaging the part.

Dropout Voltage

The dropout voltage refers to the voltage difference between the V_{IN} and V_{OUT} pins while operating at specific output current. The dropout voltage V_{DROP} can also be expressed as the voltage drop on the pass-FET at specific output current (I_{RATED}) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized as an resistance $R_{DS(ON)}$. Thus the dropout voltage can be defined as ($V_{DROP} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{RATED}$).

For normal operation, the suggested LDO operating range is ($V_{IN} > V_{OUT} + 0.2$ V) for good transient response and PSRR ability. Conversely, operating at the ohmic region will degrade these performance severely. Additionally, the output of PJ20703A is automatically discharged through an internal 1.5 kΩ pull-down resistance when the EN pin is low and the device is disabled.

Enable Operation

The PJ20703A has an EN pin to turn on or turn off the regulator, When the EN pin is in logic high, the regulator will be turned on. The shutdown current is almost 0 μA typical. The EN pin may be directly tied to V_{IN} to keep the part on. The Enable input is CMOS logic and cannot be left floating.

Minimum Operating Input Voltage (V_{IN})

The PJ20703A does not include any dedicated UVLO circuitry. The PJ20703A at least 2.2 V. The output voltage is not regulated until V_{IN} has reached at least the greater of 2.2 V or (V_{OUT} + 0.2V)

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}, \text{ and } P_{D(MAX)} = \frac{[T_{J(MAX)} - T_A]}{R_{\theta JA}}$$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction to ambient thermal resistance.

For recommended operating condition specifications the maximum junction temperature is 125°C and T_A is the ambient temperature. The junction to ambient thermal resistance, θ_{JA}, is layout dependent. For DFN1x1-4 package,

the thermal resistance, θ_{JA}, is 226°C/W on a two-layer MetaWells evaluation board. For SOT23-5 package, the thermal resistance, θ_{JA}, is 218.1°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by the following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (226°C/W) = 0.44 W for DFN1x1-4 package.

$P_{D(MAX)}$ = (125°C − 25°C) / (218.1°C/W) = 0.45 W for SOT23-5 package.

The maximum power dissipation depends on the operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance, θ_{JA}. The de-rating curve in Figure (below) allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

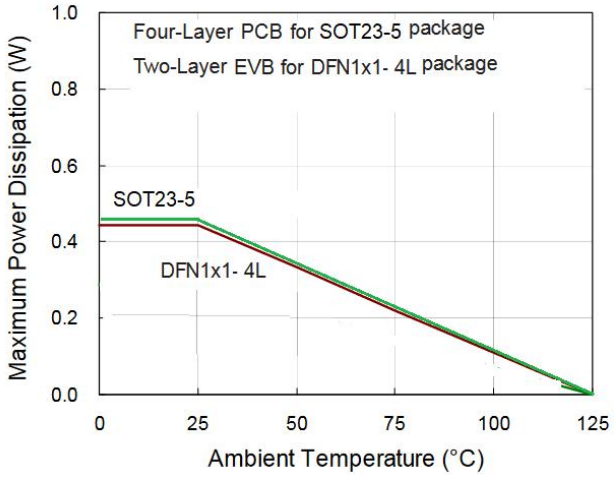


Figure 12. Power dissipation

Layout Considerations

The dynamic performance of the PJ20703A is dependent on the layout of the PCB. PCB layout practices that are adequate for typical LDOs may degrade the PSRR, noise, or transient performance of the PJ20703A. Best performance is achieved by placing C_{IN} and C_{OUT} on the same side of the PCB as the PJ20703A, and as close to the package as possible is practical. The ground connections for C_{IN} and C_{OUT} must be back to the PJ20703A ground pin using a copper trace as wide and short as possible. Connections using long trace lengths, narrow trace widths, and/or connections through vias must be avoided. These added parasitic inductances and resistance may result in inferior performance especially during transient conditions.

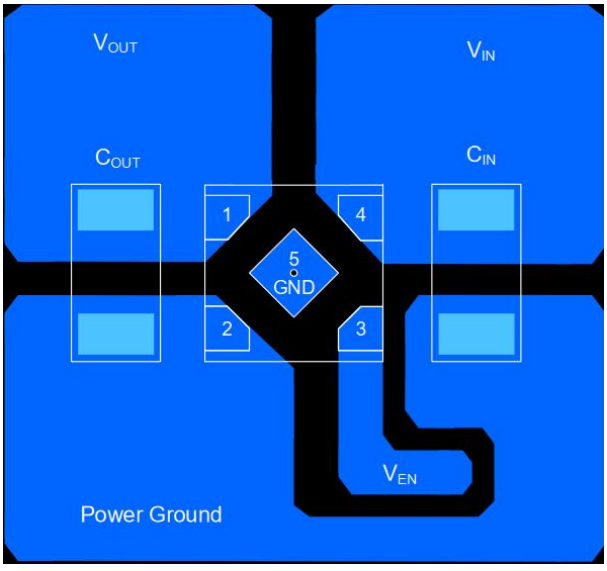


Figure 13. DFN1x1-4 Layout recommendation

GND pad (2) and (5) connect to second layer ground path by via to increase cooling area directly.

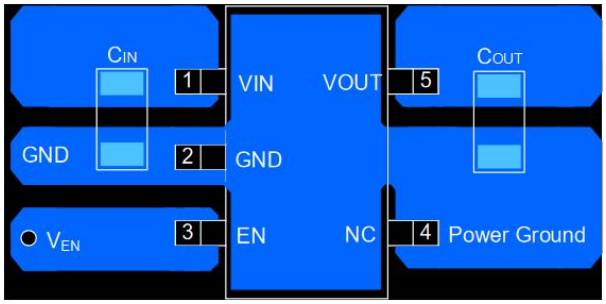
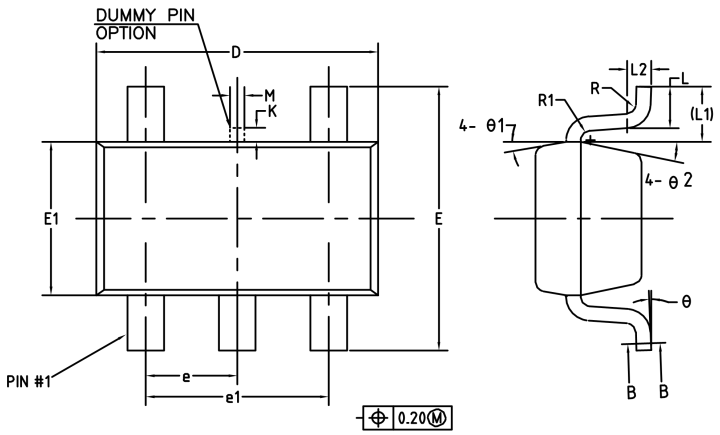


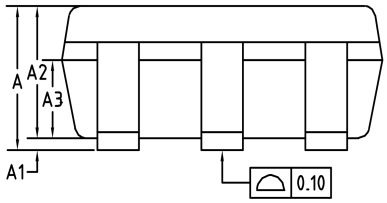
Figure 14. SOT23-5 Layout recommendation

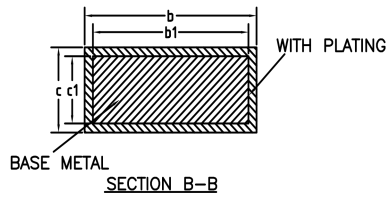
GND pad (2) connect to second layer ground path by via to increase cooling area directly.

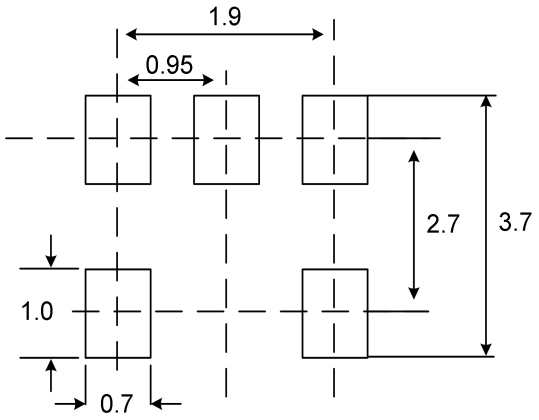
Package Outline Dimension-SOT23-5

SOT23-5 Unit (mm)







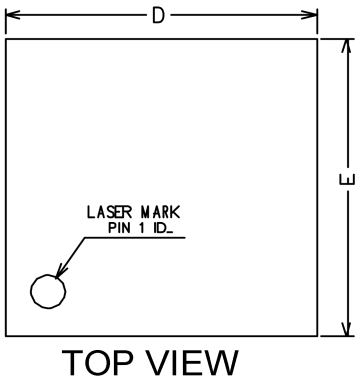


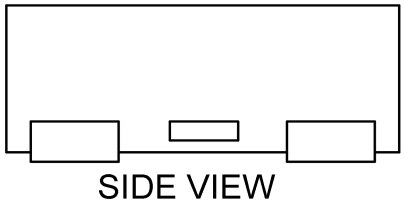
RECOMMENDED LAND PATTERN

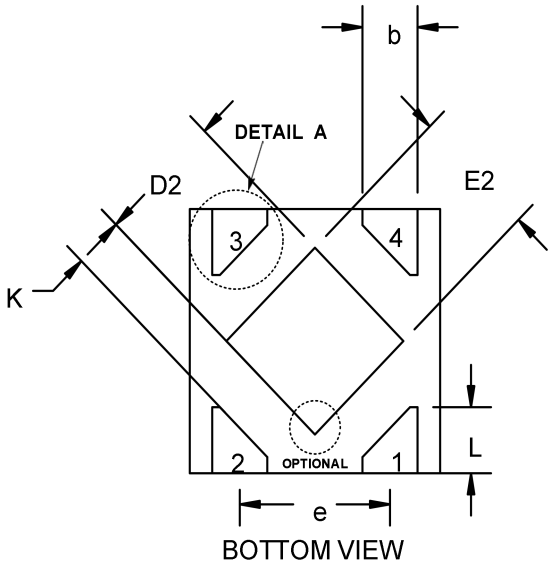
Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Typ**	**Max**
A	-	-	1.25
A1	0	-	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	-	0.45
b1	0.35	0.38	0.41
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e 1	1.80	1.90	2.00
K	0	-	0.25
L	0.30	0.40	0.60
L1		0.59 REF	
L2		0.25 BSC	
M	0.10	0.15	0.25
R	0.05	-	0.20
R1	0.05	-	0.20
θ	0°	-	8°
θ1	8°	10°	12°
θ2	10°	12°	14°

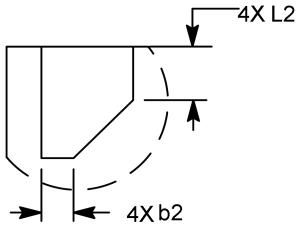
Package Outline Dimension-DFN1x1-4

DFN1x1-4 Unit (mm)



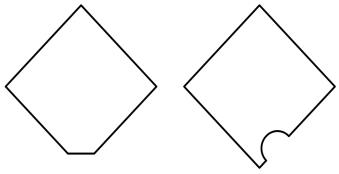


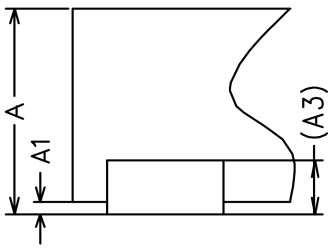


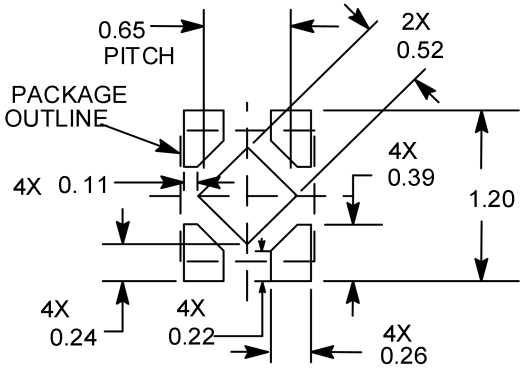


DETAIL A

Two options:







RECOMMENDED LAND PATTERN (Unit: mm)

Package Outline Dimension-DFN1x1-4

DFN1x1-4 Unit (mm)

Common Dimensions (Units of measure = Millimeter)			
Symbol	**Min**	**Nom**	**Max**
A	0.34	0.37	0.40
A1	0	0.02	0.05
A3		0.10 REF	
b	0.17	0.22	0.27
D	0.95	1.00	1.05
E	0.95	1.00	1.05
D2	0.43	0.48	0.53
E2	0.43	0.48	0.53
L	0.20	0.25	0.30
e	0.60	0.65	0.70
K	0.15	-	-
L2	0.07	0.12	0.17
b2	0.02	-	0.12

Version History

Version	Date	Changes
Rev.1.0	2025-12-10	Initial release

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