# PJ74AUP1G08 Datasheet

## Low-Power Single 2-Input Positive-AND Gate

**Version：Rev.1.0**

Release Date：2025-10-28

MetaWells Co., Ltd.

www.MetaWells.com

## General Description

This single 2-input positive-AND gate is designed for 0.8-V to 3.6-V $V_{CC}$ operation.

The PJ74AUP1G08 device performs the Boolean function Y=A x B in positive logic.

The CMOS device has high output drive while maintaining low static power dissipation over a broad $V_{CC}$ operating range.

The PJ74AUP1G08 is available in a variety of packages, including SOT23-5, SC70-5.

## Simplified Schematic


## Features

- Inputs Accept Voltages 0.8V to 3.6 V
- Max $T_{PD}$ of 4.8 ns at 3.3 V
- Low Static-Consumption, 0.9-μA Max $I_{CC}$
- Low Noise Overshoot and Undershoot<10% of $V_{CC}$
- $I_{off}$ Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Input Hysteresis Allows Slow Input Transition and Better Switching Noise Immunity at Input($V_{hys}$= 250mV Typical 3.3V)
- 3.6V I/O Tolerant to Support Mixed-Mode Signal Operation
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

## Applications

- ATCA Solutions
- Active Noise Cancellation (ANC)
- Barcode Scanner
- Blood Pressure Monitor
- CPAP Machine
- Cable Solutions
- DLP 3D Machine Vision, Hyperspectral Imaging, Optical Networking, and Spectroscopy
- E-Book
- Embedded PC
- Field Transmitter: Temperature or Pressure Sensor
- Fingerprint Biometrics
- HVAC: Heating, Ventilating, and Air Conditioning

# Ordering Information

## Ordering Information

| Order number | Marking ID | Package | MSL | Description |
|---|---|---|---|---|
| PJ74AUP1G08S5 | C4DNN | SOT23-5 | Level-3 | Halogen free RoHS compliant in T/R, 3,000 pcs/Reel |
| PJ74AUP1G08C5 | APW | SC70-5 | Level-3 | Halogen free RoHS compliant in T/R, 3,000 pcs/Reel |

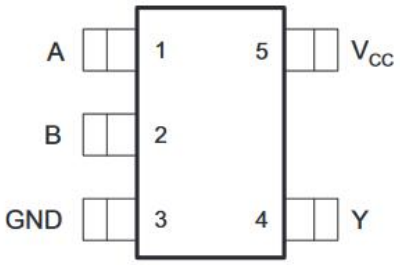
Note:

(1) MetaWells can meet RoHS 2.0/REACH requirement. So most package types MetaWells offers only states halogen free, instead of lead free.

## Marking Information

| Marking | Package | Definition |
|---|---|---|
| C4DNN | SOT23-5 | C4: Product code ; D: Date code ; NN: Serial number |
| APW | SC70-5 | AP: Product code ; W: Week code |

## Pin Configuration




**SOT23-5 and SC70-5 (Top View)**

## Pin Description

| Pin | | Function |
|---|---|---|
| Num | Name | |
| 1 | A | Input |
| 2 | B | Input |
| 3 | GND | Ground |
| 4 | Y | Output |
| 5 | $V_{CC}$ | Power Pin |

## Function Table

*H = HIGH voltage level; L = LOW voltage level; X = do not care*

| INPUTs | | OUTPUT |
|---|---|---|
| A | B | Y |
| H | H | H |
| L | X | L |
| X | L | L |

## Absolute Maximum Ratings

| Symbol | Value | Units |
|---|---|---|
| $V_{CC}$ | -0.5 to 4.6 | V |
| $V_I$ | -0.5 to 4.6 | V |
| $V_O$(Voltage range applied to any output in the high-impedance or power-off state) | -0.3 to 4.6 | V |
| $V_O$(Voltage range applied to any output in the high or slow state) | -0.3 to $V_{CC}$+0.3 | V |
| Input clamp current | -50 | mA |
| Output clamp current | -50 | mA |
| Continuous output current | ±20 | mA |
| Storage Temperature | -65 to 150 | °C |

## Recommended Operating Conditions

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | Operating | 0.8 | | 3.6 | V |
| Input voltage | $V_I$ | | 0 | | 3.6 | V |
| Output voltage | $V_O$ | | 0 | | $V_{CC}$ | V |
| High- level input voltage | $V_{IH}$ | $V_{CC}$ = 0.8V | $V_{CC}$ | | | V |
| | | $V_{CC}$ = 1.1V to 1.95V | 0.65 x$V_{CC}$ | | | |
| | | $V_{CC}$ = 2.3V to 2.7V | 1.6 | | | |
| | | $V_{CC}$ = 3V to 3.6V | 2 | | | |
| Low- level input voltage | $V_{IL}$ | $V_{CC}$ = 0.8V | | | 0 | V |
| | | $V_{CC}$ = 1.1V to 1.95V | | | 0.35 x $V_{CC}$ | |
| | | $V_{CC}$ = 2.3V to 2.7V | | | 0.7 | |
| | | $V_{CC}$ = 3V to 3.6V | | | 0.9 | |
| High- level output current | $I_{OH}$ | $V_{CC}$ = 0.8V | | | -20 | μA |
| | | $V_{CC}$ = 1.1V | | | -1.1 | mA |
| | | $V_{CC}$ = 1.4V | | | -1.7 | |
| | | $V_{CC}$ = 1.65V | | | -1.9 | |
| | | $V_{CC}$ = 2.3V | | | -3.1 | |
| | | $V_{CC}$ = 3V | | | -4 | |
| Low- level output current | $I_{OL}$ | $V_{CC}$ = 0.8V | | | 20 | μA |
| | | $V_{CC}$ = 1.1V | | | 1.1 | mA |
| | | $V_{CC}$ = 1.4V | | | 1.7 | |
| | | $V_{CC}$ = 1.65V | | | 1.9 | |
| | | $V_{CC}$ = 2.3V | | | 3.1 | |
| | | $V_{CC}$ = 3V | | | 4 | |
| Input transition rise or fall rate | △T/△V | $V_{CC}$ = 0.8V to 3.6V | | | 200 | ns/V |
| Operating temperature | $T_A$ | | -40 | | 85 | °C |

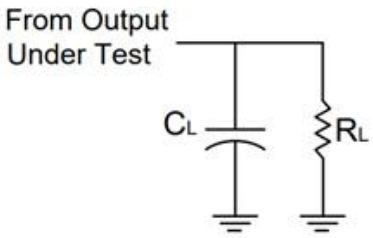
## Electrical Characteristics

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| High- level output voltage | $V_{OH}$ | $V_{CC}$ = 0.8~3.6V, $I_{OH}$= -20uA | $V_{CC}$-0.1 | | | V |
| | | $V_{CC}$ = 1.1V, $I_{OH}$= -1.1mA | 0.75 x$V_{CC}$ | | | |
| | | $V_{CC}$ = 1.4V, $I_{OH}$= -1.7mA | 1.11 | | | |
| | | $V_{CC}$ = 1.65V, $I_{OH}$= -1.9mA | 1.32 | | | |
| | | $V_{CC}$ = 2.3V, $I_{OH}$= -2.3mA | 2.05 | | | |
| | | $V_{CC}$ = 2.3V, $I_{OH}$= -3.1mA | 1.9 | | | |
| | | $V_{CC}$ = 3V, $I_{OH}$= -2.7mA | 2.72 | | | |
| | | $V_{CC}$ = 3V, $I_{OH}$= -4mA | 2.6 | | | |
| Low- level output voltage | $V_{OL}$ | $V_{CC}$ = 0.8~3.6V, $I_{OL}$= 20uA | | | 0.1 | V |
| | | $V_{CC}$ = 1.1V, $I_{OL}$= 1.1mA | | | 0.3 x$V_{CC}$ | |
| | | $V_{CC}$ = 1.4V, $I_{OL}$= 1.7mA | | | 0.31 | |
| | | $V_{CC}$ = 1.65V, $I_{OL}$= 1.9mA | | | 0.31 | |
| | | $V_{CC}$ = 2.3V, $I_{OL}$= 2.3mA | | | 0.31 | |
| | | $V_{CC}$ = 2.3V, $I_{OL}$= 3.1mA | | | 0.44 | |
| | | $V_{CC}$ = 3V, $I_{OL}$= 2.7mA | | | 0.31 | |
| | | $V_{CC}$ = 3V, $I_{OL}$= 4mA | | | 0.44 | |
| Input leakage current | $I_L$ | $V_{IN}$= 3.6V or GND, $V_{CC}$= 0~3.6V | | | 0.1 | μA |
| Power off leakage current | $I_{OFF}$ | $V_I$ or $V_O$=0V to 3.6V, $V_{CC}$=0V | | | 0.2 | μA |
| Supply current | $I_{CC}$ | $V_I$= GND or ($V_{CC}$ to 3.6V), $I_{OUT}$=0, $V_{CC}$=0.8~3.6V | | | 0.5 | μA |
| Additional supply current per input pin | $\triangle I_{CC}$ | $V_I$= $V_{CC}$-0.6V, $I_{OUT}$=0 | | | 40 | mA |

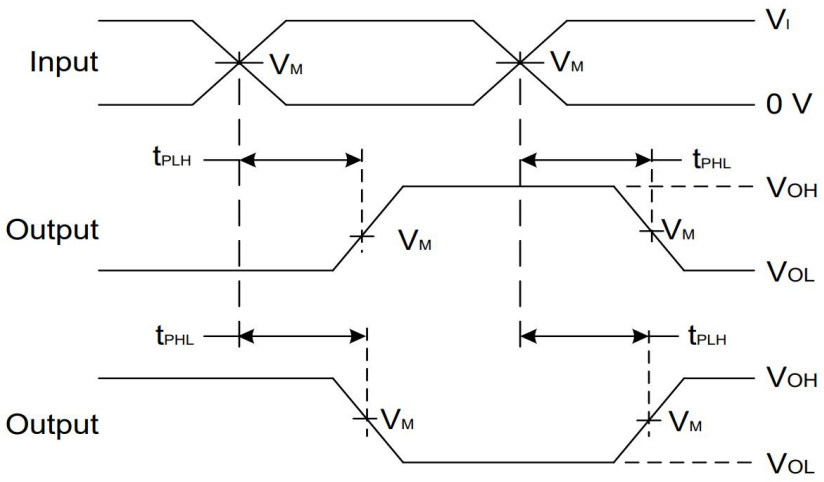
## Switching Characteristics

| Parameter | Symbol | Test Conditions | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| Propagation delay from input (A or B) to output (Y) | $T_{PD}$ | $V_{CC}$ = 0.8V | $C_L$ = 15 pF<br>$R_L$ = 1 MΩ | | 24 | | nS |
| | | $V_{CC}$ = 1.2V±0.1V, | | 3.6 | 9.9 | 16.3 | nS |
| | | $V_{CC}$ = 1.5V±0.1V, | | 2.3 | 7.2 | 11.1 | nS |
| | | $V_{CC}$ = 1.8V±0.15V | | 1.6 | 5.8 | 8.7 | nS |
| | | $V_{CC}$ = 2.5V±0.2V | | 1 | 4.3 | 5.9 | nS |
| | | $V_{CC}$ = 3.3V±0.3V | | 1 | 3.4 | 4.8 | nS |

# Parameter Measurement Information




| $V_{CC}$ | INPUTS | | $V_M$ | $C_L$ | $R_L$ |
|---|---|---|---|---|---|
| | $V_I$ | $t_r/t_f$ | | | |
| 0.8V | $V_{CC}$ | ≦2 ns | $V_{CC}/2$ | 15 pF | 1 MΩ |
| 1.2V ± 0.1V | $V_{CC}$ | ≦2 ns | $V_{CC}/2$ | 15 pF | 1 MΩ |
| 1.5V ± 0.1V | $V_{CC}$ | ≦2 ns | $V_{CC}/2$ | 15 pF | 1 MΩ |
| 1.8V ± 0.15V | $V_{CC}$ | ≦2 ns | $V_{CC}/2$ | 15 pF | 1 MΩ |
| 2.5V ± 0.2V | 3 V | ≦2.5 ns | 1.5 V | 15 pF | 1 MΩ |
| 3.3V ± 0.3V | $V_{CC}$ | ≦2.5 ns | $V_{CC}/2$ | 15 pF | 1 MΩ |




**Voltage waveform propagation delay times, Inverting and non-inverting outputs**

Notes:

(1) $C_L$ includes probe and jig capacitance.

(2) All pulses and supplied at pulse repetition rate≦10MHz.

(3) The Inputs are measured separately one transition per measurement.

(4) $t_{PLH}$ and $t_{PHL}$ are the same as $t_{PD}$.

# IC Operation Information

## Basic Operation

The PJ74AUP1G08 device contains one 2-input positive AND gate device and performs the Boolean function Y=A x B or $Y = \overline{\overline{A} + \overline{B}}$. The AUP family of devices has quiescent power consumption less than 1 μA. This device is fully specified for partial-power-down applications using $I_{off}$. The $I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the device when it is powered. The $I_{off}$ feature also allows for live insertion.

## Function Block Diagram


## Feature Description

- Wide operating $V_{CC}$ range of 0.8V to 3.6V.
- 3.6-V I/O tolerant to support down translation.
- Input hysteresis allows slow input transition and better switching noise immunity at the input.
- $I_{off}$ feature allows voltages on the inputs and outputs when $V_{CC}$ is 0 V.
- Low noise due to slower edge rates.

## Device Functional Table

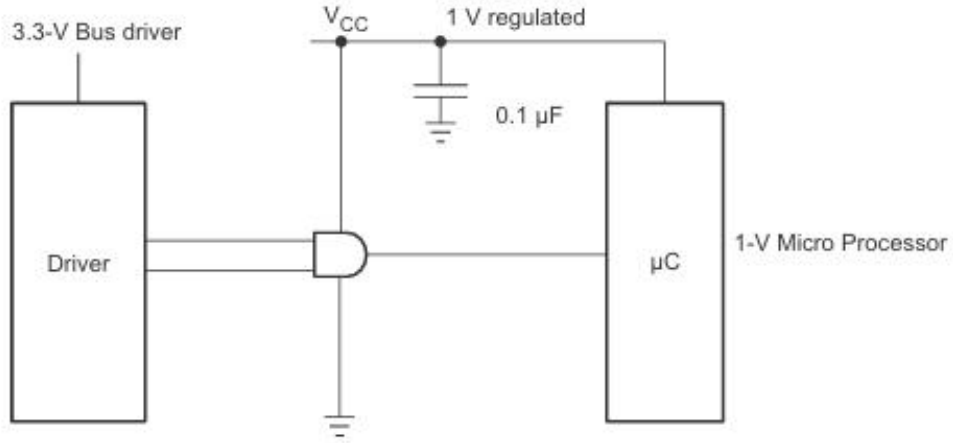
*H = HIGH voltage level; L = LOW voltage level; X = do not care*

| INPUTs | | OUTPUT |
|---|---|---|
| **A** | **B** | **Y** |
| H | H | H |
| L | X | L |
| X | L | L |

# IC Application Information

The AUP family is the solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static and dynamic power consumption across the entire $V_{CC}$ range of 0.8 V to 3.6 V, resulting in an increased battery life. This product also maintains excellent signal integrity. It has a small amount of hysteresis built in allowing for slower or noisy input signals. The lowered drive produces slower edges and prevents overshoot and undershoot on the outputs.

### Typical Application




### Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits

### Detailed Design Procedure

1. Recommended Input conditions:
   - – Rise time and fall time specs. See (Δt/ΔV)
   - – Specified high and low levels. See ($V_{IH}$ and $V_{IL}$)
   - – Inputs are overvoltage tolerant allowing them to go as high as 3.6 V at any valid $V_{CC}$
2. Recommended output conditions:
   - – Load currents should not exceed 20 mA on the output and 50 mA total for the part
   - – Outputs should not be pulled above $V_{CC}$

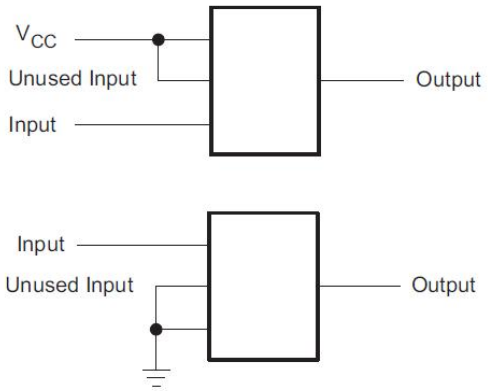
## Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the Recommended Operating Conditions table. Each $V_{CC}$ pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1 μF is recommended; if there are multiple $V_{CC}$ pins, then 0.01 μF or 0.022 μF is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1 μF and a 1 μF are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results

## Layout Considerations

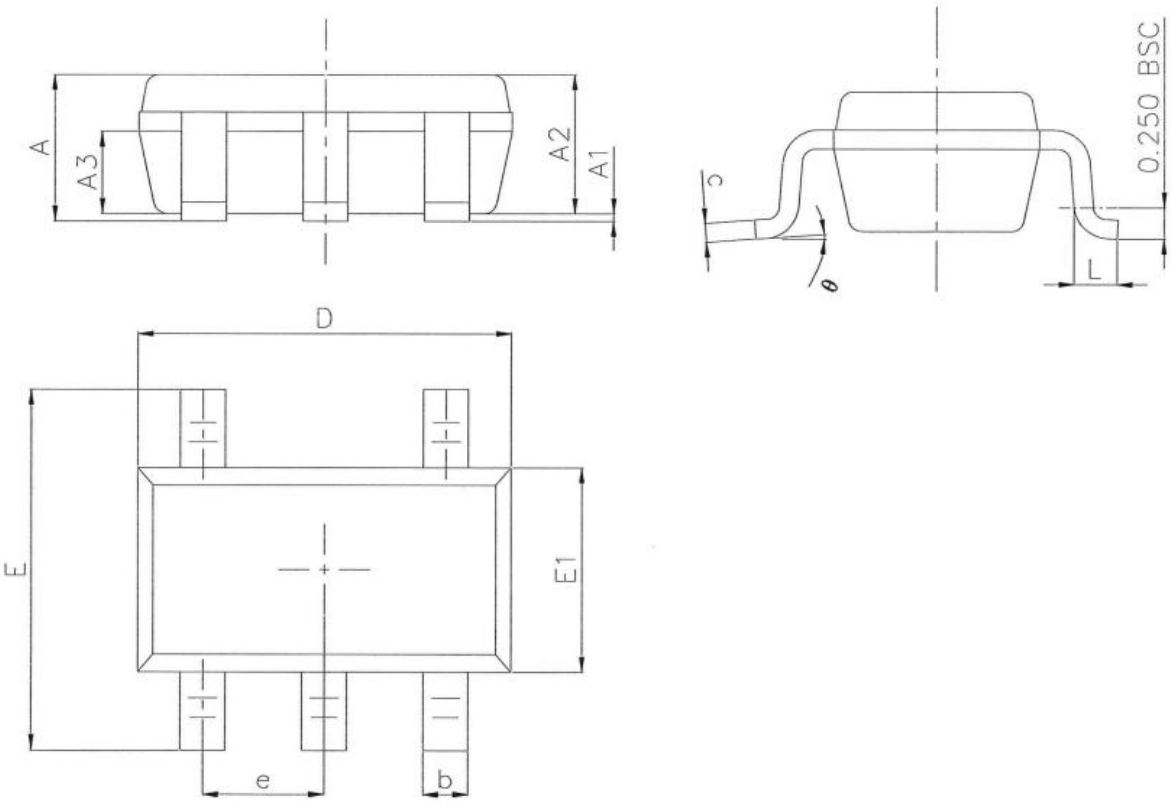
When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Below figure specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or $V_{CC}$, whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the I/Os, so they cannot float when disabled.



# Package Outline Dimension-SOT23-5

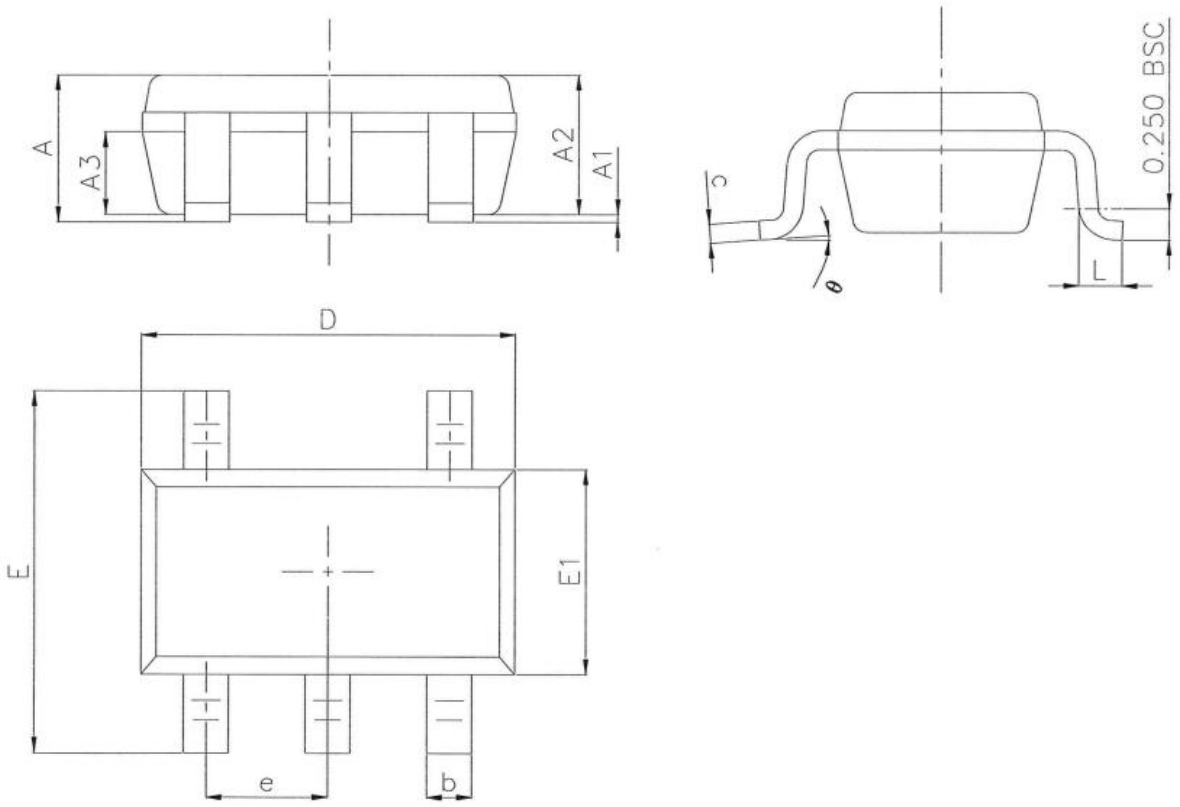
**SOT23-5 Unit (mm)**




| Symbol | Dimension in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 1.050 | 1.150 | 1.250 |
| A1 | 0.000 | 0.060 | 0.100 |
| A2 | 1.000 | 1.100 | 1.200 |
| A3 | 0.550 | 0.650 | 0.750 |
| D | 2.820 | 2.920 | 3.020 |
| E1 | 1.510 | 1.610 | 1.700 |
| E | 2.650 | 2.800 | 2.950 |
| b | 0.300 | 0.400 | 0.500 |
| e | 0.950BSC | | |
| θ | 0° | 4° | 8° |
| L | 0.300 | 0.420 | 0.570 |
| c | 0.100 | 0.152 | 0.200 |

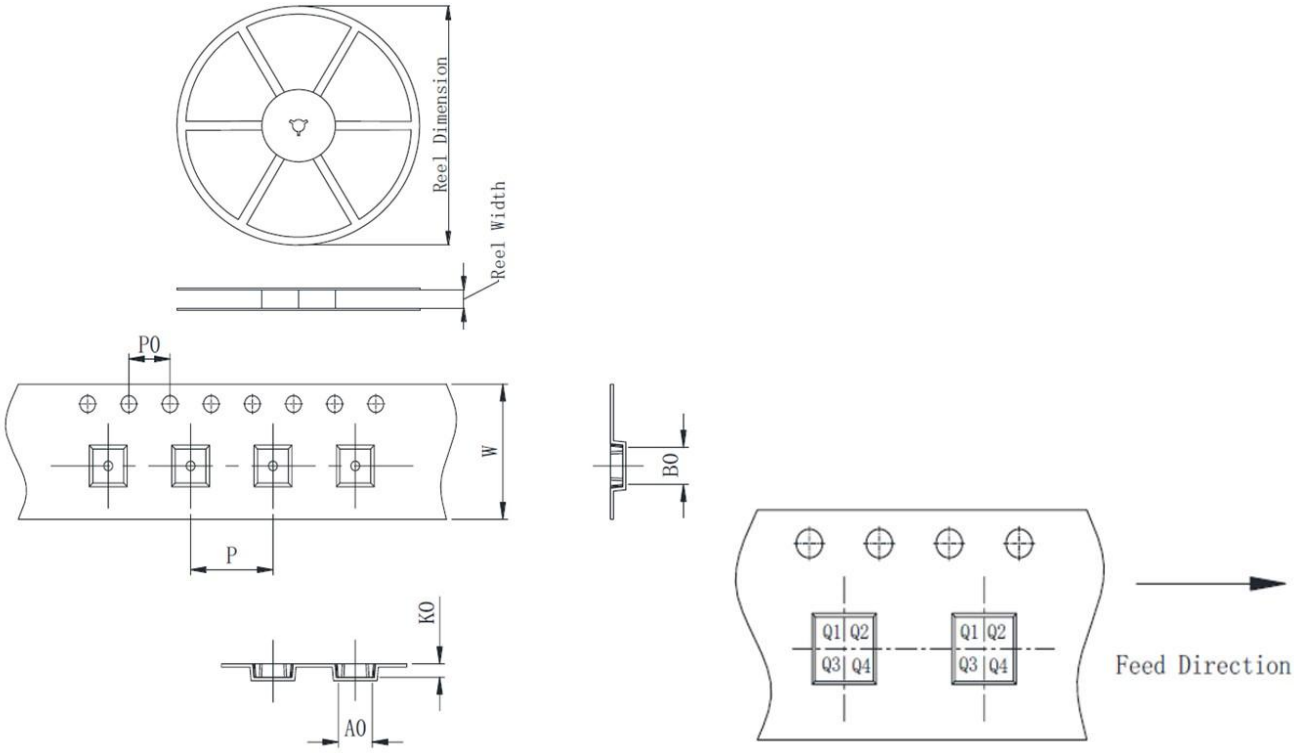
# Package Outline Dimension-SC70-5

**SC70-5 Unit (mm)**




| Symbol | Dimension in mm | | |
|---|---|---|---|
| | Min. | Nom. | Max. |
| A | 0.90 | 0.95 | 1.00 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | | 0.9 | |
| A3 | | 0.55 | |
| D | 2.00 | 2.10 | 2.20 |
| E1 | 1.15 | 1.25 | 1.35 |
| E | 2.00 | 2.10 | 2.20 |
| b | 0.15 | 0.225 | 0.30 |
| e | 0.65BSC | | |
| θ | 0° | 4° | 8° |
| L | 0.26 | 0.35 | 0.46 |
| c | 0.10 | 0.15 | 0.20 |

## Packing information




| Package type | Reel size | Reel dimension (±3.0mm) | Reel width (±1.0mm) | A0 (±0.1mm) | B0 (±0.1mm) | K0 (±0.1mm) | P (±0.1mm) | P0 (±0.1mm) | W (±0.3mm) | Pin1 |
|---|---|---|---|---|---|---|---|---|---|---|
| SOT23-5 | 7' | 180 | 8.4 | 3.23 | 3.17 | 1.32 | 4.0 | 4.0 | 8.0 | Q3 |
| SC70-5 | 7' | 180 | 8.4 | 3.23 | 3.17 | 1.32 | 4.0 | 4.0 | 8.0 | Q3 |

# Version History

| Version | Date | Changes |
|---|---|---|
| Rev.1.0 | 2025-10-28 | Initial release |

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