PJ74LVC1G06 Datasheet

Single Inverter Buffer/Driver With Open-Drain Output

Version：Rev.1.0

Release Date：2025-12-01

MetaWells Co., Ltd.

www.MetaWells.com

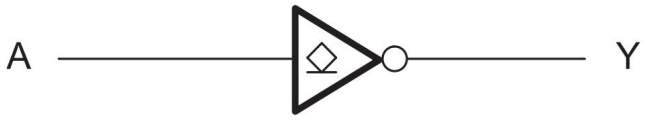
General Description

This single inverter buffer and driver is designed for 1.65-V to5.5-V V_{CC} operation.

The output of the PJ74LVC1G06 device is open-drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32mA.

This device is fully specified for partial- power-down applications using I_{OFF} circuitry disables the outputs when the device is powered down. This inhibits current backflow into the device which prevents damage to the device.

Simplified Schematic



Features

- Supports 5-V V_{CC} Operation
- Input and Open-Drain Output Accept Voltage up to 5.5V
- Max Tpd of 4.5 ns at 3.3 V
- Low Power Consumption, 10-μA Max I_{CC}
- ±24-mA Output Drive at 3.3 V for open-drain devices
- I_{OFF} Supports Partial-Power-Down Mode and Back-Drive
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- Can Be Used For Up or Down Translation
- Schmitt Trigger Action on All Ports
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

Applications

- AV Receiver
- Blu-ray Player and Home Theater
- DVD Recorders and Players
- Desktop or Notebook PCs
- Digital Radio or Internet Radio Players
- Digital Video Cameras (DVC)
- Embedded PC
- GPS: Personal Navigation Devices
- Mobile Internet Devices
- Network Projector Front-Ends
- Portable Media Players
- Pro Audio Mixers
- Smoke Detectors
- Solid State Drive (SSD): Enterprise
- High-Definition (HDTV)
- Tablet: Enterprise
- Audio Dock: Portable
- DLP Front Projection Systems
- DVR and DVS
- Digital Picture Frame (DPF)
- Digital Still Cameras

Ordering Information

Order number	Marking ID	Package	MSL	Description
PJ74LVC1G06S5	C3DNN	SOT23-5	Level-3	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel
PJ74LVC1G06C5	ANW	SC70-5	Level-3	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel

Note:

(1) MetaWells can meet RoHS 2.0/REACH requirement. So most package types MetaWells offers only states halogen free, instead of lead free.

Marking Information

Marking ID	Package	Definition
C3DNN	SOT23-5	C3: Product code D: Date code NN: Serial number
ANW	SC70-5	AN: Product code W: Week code

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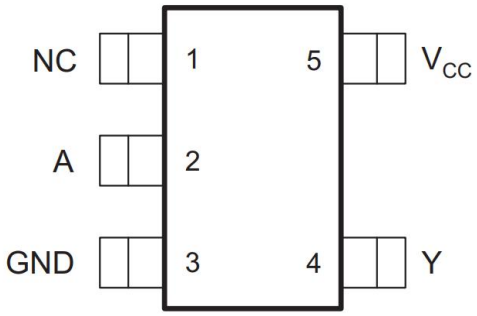
Pin Configuration



SOT23-5 and SC70-5 (Top View)

Functional Pin Description

Pin		Description
Name	**Num**	
NC	1	No connect
A	2	Input
GND	3	Ground
Y	4	Output
V_{CC}	5	Power pin

Function Table

H = HIGH voltage level; L = LOW voltage level; Hi-Z = High impedance

INPUTs	OUTPUT
A	**Y**
L	Hi-Z
H	L

Absolute Maximum Ratings

Parameter	Value	Units
V_{CC}	-0.5 to 6.5	V
V_I	-0.5 to 6.5	V
V_O(Voltage applied to any output in the high-impedance or power-off state)	-0.5 to 6.5	V
V_O(Voltage applied to any output in the high or slow state)	-0.5 to 6.5	V
Input clamp current	-50	mA
Output clamp current	-50	mA
Continuous output current	±50	mA
Storage temperature	-65 to 150	°C

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			
Input voltage	V_I		0		5.5	V
Output voltage	V_O				5.5	V
High- level input voltage	V_{IH}	V_{CC} = 1.65V to 1.95V	0.65 x V_{CC}			V
		V_{CC} = 2.3V to 2.7V	1.7			
		V_{CC} = 3V to 3.6V	2			
		V_{CC} = 4.5V to 5.5V	0.7 x V_{CC}			
Low- level input voltage	V_{IL}	V_{CC} = 1.65V to 1.95V			0.35 x V_{CC}	V
		V_{CC} = 2.3V to 2.7V			0.7	
		V_{CC} = 3V to 3.6V			0.8	
		V_{CC} = 4.5V to 5.5V			0.3 x V_{CC}	
Low- level output current	I_{OL}	V_{CC} = 1.65V			4	mA
		V_{CC} = 2.3V			8	
		V_{CC} = 3V			16	
		V_{CC} = 3V			24	
		V_{CC} = 4.5V			32	
Input transition rise or fall rate	△T/△V	V_{CC} = 1.8V±0.15V,2.5V±0.2V			20	ns/V
		V_{CC} = 3.3V±0.3V			10	
		V_{CC} = 5V±0.5V			5	
Operating temperature	T_A		-40		125	°C

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Low- level output voltage	V_{OL}	V_{CC} = 1.65~5.5V, I_{OL}= 100μA			0.1	V
		V_{CC} = 1.65V, I_{OL}= 4mA			0.45	
		V_{CC} = 2.3V, I_{OL}= 8mA			0.3	
		V_{CC} = 3V, I_{OL}= 16mA			0.4	
		V_{CC} = 3V, I_{OL}= 24mA			0.55	
		V_{CC} = 4.5V, I_{OL}= 32mA			0.55	
Inflection-point current	I_I	V_{IN}= 5.5V or GND, V_{CC}= 0~5.5V			±1	μA
Power off leakage current	I_{OFF}	V_I or V_O = 5.5V, V_{CC}=0V			±10	μA
Supply current	I_{CC}	V_I= 5.5V or GND, I_{OUT}=0, V_{CC}=1.65~5.5V			10	μA
Additional supply current per input pin	$\triangle I_{CC}$	V_{CC}=3~5.5V, one input at V_{CC}-0.6V, other input at V_{CC} or GND			500	μA

Switching Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation delay from input(A) to output(Y)	T_{PD}	V_{CC} = 1.8V±0.15V,	2.2		7	nS
		V_{CC} = 2.5V±0.2V	1.1		4.5	nS
		V_{CC} = 3.3V±0.3V	1.2		4.5	nS
		V_{CC} = 5V±0.5V	1		3.5	nS

Typical Characteristics

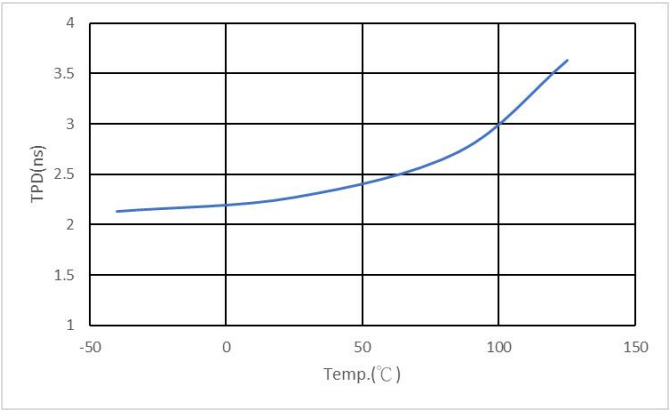


Figure 1. TPD across Temperature at 3.3V V_{CC}

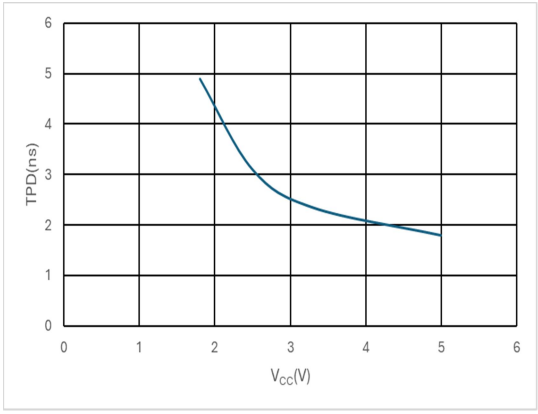
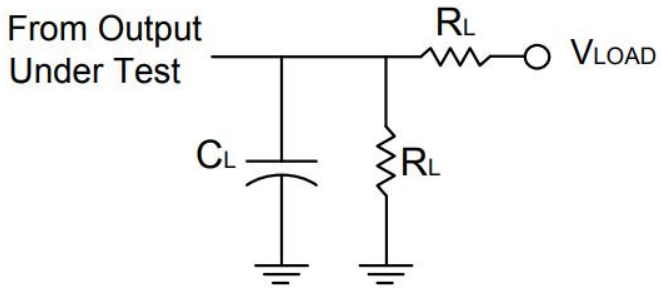


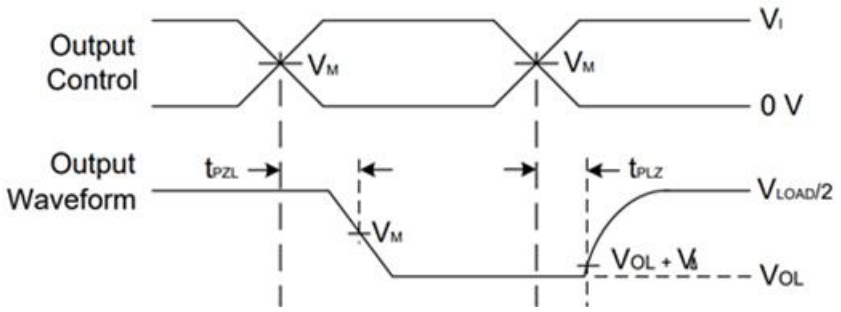
Figure 2. TPD across V_{CC} at 25℃

Parameter Measurement Information



Test	Condition
t_{PLZ}	V_{LOAD}
t_{PZL}	V_{LOAD}

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	$V_\triangle$
	V_I	t_r/t_f					
1.8V ± 0.15V	V_{CC}	≦2ns	$V_{CC}/2$	2 X V_{CC}	30pF	1kΩ	0.15V
2.5V ± 0.2V	V_{CC}	≦2ns	$V_{CC}/2$	2 X V_{CC}	30pF	500Ω	0.15V
3.3V ± 0.3V	3V	≦2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V ± 0.5V	V_{CC}	≦2.5ns	$V_{CC}/2$	2 X V_{CC}	50pF	500Ω	0.3V



Voltage Waveform Enable and DisableTimes

Low- and High-Level Enabling

Notes:

(1) C_L includes probe and jig capacitance.

(2) All pulses and supplied at pulse repetition rate≦10MHz.

(3) The Inputs are measured one at a time with one transition per measurement.

(4) For the open drain device t_{PLZ} and t_{PZL} are the same as t_{PD}.

(5) t_{PZL} is measured at V_M.

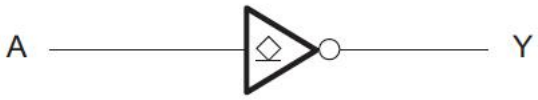
(6) t_{PLZ} is measured at V_{OL} + $V_\triangle$.

IC Operation Information

Basic Operation

The PJ74LVC1G06 device contains one open-drain inverter with a maximum sink current 32mA. This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The DFN1X1 package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

Function Block Diagram



Feature Description

• Wide operating voltage range.

– Operates from 1.65 V to 5.5 V.

• Allows down voltage translation.

• Inputs accept voltages to 5.5 V.

• Ioff feature allows voltages on the inputs and outputs when V_{CC} is 0 V.

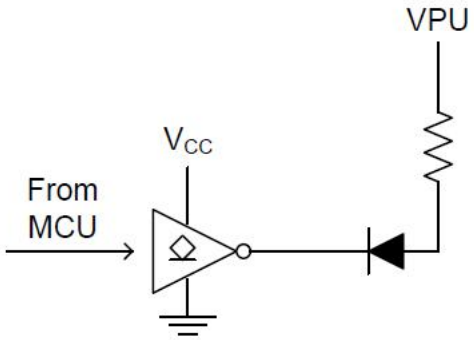
Device Functional Table

INPUTs	OUTPUT
A	**Y**
L	Hi-Z
H	L

IC Application Information

The PJ74LVC1G06 is a high drive CMOS device that can be used to implement a high output drive buffer, such as an LED application. It can produce 32 mA of drive current at 4.5 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to V_{CC}.

Typical Application



Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

Detailed Design Procedure

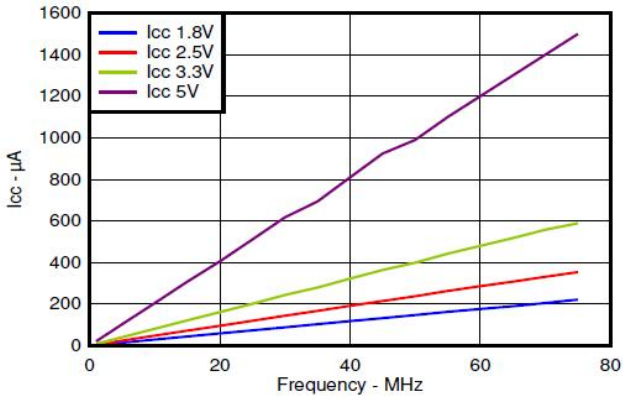
1. Recommended Input Conditions

- Rise time and fall time specs. See (Δt/ΔV) in the Recommended Operating Conditions table.
- Specified high and low levels. See (V_{IH} and V_{IL}) in the Recommended Operating Conditions table.
- Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the Recommended Operating Conditions table at any valid V_{CC}.

2. Recommend Output Conditions

- Load currents should not exceed (I_O max) per output and should not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the Absolute Maximum Ratings table.
- Outputs should not be pulled above V_{CC}.

Application Curves



Icc vs Frequency

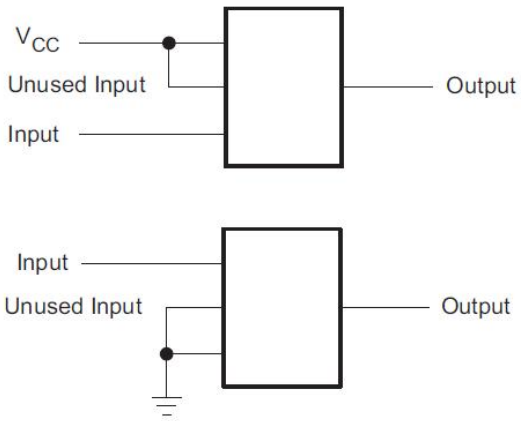
Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF capacitor is recommended and if there are multiple V_{CC} pins then 0.01-μF or 0.022-μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-μF and 1-μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

Layout Considerations

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input buffer gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.



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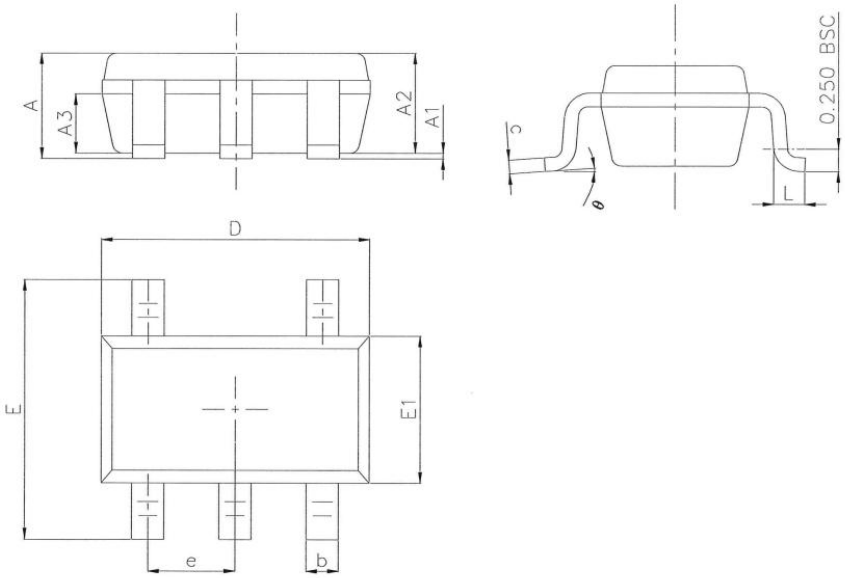
Package Outline Dimension-SOT23-5

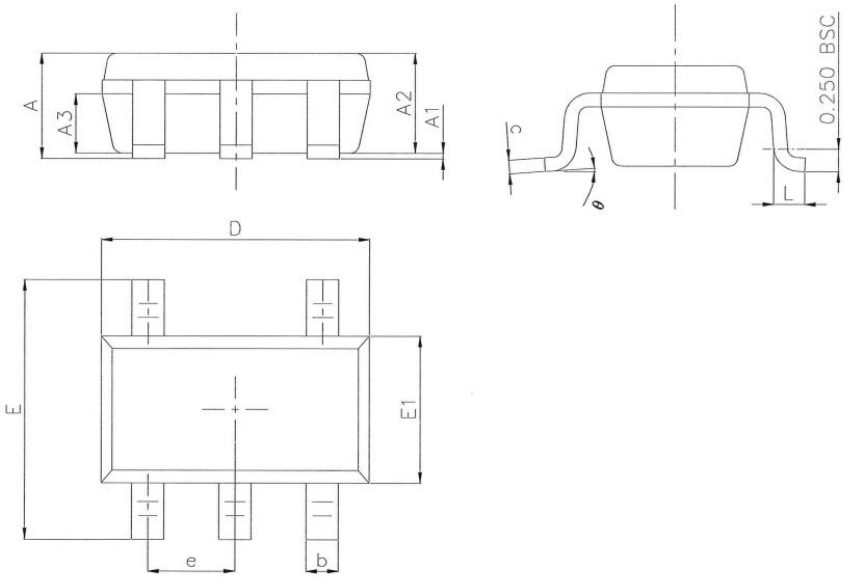
SOT23-5 Unit (mm)



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	1.050	1.150	1.250
A1	0.000	0.060	0.100
A2	1.000	1.100	1.200
A3	0.550	0.650	0.750
D	2.820	2.920	3.020
E1	1.510	1.610	1.700
E	2.650	2.800	2.950
b	0.300	0.400	0.500
e	0.950BSC		
θ	0°	4°	8°
L	0.300	0.420	0.570
c	0.100	0.152	0.200

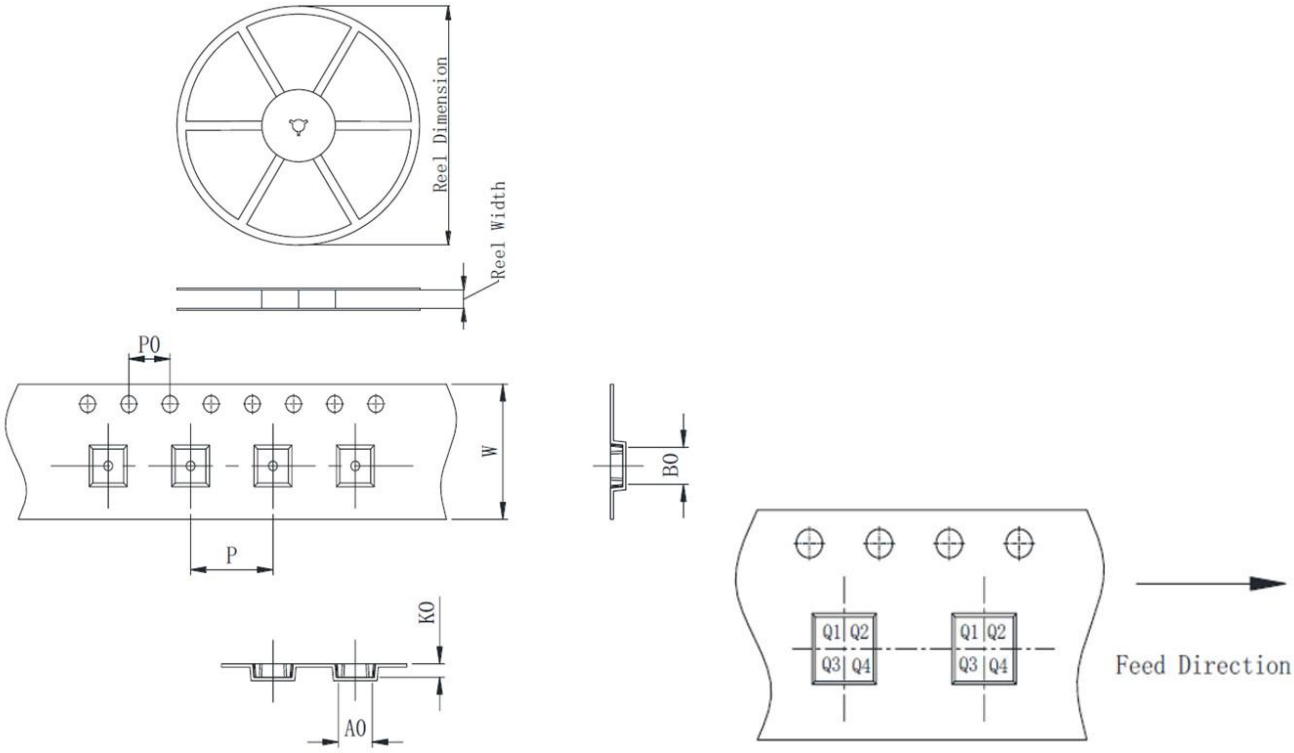
Package Outline Dimension-SC70-5

SC70-5 Unit (mm)



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	0.90	0.95	1.00
A1	0.00	0.05	0.10
A2		0.9	
A3		0.55	
D	2.00	2.10	2.20
E1	1.15	1.25	1.35
E	2.00	2.10	2.20
b	0.15	0.225	0.30
e	0.65BSC		
θ	0°	4°	8°
L	0.26	0.35	0.46
c	0.10	0.15	0.20

Packing information



Package type	Reel size	Reel dimension (±3.0mm)	Reel width (±1.0mm)	A0 (±0.1mm)	B0 (±0.1mm)	K0 (±0.1mm)	P (±0.1mm)	P0 (±0.1mm)	W (±0.3mm)	Pin1
SOT23-5	7'	180	8.4	3.23	3.17	1.32	4.0	4.0	8.0	Q3
SC70-5	7'	180	8.4	3.23	3.17	1.32	4.0	4.0	8.0	Q3

Version History

Version	Date	Changes
Rev.1.0	2025-12-01	Initial release

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