PJ85753 Datasheet

±1°C Remote and Local Temperature Sensor with SMBus, I^2C Interface In a SOT23-5 Package

Version：Rev.1.0

Release Date：2025-11-11

MetaWells Co., Ltd.
www.MetaWells.com

General Description

PJ85753 is a digital temperature sensor with ±1°C accuracy. Temperature data can be read out directly via digital interface (Compatible with SMBus, I²C) by MCU, Bluetooth chip or SoC chip. PJ85753 supports I²C communication with speed up to 3.4 MHz.

Each chip is specially calibrated for ±1°C (Max.) accuracy over -20°C to 100°C range in factory before shipment to customers. There is no need for re-calibration anymore for ±1°C accuracy.

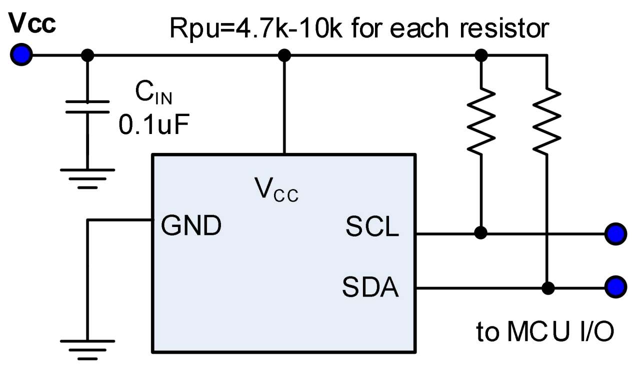
It includes a high precision band-gap circuit, a 12-bit Analog to Digital converter that can offer 0.0625°C resolution, a calibration unit with non-volatile memory and a digital interface block.

Available Package : SOT23-5.

Features

- Operation Voltage : 1.4 V to 5.5 V
- Average Quiescent Current : 3 μA (Typ.) at 1.0 con/s, 3.3 V
- Standby Current : 30 nA (Typ.)
- Temperature Accuracy without calibration :
  - Maximum : ±1°C from -20°C to 100°C
  - Maximum : ±2°C from -40°C to 125°C
- 12 bit ADC for 0.0625°C resolution
- Digital interface compatible with SMBus and I²C
- Programmable Over/Under Temperature
- 9 different slave addresses available with different suffix
- Temperature Range: -50°C to 125°C

Application Schematic



Applications

- Camera Module
- SSD Module
- Portable Devices

Ordering Information

Ordering Information

Order PN	Slave Address (R/W)	Accuracy	Green[1]	Package	Marking ID	Packing	MPQ	Operation Temperature
PJ85753AS5	0xE0	±1°C	Halogen free	SOT23-5	A3 D7NN	Tape & Reel	3,000	-50°C ~+125°C
PJ85753BS5	0xE2	±1°C	Halogen free	SOT23-5	AF DNN	Tape & Reel	3,000	-50°C ~+125°C
PJ85753CS5	0xE4	±1°C	Halogen free	SOT23-5	AG DNN	Tape & Reel	3,000	-50°C ~+125°C
PJ85753DS5	0xE6	±1°C	Halogen free	SOT23-5	AH DNN	Tape & Reel	3,000	-50°C ~+125°C
PJ85753ES5	0xE8	±1°C	Halogen free	SOT23-5	AJ DNN	Tape & Reel	3,000	-50°C ~+125°C
PJ85753FS5	0xEA	±1°C	Halogen free	SOT23-5	AK DNN	Tape & Reel	3,000	-50°C ~+125°C
PJ85753GS5	0xEC	±1°C	Halogen free	SOT23-5	AL DNN	Tape & Reel	3,000	-50°C ~+125°C
PJ85753HS5	0xEE	±1°C	Halogen free	SOT23-5	AM DNN	Tape & Reel	3,000	-50°C ~+125°C
PJ85753JS5	0x90	±1°C	Halogen free	SOT23-5	AN DNN	Tape & Reel	3,000	-50°C ~+125°C

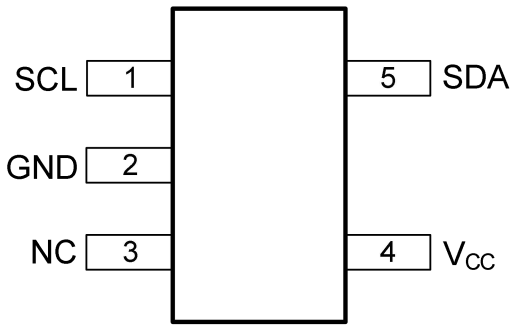
Note:

(1) MetaWells can meet RoHS 2.0/REACH requirement. So most package types MetaWells offers only states halogen free, instead of lead free.

Marking Information

Marking ID	Package	Definition
Ax DNN	SOT23-5	Ax: Product code D: Date code NN: Serial number

Pin Configuration

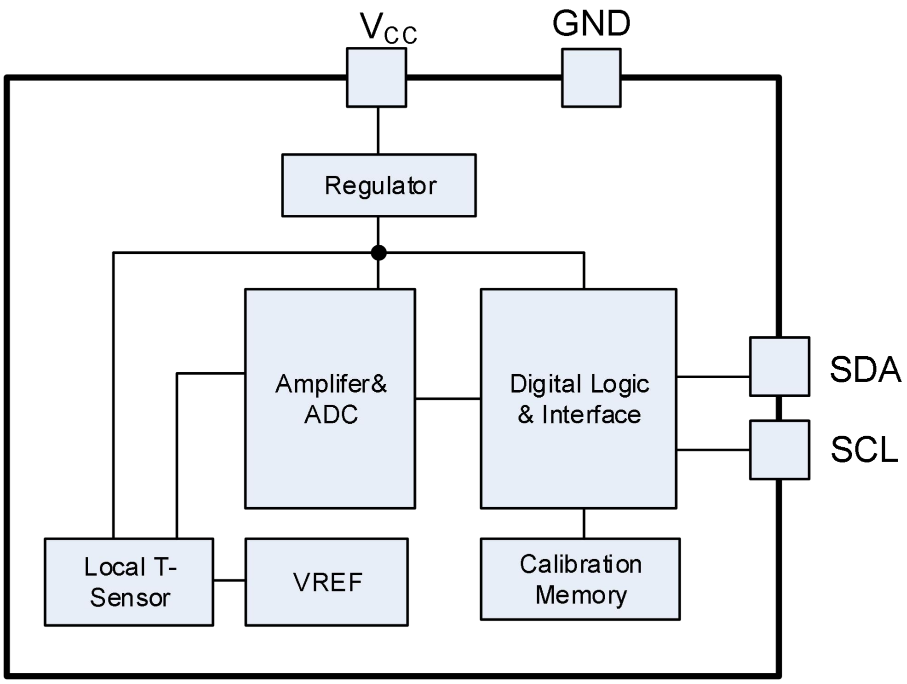


SOT23-5 (Top View)

Pin Description

Pin		Function
Num	Name	
1	SCL	Digital interface clock input pin, need a pull-up resistor to VCC.
2	GND	Ground pin.
3	NC	Not connected
4	VCC	Power supply input pin, using 0.1 μF low ESR ceramic capacitor to ground
5	SDA	Digital interface data input or output pin, need a pull-up resistor to VCC.

Function Block



PJ85753x Function Block

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

Parameter		Min	Max	Units
V_{CC} to GND	Supply Voltage	-0.3	7	V
V_{SDA}/V_{SCL} to GND	SDA, SCL Voltage	-0.3	7	V
T_{STG}	Storage temperature range	-65	150	°C
T_{LEAD}	Lead Temperature (Soldering, 10 Seconds)		260	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Handling Ratings

Parameter	Definition	Min	Max	Units
ESD(1)	Human Body Model (HBM) ESD stress voltage(2)	-2	2	kV
	Charged Device Model (CDM) ESD stress voltage(3), all pins	-1	1	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Units
V_{CC}	Supply Voltage	1.4	5.5	V
T_J	Operating junction temperature	-50	125	°C

Electrical Characteristics

Test Condition: C_{IN} = 0.1 µF, V_{CC} = 3.3 V, T_A = 25°C unless otherwise specified, all limits are 100% test at T_A = 25°C. (1)

Parameter		Test Conditions	Min	Typ	Max	Units
V_{CC}	Supply voltage range		1.4		5.5	V
T_{AC}	Temperature Accuracy	T_A = -20 to 110°C	-1.0		1.0	°C
		T_A = -40 to 125°C	-2.0		2.0	°C
$T_{RESOLUTION}$	Temperature Resolution			0.0625		°C
Temperature variation from V_{CC} Voltage		V_{CC} = 1.4 V to 5.5 V T_A = -40 to 125°C		0.1		°C/V
I_{AOC}	Average Operating Current	V_{CC} = 3.3 V, 1.0 con/s		3.0	4.5	µA
I_{SD}	Shutdown Current	Enable STB bit, force SDA/SCL to Vcc or GND		30	200	nA
T_{CON}	Conversion time (each channel)	From active to finish completely		7.2		mS
DIGITAL INTERFACE						
C_{IL}	Logic Input Capacitance	SDA, SCL pin		3.0		pF
V_{IH}	Logic Input High Voltage	SDA, SCL pin	0.7xV_{CC}		V_{CC}+0.3	V
V_{IL}	Logic Input Low Voltage	SDA, SCL pin	-0.3		0.3xV_{CC}	V
I_{INL}	Logic Input Current	SDA, SCL pin	-1.0		1.0	µA
I_{OLS}	Logic Output Sink Current	SDA, forced 0.2 V		5		mA
f_{CLK}	SCL frequency (2)	Fast Mode	1		400	KHz
		High Speed Mode	0.001		3.4	MHz
t_{LOW}	Clock low period time	Fast Mode	1300			nS
t_{HIGH}	Clock high period time	Fast Mode	600			nS
t_{BUF}	Bus free time	Between Stop and Start condition	1200			nS
$t_{HD:STA}$	Hold time after Start condition		600			nS
$t_{SU:STA}$	Repeated Start condition setup time		600			nS
$t_{SU:STO}$	Stop condition setup time		600			nS
$t_{HD:DAT}$	Data Hold time		100			nS
$t_{SU:DAT}$	Data Setup time		100			nS
t_F	Clock/Data fall time				300	nS
t_R	Clock/Data rise time				1000	nS
t_{TOUT}	Timeout of detecting clock low period time	SMBus Protocol		30		mS

(1) All devices are 100% production tested at T_A = +25°C; all specifications over the automotive temperature range is guaranteed by design, not production tested.

(2) For SCL, the minimal frequency is limited by SMBus timeout feature.

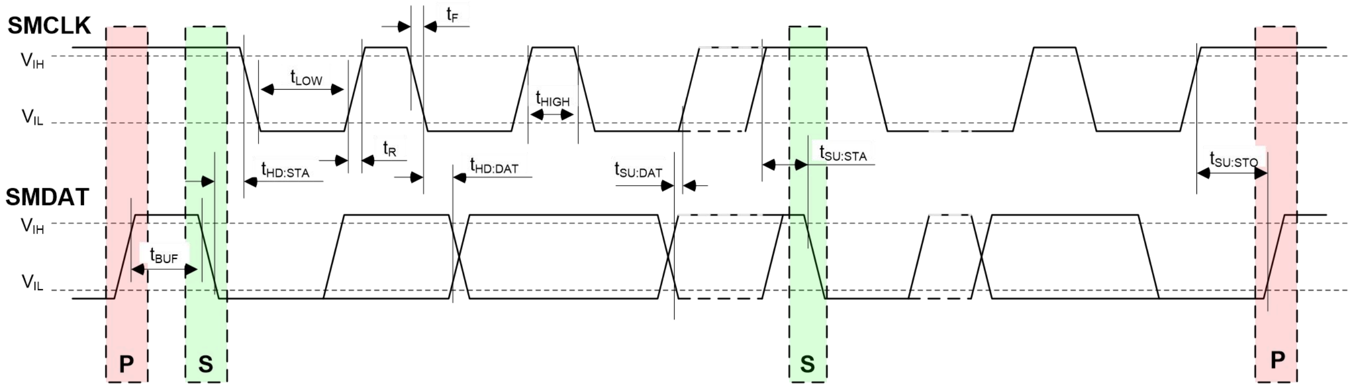


Figure-1. SMBus / I²C Timing Diagram

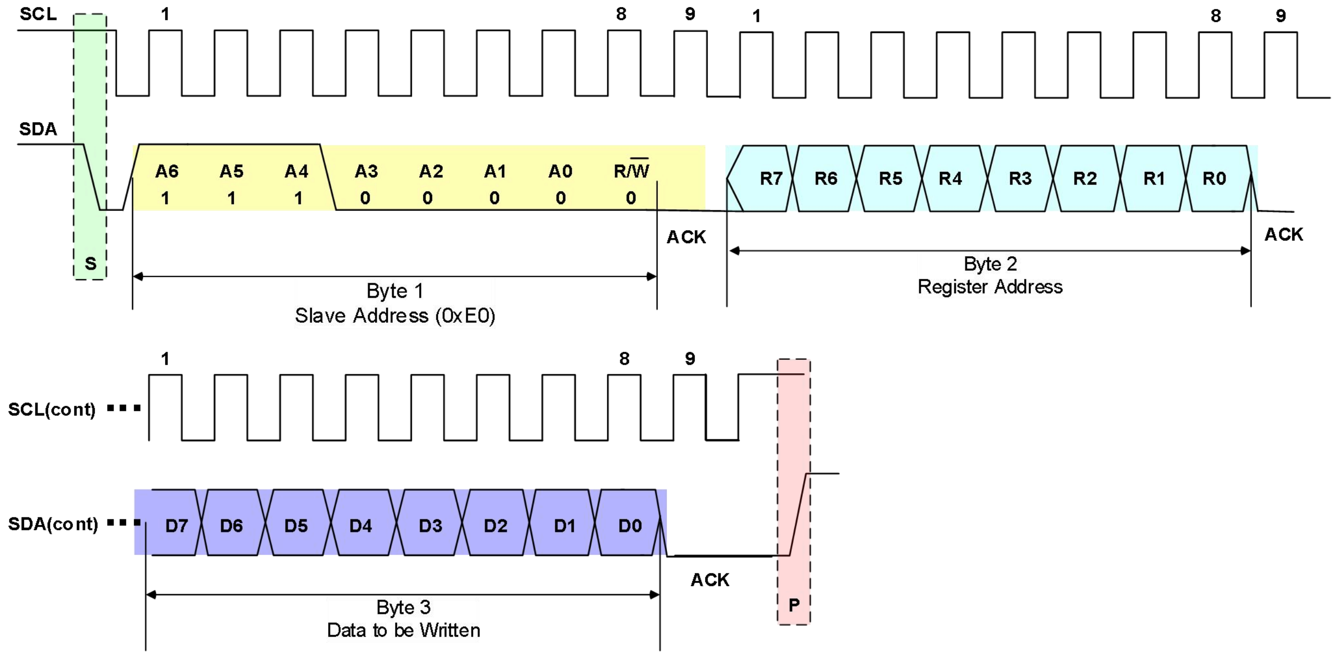


Figure-2. SMBus / I²C Write Byte Timing Diagram

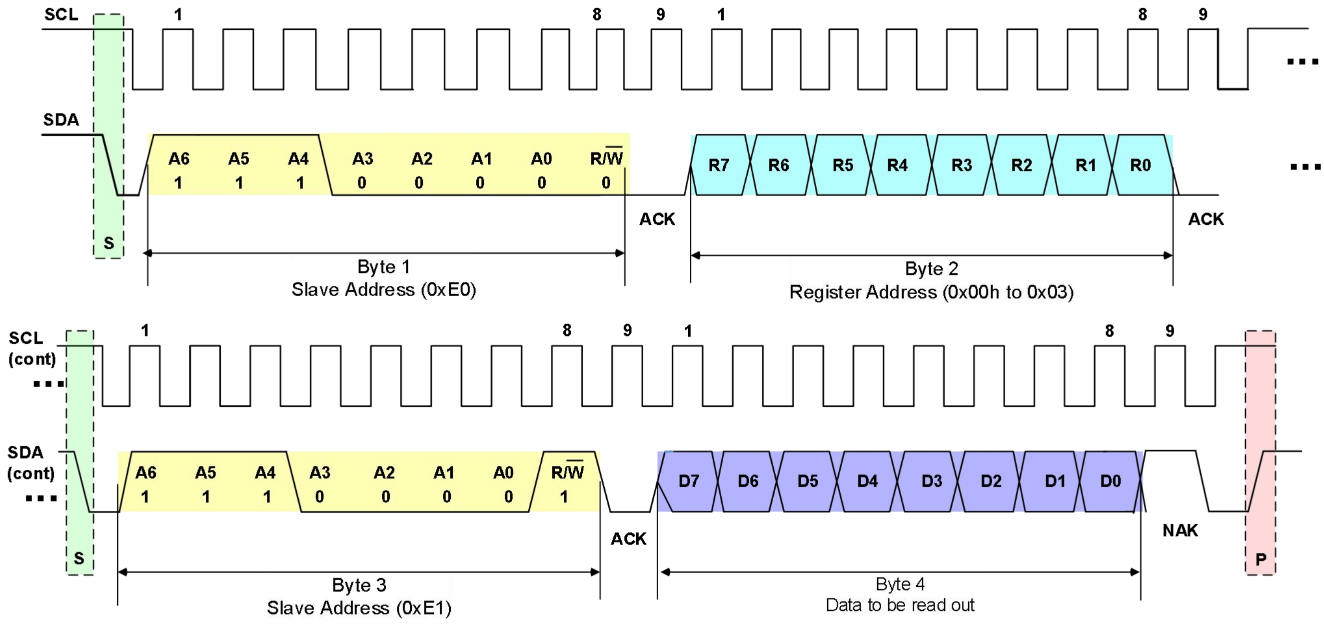


Figure-3. SMBus / I²C Read Byte Timing Diagram

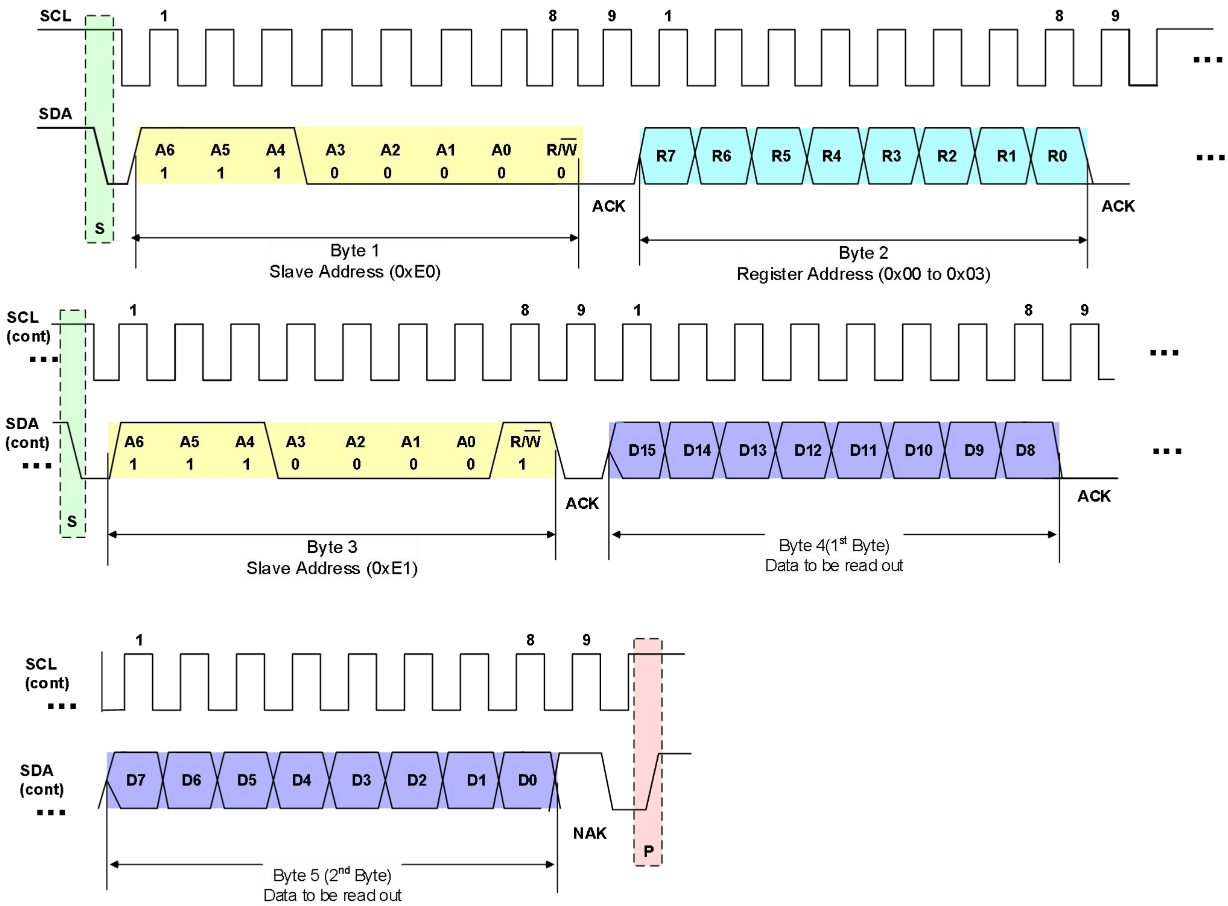


Figure-4. SMBus / I²C Read Double Bytes Timing Diagram

Function Description

Overview

The chip can sense temperature and convert it into digital data by a 12-bit ADC. Also the chip supports programmable high-/low-limit temperature settings. If the measured temperature is higher than the high-limit temperature, FH (Flag-High) bit will be set as '1'. Also once the measured temperature is lower than the low-limit temperature, LH (Flag-Low) bit will be set as '1'. If both flag bits remain 0, then the temperature is within the temperature window set by the temperature limit registers, as shown in Figure-5.

Digital Output of Temperature Data

The temperature measurement data is stored in Read Only temperature register. The temperature register is in 12-bit binary format with 2-Byte. The relationship between Temperature data in Celsius degree and binary data is shown as below tables.

Table-1. Sensor Temperature vs. 12-bit Digital Data

Temperature (°C)	12-bit Digital Output (HEX)	12-bit Digital Output (BIN)
+150	0x7FF0	0111,1111,1111 (0000)
+128	0x7FF0	0111,1111,1111 (0000)
+127.9375	0x7FF0	0111,1111,1111 (0000)
+100	0x6400	0110,0100,0000 (0000)
+25	0x1900	0001,1001,0000 (0000)
+0.25	0x0040	0000,0000,0100 (0000)
0	0x0000	0000,0000,0000 (0000)
-0.0625	0xFFF0	1111,1111,1111 (0000)
-0.25	0xFFC0	1111,1111,1100 (0000)
-25	0xE700	1110,0111,0000 (0000)
-40	0xD800	1101,1000,0000 (0000)

Register Map

The chip has 5 registers, shown as below table. 16-bit / 8-bit data can be read out and written at one time via read or write 1-byte / 2-byte operation command.

Table-2. Register Map

Register Address	Register Name	Attribution	Default Data	BIT							
				7	6	5	4	3	2	1	0
0x00	Temp (1st Byte)	R	N/A	Temp_ Data [11]	Temp_ Data [10]	Temp_ Data [9]	Temp_ Data [8]	Temp_ Data [7]	Temp_ Data [6]	Temp_ Data [5]	Temp_ Data [4]
	Temp (2nd Byte)			Temp_ Data [3]	Temp_ Data [2]	Temp_ Data [1]	Temp_ Data [0]	0	0	0	0
0x01	Config	R/W	0x02	ID	CR1	CR0	FH	FL	LC	M1	M0
0x02	Low_Temp_Set	R/W	0xF6	Low_Temp _Setup_ Data [7]	Low_Temp _Setup_ Data [6]	Low_Temp _Setup_ Data [5]	Low_Temp _Setup_ Data [4]	Low_Temp _Setup_ Data [3]	Low_Temp _Setup_ Data [2]	Low_Temp _Setup_ Data [1]	Low_Temp _Setup_ Data [0]
0x03	High_Temp_Set	R/W	0x3C	High_Temp _Setup_ Data [7]	High_Temp _Setup_ Data [6]	High_Temp _Setup_Dat a [5]	High_Temp _Setup_ Data [4]	High_Temp _Setup_ Data [3]	High_Temp _Setup_ Data [2]	High_Temp _Setup_ Data [1]	High_Temp _Setup_ Data [0]
0x07	Manufacture ID	R	0x59	0	1	0	1	1	0	0	1

Register Description

Temp_Data, Temperature Data

- Register Address: 0x00
- Register Attribution: Read only
- Default Data: N/A

BIT (1st Byte)	7	6	5	4	3	2	1	0
Name: Temp_MSB (1st Byte)	Temp_Data [11:4]							
Temperature Data (°C)	SIGN	64	32	16	8	4	2	1
	T11	T10	T9	T8	T7	T6	T5	T4

BIT (2nd Byte)	7	6	5	4	3	2	1	0
Name: Temp_LSB (2nd Byte)	Temp_Data [3:0]							
Temperature Data (°C)	0.5	0.25	0.125	0.0625	-	-	-	-
	T3	T2	T1	T0	-	-	-	-

Note:

(1) The 1st byte can be read out independently by a "Not Ack" right after itself and before the "STOP". In other words, user will get the 1°C resolution temperature data with one byte read timing (refer to Figure 3).

Config, Configuration Setup register

- Register Address: 0x01
- Register Attribution: Read/Write
- Default Data: 0x02 after POR. If user used only 1-Byte, it is ok to read/write 1-Byte command via digital interface; the 1st Byte (MSB) will be accessed.

BIT	7	6	5	4	3	2	1	0
0x01	ID	CR1	CR0	FH	FL	LC	M1	M0
Default	0	0	0	0	0	0	1	0
R/W	R	RW	RW	R	R	RW	RW	RW

BIT NO.	Name	Description
7	ID	Reserved, read only, default is 0.
6-5	CR[1:0]	**Conversion Rate Setting bits** 00 : 0.25 Hz / 4.0 s (default) 01 : 1.0 Hz / 1.0 s 10 : 4.0 Hz / 0.25 s 11 : 8.0 Hz / 0.125 s
4	FH	**Flag-High bit** 0 : Measured temperature is higher than *High_Temp_Set* 1 : Measured temperature is higher than *High_Temp_Set*
3	FL	**Flag-Low bit** 0 : Measured temperature is lower than *Low_Temp_Set* 1 : Measured temperature is lower than *Low_Temp_Set*
2	LC	**Latch bit** 0 : FH and FL bits cannot be cleared by read operation.(default) 1 : FH and FL bits can be cleared by read operation (Latch Mode).
1-0	M1,M0	**Operation Mode control bit** 00 : Shutdown mode 01 : One-shot operation when PJ85753 in shutdown mode. 1x : Continuous Conversion Mode. (default)

CR1, CR0, Conversion Rate Setting bits

These 2 bits allow user to setup different conversion rate for temperature measurement. The default is 00 after POR, which means the conversion rate is 0.25 Hz, i.e. one time conversion every 4 seconds.

CR1	CR0	Conversion Rate	Conversion Period
0	0	0.25 Hz (default)	4.0 s (default)
0	1	1.0 Hz	1.0 s
1	0	4.0 Hz	0.25 s
1	1	8.0 Hz	0.125 s

FH, Flag-High bit; FL, Flag-Low bit (read only)

This FH bit indicates the status of the chip measured temperature exceeds High_Temp_Set register data (Register Add, 0x03). If measured temperature is higher than that of High_Temp_Set register data, it will trigger over temperature status, this FH bit will be set as '1'. Also once measured temperature drops below Low_Temp_Set register data (Register Add = 0x02), the FL bit will be reset as '1'. If both flag bits remain 0, then the temperature is within the temperature window set by the temperature limit registers, as shown in Figure-5.

LC, Latch bit

The latch bit (LC) in the configuration register is used to latch the value of the flag bits (FH and FL) until the master issues a read command to the configuration register. The flag bits are set to 0 if a read command is received by the PJ85753, or if LC = 0 and the temperature is within the temperature limits. The power-on default values for these bits are FH = 0, FL = 0, and LC = 0.

Shutdown Mode (M1=0, M0=0)

These bits allow user to shutdown the chip and to make the chip enter shutdown mode once writing 00B to bits M1 and M0 in configuration resister after the accomplishment of the current conversion process. During shutdown mode, the temperature data is kept at that of last time, no more update, and all function blocks are turned-off except interface. In shutdown mode, the quiescent is 30 nA (Typ.).

One-Shot (M1 = 0, M0 = 1)

The PJ85753 features a One-Shot Temperature Measurement mode. When the device is in Shutdown mode, writing a 01B to bits M1 and M0 starts a single temperature conversion. During the conversion, bits M1 and M0 read 01. The device returns to the shutdown state at the completion of the single conversion. After the conversion, bits M1 and M0 read 00. This feature is useful for reducing power consumption in the chip when continuous temperature monitoring is not required.

As a result of the short conversion time, the PJ85753 can achieve a higher conversion rate. A single conversion typically takes less 8 ms and a read can take place in less than 20 µs. When using One-Shot mode, 100 or more conversions per second are possible.

Continuous Conversion Mode (M1 = 1, M0 = 0 or 1)

When the PJ85753 is in Continuous Conversion mode (M1 = 1), a single conversion is performed at a rate determined by the conversion rate bits, CR1 and CR0 (in the Configuration Register). The PJ85753 performs a single conversion and then powers down and waits for the appropriate delay set by CR1 and CR0.

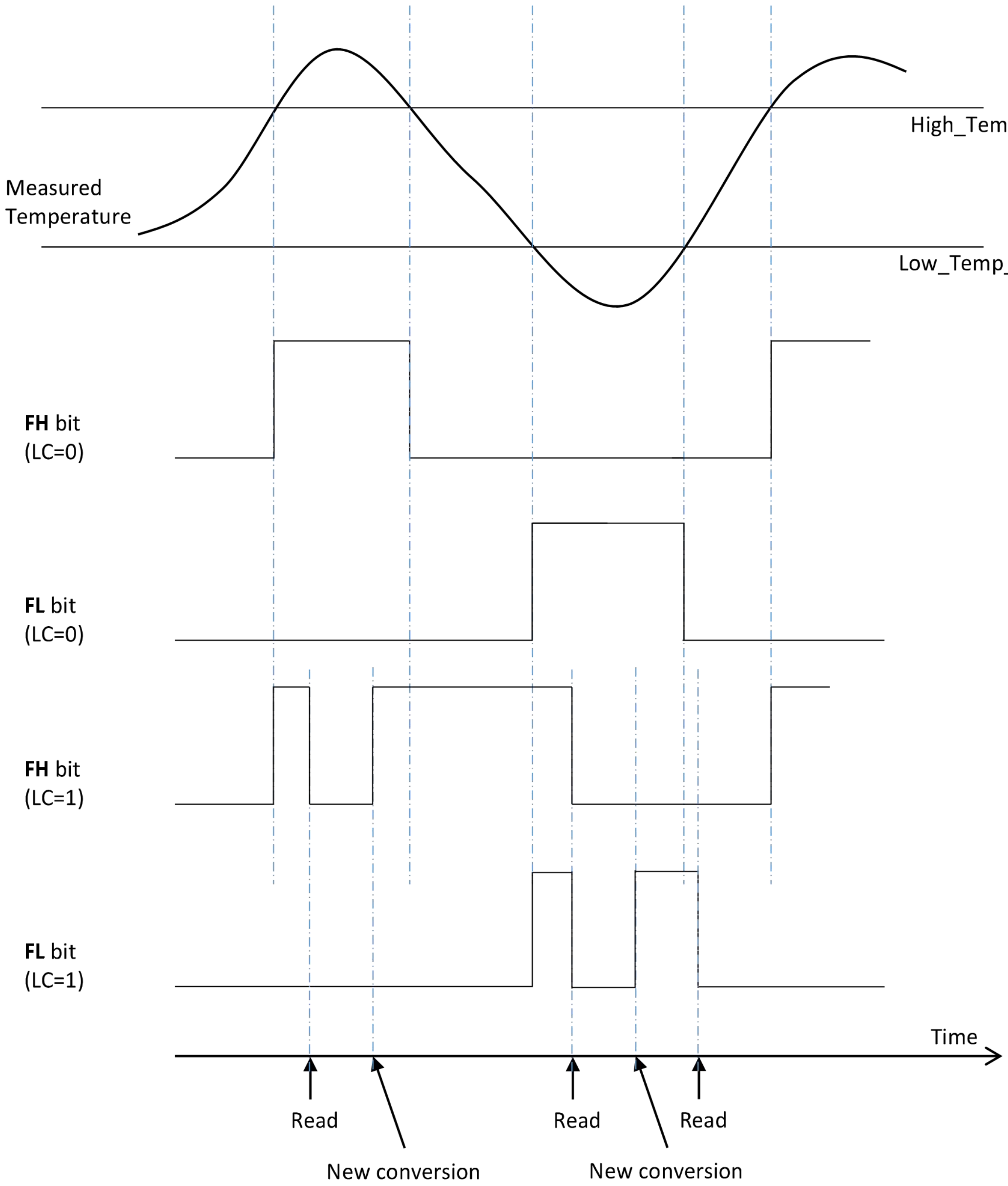


Figure-5. Temperature Flag Functional Diagram

Low_Temp_Set, Setup Low Temperature Limitation register

- Register Address: 0x02
- Register Attribution: Read/Write
- Default Data: 0xF6 after POR.

BIT	7	6	5	4	3	2	1	0
Low_Temp_Set	SIGN	64	32	16	8	4	2	1
Default	1	1	1	1	0	1	1	0

The low-limit temperatures is determined by Low_Temp_Set register [Reg Add, 0x02] with same format as Temp_Data register [Reg Add, 0x00], which could be in 8-bit or 12-bit binary format. The chip compares Temp_Data [0x00] register and High_Temp_Set register/Low_Temp_Set register in each conversion cycle, which will affect OTS bit. The default value is 0xF6 with 8-bit binary format, which means -10°C. For other default data of low-limit temperature, please contact our sales.

High_Temp_Set, Setup High Temperature Limitation register

- Register Address: 0x03
- Register Attribution: Read/Write
- Default Data: 0x3C after POR

BIT	7	6	5	4	3	2	1	0
High_Temp_Set	SIGN	64	32	16	8	4	2	1
Default	0	0	1	1	1	1	0	0

The high-limit temperature is determined by High_Temp_Set register [Reg Add, 0x03] with the same format as Temp_Data register [Reg Add, 0x00], which could be in 8-bit or 12-bit binary format. The chip compares Temp_Data register and High_Temp_Set register/Low_Temp_Set register in each conversion cycle, which will affect OTS bit. The default value is 0x3C with 8-bit binary format, which means 60°C. For other default data of high-limit temperature, please contact our sales

Manufacture ID

- Register Address: 0x07
- Register Attribution: Read Only
- Default Data: 0x59 after POR

BIT	7	6	5	4	3	2	1	0
Manufacture ID	M7	M6	M5	M4	M3	M2	M1	M0
Default	0	1	0	1	1	0	0	1

I²C Digital Interface

A standard I²C compatible 2-wire serial interface reads temperature data from the temperature registers (Reg Add, 0x00) and reads and writes configuration bits to and from the configuration registers (Reg Add, 0x01). Also the digital interface of this chip supports useful SMBus functions, including selectable bus timeout.

Timeout

The chip supports SMBus timeout. If the data (SDA PIN) or clock (SCL PIN) are held low for longer than 30 ms (Typ.) between a start and stop condition, the chip will reset the SMBus protocol and be ready for a new transmission.

Slave Address

The chip has 8 different slave addresses distinguished by suffix, shown as below table, which permit connecting total 8 chips in the same bus.

No.	Part No.	Slave Address in Hex [R/W]
1	PJ85753A	0xE1/0xE0
2	PJ85753B	0xE3/0xE2
3	PJ85753C	0xE5/0xE4
4	PJ85753D	0xE7/0xE6
5	PJ85753E	0xE9/0xE8
6	PJ85753F	0xEB/0xEA
7	PJ85753G	0xED/0xEC
8	PJ85753H	0xEF/0xEE
9	PJ85753J	0x91/0x90

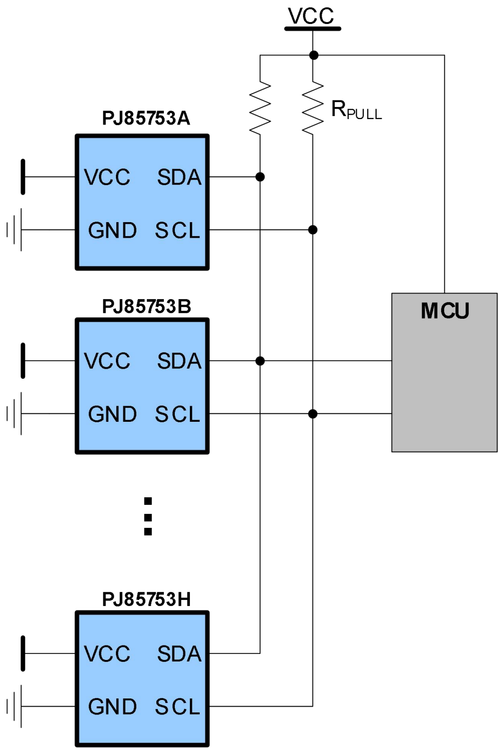


Figure-6. Multiple Devices Application with difference slave address

SMBus / I²C Protocol

The chip supports four standard SMBus / I²C protocols Send Byte, Read Byte, Write Byte and Receive Byte, shown as below tables.

Write Byte

S	Slave Address	W	A	Register Add	A	Register Data	NA	P

Read Byte

S	Slave Address	W	A	Register Add	A	Sr	Slave Address	R	A

Register Data	NA	P

Send Byte is similar as Write Byte without Register Add. Receive Byte is similar as Read Byte without Register Add.

Here S and Sr means SMBus Start to communication with master, P, means communication STOP.

A redundant STOP can be inserted before the Sr without affecting the read-out data.

Slave Address, means the chip's slave address.

Register Add, means pointed Register Address.

Register Data, means data to be written into register or read from register.

Compatible with SMBus

The chip is compatible with both SMBus and I²C. And the major difference between SMbus and I²C are shown as below. For more information, refer to SMBus specification v2.0 and I²C specification v2.1.

(1) This chip supports I^2C standard mode (up to 100 kHz), fast mode (up to 400 kHz) and high-speed mode (up to 3.4 MHz), which can cover SMBus maximum frequency 100 kHz.

(2) For SMBus protocol, the minimum frequency is 10 kHz due to time out feature. The slave device will reset if hold clock at '0' longer than 30 ms. There is no such limitation for I^2C.

(3) Logic levels are slight difference: V_{IL} (Max.) = 0.8 V (SMBus) vs. 30 %V_{CC} (I^2C); V_{IH} (Min.) = 2.1 V (SMBus) vs. 70 %V_{CC} (I^2C). If V_{CC} is over 3.0 V, there is almost no difference between SMBus and I^2C.

General Call

The PJ85753 device responds to a two-wire general-call address (0000 0000B). The device acknowledges the general-call address and responds to commands in the second byte. If the second byte is 0x06, the device will acknowledge the 0x06 command. After 2 ms (Typ.), the PJ85753 internal registers are reset to power-on reset values.

High-Speed Mode (HSM)

If I^2C/SMBus needs to run at frequencies above 400 kHz, the master device must issue an Hs-mode master code (0000 1xxx) as the first byte after a START condition to switch the bus to high-speed operation. After the Hs-mode master code has been issued, the master transmits a slave address to initiate a data-transfer operation. The bus continues to operate in Hs-mode until a STOP condition occurs on the bus. Upon receiving the STOP condition, the PJ85753 device will return back to fast-mode operation.

Multiple Device Access (MDA) Write

The master transmits an MDA write address to all devices on the same bus by 0x00 I^2C / SMBus address (general address), and all the registers of the devices will be modified. For example, three devices (PJ85753A, PJ85753B and PJ85753E) are connected to the same communication bus, the master transmits

S	0x00,general address	W	A	0x01,Register Add	A	0x62,data to be written	A	P

Then three registers (0x01 for PJ85753A, 0x01 for PJ85753B, 0x01 for PJ85753E) are all written to 0x62.

Multiple Device Access (MDA) Read

The master can read all devices on the same bus by 0x00 I^2C / SMBus address (general address), this MDA read process gets the data from the devices in a certain sequence, PJ85753A (0xE0) is the first order and the following is PJ85753B (0xE2), PJ85753C (0xE4), PJ85753D (0xE6), PJ85753E (0xE8), PJ85753F (0xEA), PJ85753G (0xEC), PJ85753H (0xEE), PJ85753J (0x90).

For example, three devices (PJ85753A, PJ85753B and PJ85753E) are on the same bus, the master will read temperature data (0x00) from all the devices. The master transmits.

PJ85753A, PJ85753B and PJ85753E the three devices return 0x1C, 0x1D and 0x1C. However, the devices except the above three return 0xFF because they are not on the communication bus.

If the master need only the former 5 devices data, it should respond acknowledge for the former four read data and not respond acknowledge for the fifth and transmits a stop as this communication end.

Applications Information

How to Improve Temperature Accuracy

The temperature measurement of the chip is based on semiconductor physics principle. Forward voltage of diode is a function of temperature. The formula is shown as below.

$$V_F = \frac{kT}{q} \ln\left(\frac{I_F}{I_S}\right)$$

Here,

V_F - forward voltage

I_F - forward current

I_S - reverse saturation current

k - Boltzmann constant

T - Temperature in K

q - electric charge constant

To cover wide temperature range, i.e. -40°C to 125°C, a very small voltage variation is corresponding to every degree C temperature change. MetaWells has applied many ways to improve measurement accuracy in chip circuits design, such as compensation, trimming etc. In real system design, however, some factors that can increase measurement error need to be considered.

Thermal Response Time

It is very necessary to wait enough time for obvious temperature changing of target due to thermal time constant. Although the single time measurement of temperature is 30 ms, enough time (at least 7 x τ) is still needed for the target device to reach thermal equilibrium. For this chip, the temperature step response changing from room temperature to 125°C shown the 1 x τ (63% of final) is approx. 2.0 s.

Self-heating

The average current is about 2.0 μA (Typ.) under VCC = 3.3 V, 1.0 Con./s condition, and the average power consumption is about 6.6 μW. The temperature rising caused by this power is too small (150 °C/W x 6.6 μW = 0.001°C) to be ignored. For this chip, it is no necessary to considerate temperature measurement accuracy caused by self-heating.

PCB Layout

Cautions below are important to improve temperature measurement in PCB layout design.

The Sensor placement

It is better to place the chip away from high speed digital bus (e.g. memory bus), coil devices (e.g. inductor) and wireless antenna (e.g. Bluetooth, WiFi, RF), and close to the target device to be monitored temperature.

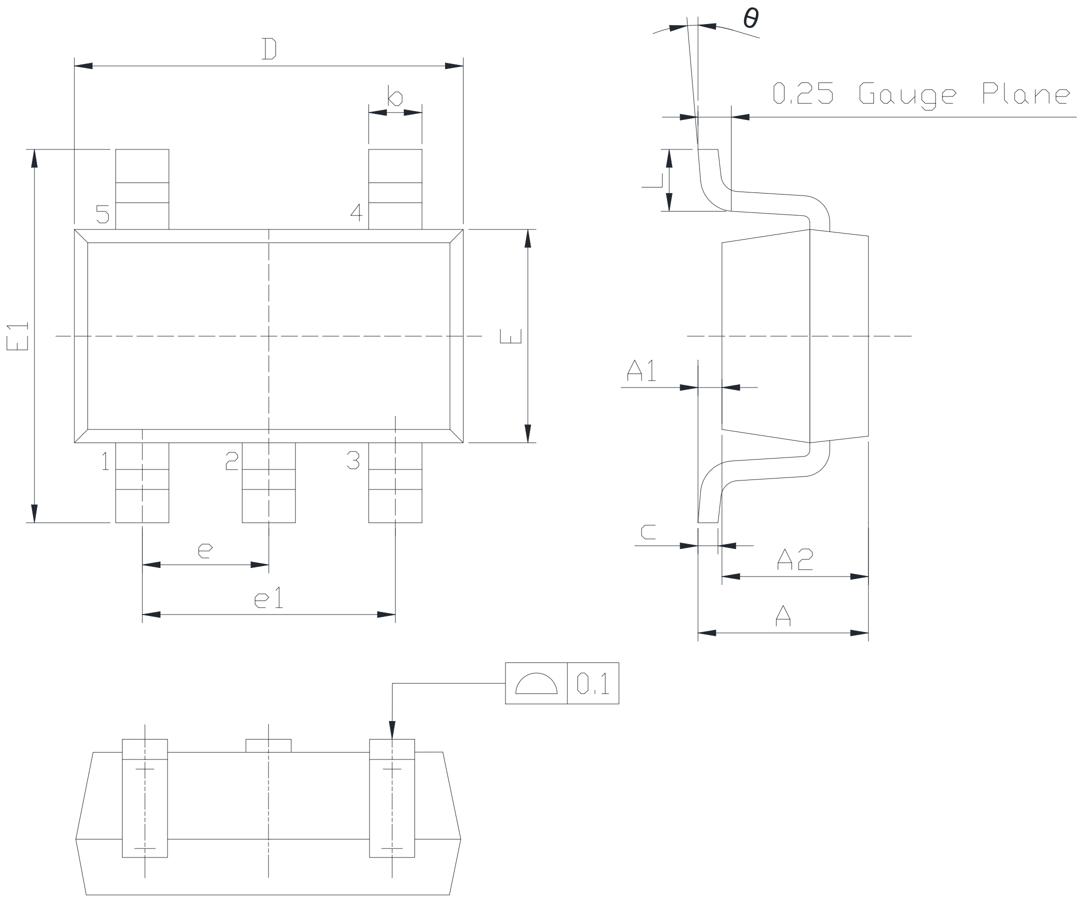
C_{IN}, Pull-up resistor

It is very necessary to place a low ESR ceramic cap (C_{IN}) between V_{CC} pin and GND pin to filter digital noise, although suppression noise circuit has been built inside the chip. This filter cap should be placed as possible as close to the chip. The recommended capacitance is 0.1 μF. In severely noisy condition, it is better to use multi caps in parallel, such as 1.0 μF plus 0.1 μF or 0.01 μF, which can suppress digital noise with wide frequency range.

User has to place a pull-up resistor with 4.7 k to 10 k for SDA and SCL pins respectively. It is ok to use smaller resistors such as 2 k – 3 k in real application, if multi slave devices are used in the same bus.

Package Outline Dimension-SOT23-5

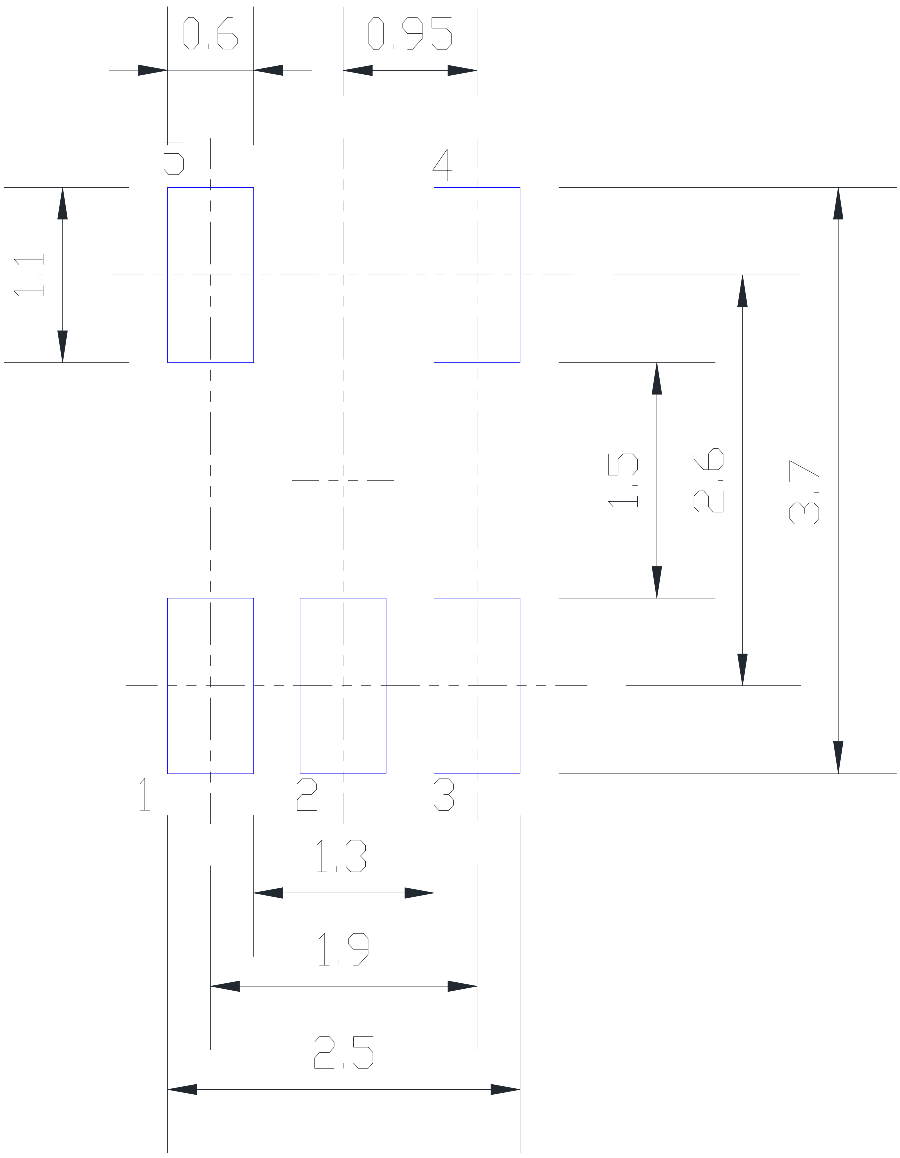
SOT23-5 Unit (mm)



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.000	1.450	0.039	0.057
A1	0.000	0.150	0.000	0.006
A2	1.000	1.200	0.039	0.047
b	0.300	0.500	0.012	0.020
C	0.100	0.200	0.004	0.008
D	2.720	3.120	0.107	0.123
E	1.400	1.800	0.055	0.071
E1	2.600	3.000	0.102	0.118
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Recommend Land Pattern Layout-SOT23-5

SC23-5 Unit (mm)



Note:

(1) All dimensions are in millimeter.

(2) Recommend tolerance is within ±0.1 mm.

Version History

Version	Date	Changes
Rev.1.0	2025-11-11	Initial release

Disclaimer

MetaWells Co., Ltd. and all other MetaWells Co., Ltd. trademarks are the exclusive property of MetaWells Co., Ltd.. Any mention of additional trademarks or registered trademarks in this document is made in acknowledgment of their respective owners.

Without the consent of MetaWells Co., Ltd. , any modification to any part or subsection of the company's product specifications and datasheets is strictly prohibited in any form or manner. MetaWells Co., Ltd. reserves the rights to make changes of the content herein the document follow PCN procedure. Please refer to our website for latest document. It is recommended that customers obtain the latest version of relevant information and verify its timeliness and completeness before placing an order. All products are sold in accordance with the terms and conditions provided in the sales contract at the time of order confirmation, which includes warranty scope, intellectual property rights, and liability limitations.

During the sales period, MetaWells Co., Ltd. guarantees that the performance of the products will be in accordance with the company's standard warranty. The company utilizes testing and other quality control techniques to ensure the necessity to maintain this warranty. Except for government-mandated requirements, there is no need for special testing of measurement tables or other instruments.

Customers must acknowledge that our products are not intended or manufactured for use in life support systems or other high-risk activities or environments. The utilization of our products in such applications may lead to severe consequences, including personal injury, loss of life, property damage, or environmental harm. Our products are explicitly not warranted for deployment in high-risk activities, and we shall bear no responsibility towards customers or third parties for such usage.

MetaWells Co., Ltd. commits to providing technical support, assistance, advice, and information, in line with our current capabilities, including guidance related to the design, development, or debugging of purchased boards or other applications. However, we hereby disclaim all warranties concerning technical support, merchantability, or fitness for a particular purpose. We do not guarantee the error-free operation of boards or applications in conjunction with our support services, and we shall not be held liable for any consequences arising from the utilization of our support services.

Website：www.MetaWells.com