PJ74LVC1G07 Datasheet

Single Buffer/Driver With Open-Drain Output In a SOT23-5 and SC70-5 Package

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General Description

The PJ74LVC1G07 is a single buffer/driver. The device is designed for 1.65 V to 5.5 V for V_{CC} operation, it can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

The output of the PJ74LVC1G07 device is open drain and can be connected to other open drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times. The CMOS device has high output drive while maintaining low static power dissipation over a broad V_{CC} operating range.

The PJ74LVC1G07 is available in SOT23-5 and SC70-5 packages.

Simplified Schematic

Features

- Wide Supply Voltage Range : 1.65 V to 5.5 V
- Max. T_{PD} of 4.2 ns at V_{CC} = 3.3 V
- Low Power Consumption, 10 µA (Max. I_{CC})
- ±24 mA Output Drive at V_{CC} = 3.3 V
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000 V Human-Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Operating temperature Range : -40˚C to 125°C
- Available Package : SOT23-5 and SC70-5

Applications

- Active Noise Cancellation (ANC)
- Blood Pressure Monitor
- Embedded PC
- Solid State Drive (SSD) : Client and Enterprise
- TV : LCD/Digital and High-Definition (HDTV)
- Tablet : Enterprise
- Video Analytics : Server
- Wireless Headset, Keyboard, and Mouse
- Power Supply : Telecom/Server AC/DC Controller

Ordering Information

Order number	Marking ID	Package	MSL	Description
PJ74LVC1G07S5	A9 DNN	SOT23-5	Level-3	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel
PJ74LVC1G07C5	A4 W	SC70-5	Level-3	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel

Note:

(1) Panjit can meet RoHS 2.0/REACH requirement. So most package types Panjit offers only states halogen free, instead of lead free.

Marking Information

Marking ID	Package	Definition
A9 DNN	SOT23-5	A9: Product code D: Date code NN: Serial number
A4 W	SC70-5	A4: Product code W: Week code

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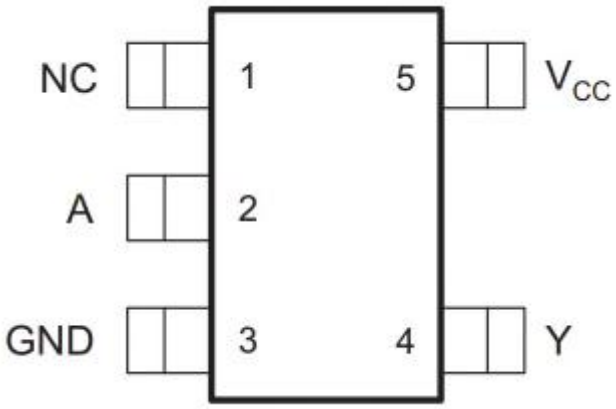
Pin Configuration



SOT23-5 and SC70-5 (Top View)

Functional Pin Description

Pin		Description
Name	Num	
NC	1	No Connect
A	2	Data Input
GND	3	Ground
Y	4	Data Output
V_{CC}	5	Supply Power Input

Function Table

H = HIGH voltage level; L = LOW voltage level

INPUTs	OUTPUT
A	**Y**
L	L
H	H

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter	Symbol	Value	Units
Supply Voltage	V_{CC}	-0.5 to 6.5	V
Input Voltage	V_I	-0.5 to 6.5	V
Voltage range applied to any output in the high-impedance or power-off state(2)	V_O	-0.5 to 6.5	V
Voltage range applied to any output in the high or low state(2)(3)	V_O	-0.5 to V_{CC}+0.5	V
Input clamp current, $V_I < 0$	I_{IK}	-50	mA
Output clamp current, $V_O < 0$	I_{OK}	-50	mA
Continuous output current	I_O	±50	mA
Storage temperature range	T_{STG}	-65 to 150	°C
ESD HBM, ANSI/ESDA/JEDEC JS-001(4)	ESD_{HBM}	±2000	V
ESD CDM, JESD22-C101(5)	ESD_{CDM}	±1000	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the Recommended Operating Conditions table.

(4) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(5) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			
Input voltage	V_I		0		5.5	V
Output voltage	V_O				V_{CC}	V
High-level input voltage	V_{IH}	V_{CC} = 1.65 V to 1.95 V	0.65 x V_{CC}			V
		V_{CC} = 2.3 V to 2.7 V	1.7			
		V_{CC} = 3 V to 3.6 V	2			
		V_{CC} = 4.5 V to 5.5 V	0.7 x V_{CC}			
Low-level input voltage	V_{IL}	V_{CC} = 1.65 V to 1.95 V			0.35 x V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V			0.7	
		V_{CC} = 3 V to 3.6 V			0.8	
		V_{CC} = 4.5 V to 5.5 V			0.3 x V_{CC}	
Low-level output current	I_{OL}	V_{CC} = 1.65 V			4	mA
		V_{CC} = 2.3 V			8	
		V_{CC} = 3 V			16	
		V_{CC} = 3 V			24	
		V_{CC} = 4.5 V			32	
Input transition rise or fall rate	$\triangle T/\triangle V$	V_{CC} = 1.8 V ±0.15 V, 2.5 V ±0.2 V			20	ns/V
		V_{CC} = 3.3 V ±0.3 V			10	
		V_{CC} = 5 V ±0.5 V			5	
Operating temperature	T_A		-40		125	°C

Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Low-level output voltage	V_{OL}	V_{CC} = 1.65~5.5 V, I_{OL} = 100 μA			0.1	V
		V_{CC} = 1.65 V, I_{OL} = 4 mA			0.45	
		V_{CC} = 2.3 V, I_{OL} = 8 mA			0.3	
		V_{CC} = 3 V, I_{OL} = 16 mA			0.4	
		V_{CC} = 3 V, I_{OL} = 24 mA			0.55	
		V_{CC} = 4.5 V, I_{OL} = 32 mA			0.55	
Input leakage current	I_I	V_{IN} = 5.5 V or GND, V_{CC} = 0~5.5 V			±5	μA
Power off leakage current	I_{OFF}	V_{IN} or GND, V_{CC} = 0~5.5 V			±10	μA
Quiescent supply current	I_Q	V_{IN} = V_{CC} or GND, I_{OUT} = 0, V_{CC} = 1.65~5.5 V			10	μA
Additional quiescent supply current per input pin	$\triangle I_Q$	V_{CC} = 3~5.5 V, one input ate V_{CC}-0.6 V, other input at V_{CC} or GND			500	μA

Switching Characteristics

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Propagation delay from input (A) to output (Y)	T_{PD}	V_{CC} = 1.8 V ± 0.15 V, R_L = 1 KΩ	C_L = 30 pF	2.4		8.3	nS
		V_{CC} = 2.5 V ± 0.2 V R_L = 500 Ω		1		5.5	nS
		V_{CC} = 3.3 V ± 0.3 V R_L = 500 Ω	C_L = 50 pF	1.5		4.2	nS
		V_{CC} = 5 V ± 0.5 V R_L = 500 Ω		1		3.5	nS

Typical Performance Characteristics

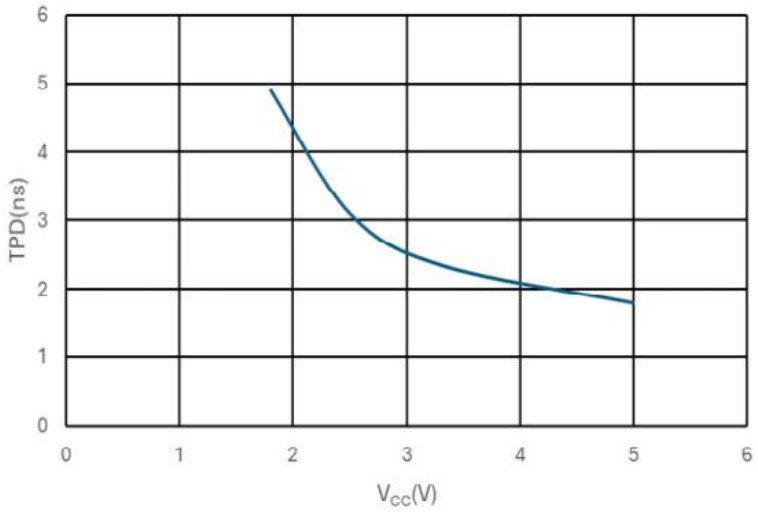
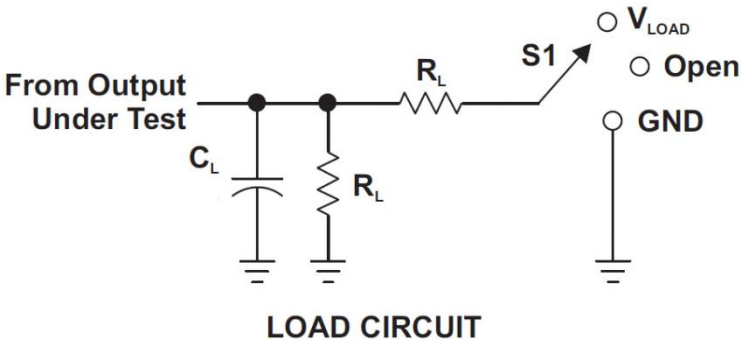


Figure 1. T_{PD} across V_{CC} at 25°C

Parameter Measurement Information



LOAD CIRCUIT

Test	Condition
t_{PLZ}	V_{LOAD}
t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2 x V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≤ 2 ns	$V_{CC}/2$	2 x V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≤ 2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤ 2.5 ns	$V_{CC}/2$	2 x V_{CC}	50 pF	500 Ω	0.3 V

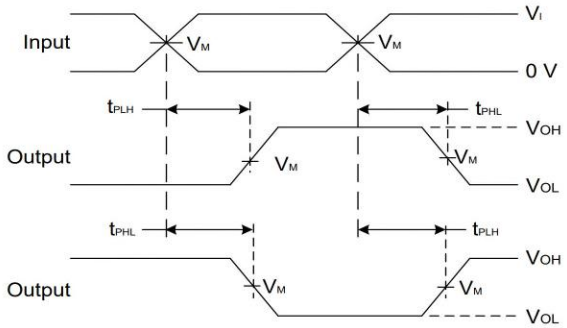


Figure 2. Voltage Waveform Propagation Delay Times Inverting and Non Inverting Outputs

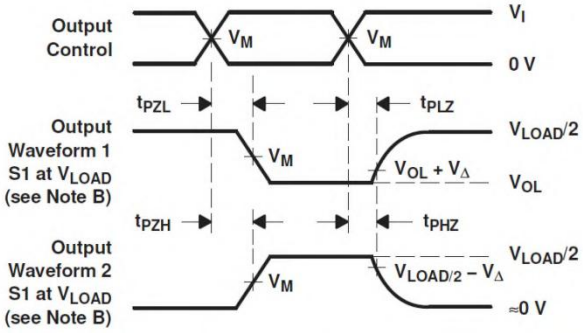


Figure 3. Voltage Waveform Enable and DisableTimes Low- and High-Level Enabling

Notes:

(1) C_L includes probe and jig capacitance.

(2) Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

(3) All pulses and supplied at pulse repetition rate ≤ 10 MHz.

(4) The Inputs are measured separately one transition per measurement.

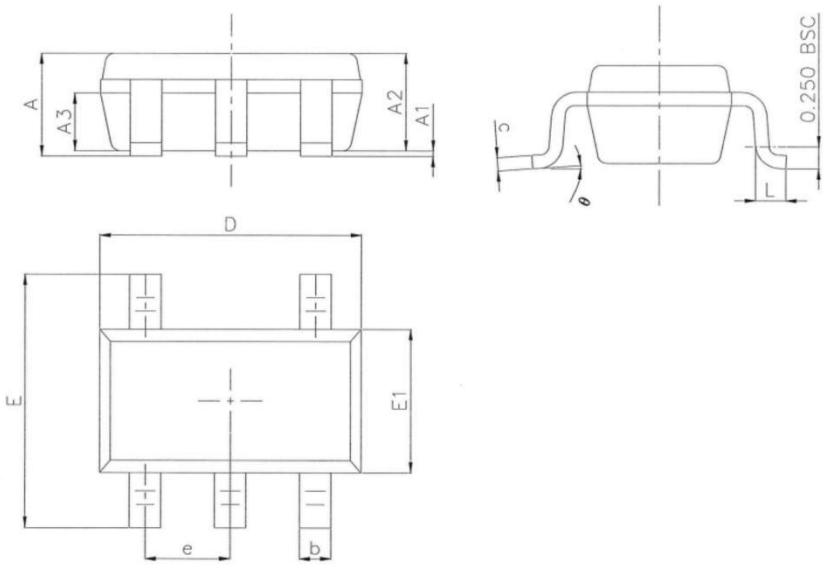
(5) Since this device has open-drain outputs, t_{PLH} and t_{PHL} are the same as t_{PD}.

(6) t_{PZL} is measured at V_M.

(7) t_{PLZ} is measured at $V_{OL} + V_\Delta$.

Package Outline Dimensions - SOT23-5

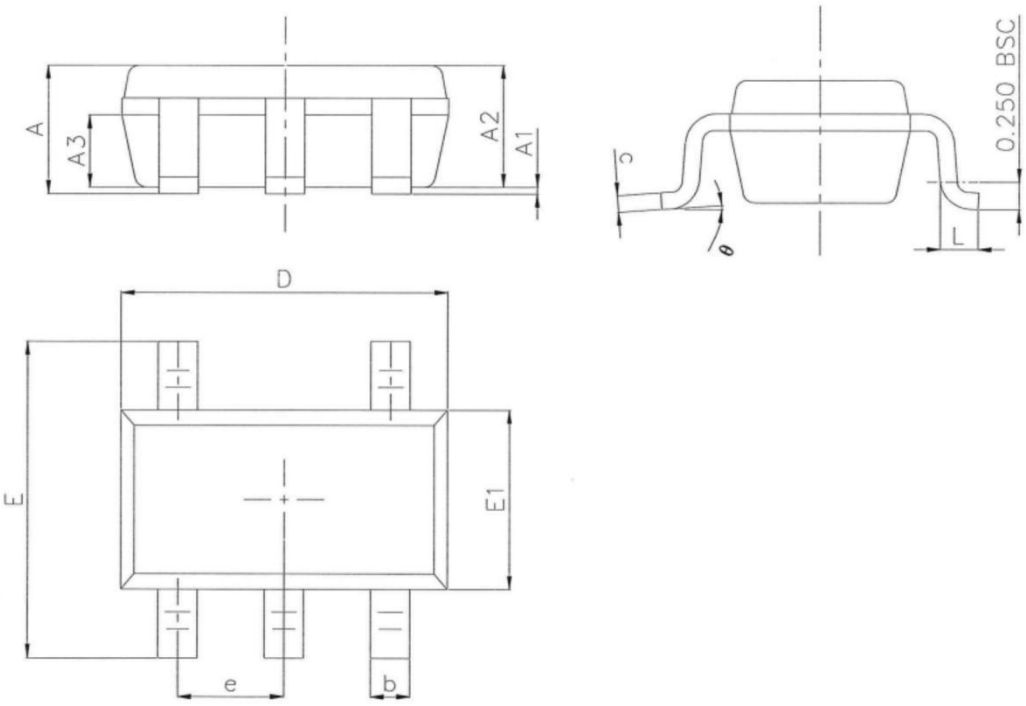
SOT23-5 Unit (mm)



Dimension in mm			
Symbol	**Min**	**Nom**	**Max**
A	1.050	1.150	1.250
A1	0.000	0.060	0.100
A2	1.000	1.100	1.200
A3	0.550	0.650	0.750
D	2.820	2.920	3.020
E1	1.510	1.610	1.700
E	2.650	2.800	2.950
b	0.300	0.400	0.500
e		0.950BSC	
θ	0°	4°	8°
L	0.300	0.420	0.570
c	0.100	0.152	0.200

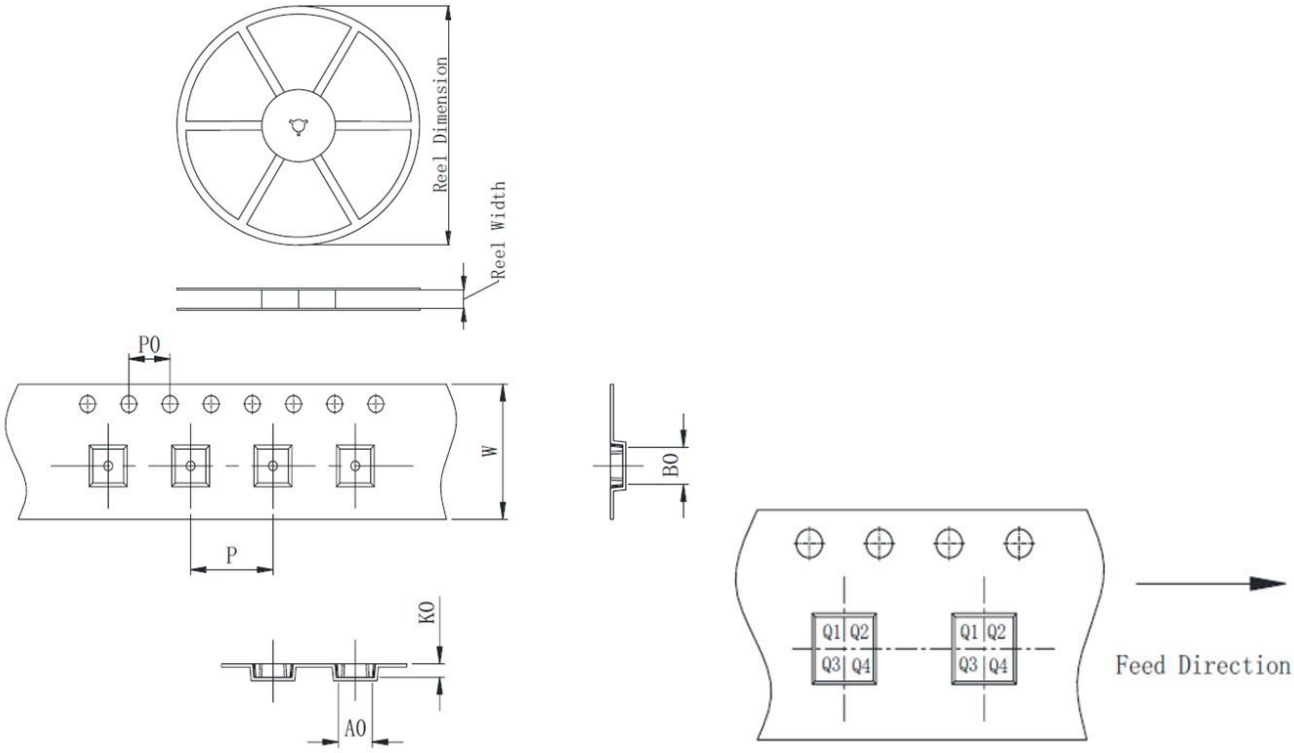
Package Outline Dimensions - SC70-5

SC70-5 Unit (mm)



Dimension in mm			
Symbol	**Min**	**Nom**	**Max**
A	0.90	0.95	1.00
A1	0.00	0.05	0.10
A2		0.9	
A3		0.55	
D	2.00	2.10	2.20
E1	1.15	1.25	1.35
E	2.00	2.10	2.20
b	0.15	0.225	0.30
e		0.65BSC	
θ	0°	4°	8°
L	0.26	0.35	0.46
c	0.10	0.15	0.20

Packing information



Package type	Reel size	Reel dimension (±3.0mm)	Reel width (±1.0mm)	A0 (±0.1mm)	B0 (±0.1mm)	K0 (±0.1mm)	P (±0.1mm)	P0 (±0.1mm)	W (±0.3mm)	Pin1
SOT23-5	7'	180	8.4	3.23	3.17	1.32	4.0	4.0	8.0	Q3
SC70-5	7'	180	8.4	3.23	3.17	1.32	4.0	4.0	8.0	Q3

Version History

Version	Date	Changes
Rev.1.0	2025-09-30	Initial release

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