

# **PJ74LVC1G86 Datasheet**

## **Single 2-Input Positive EXCLUSIVE-OR Gate In a SOT23-5 and SC70-5 Package**

**Version: Rev.1.0**

Release Date: 2025-11-11

MetaWells Co., Ltd.

[www.MetaWells.com](http://www.MetaWells.com)

## General Description

The PJ74LVC1G86 is a single 2-Input EXCLUSIVE-OR gate. The device is designed for 1.65 V to 5.5 V for  $V_{CC}$  operation, it can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

The PJ74LVC1G86 performs the Boolean function  $Y = \overline{A}B + A\overline{B}$  in positive logic.

If the input is low, the other input is reproduced in true form at the output. If the input is high, the signal on the other input is reproduced inverted at the output. This device has low power consumption with maximum  $T_{PD}$  of 4.0 ns at 3.3 V and 15 pF capacitive load.

The CMOS device has high output drive while maintaining low static power dissipation over a broad  $V_{CC}$  operating range.

The PJ74LVC1G86 is available in SOT23-5 and SC70-5 packages.

## Simplified Schematic



## Features

- ◆ Wide Supply Voltage Range : 1.65 V to 5.5 V
- ◆ Max.  $T_{PD}$  of 4.0 ns at  $V_{CC} = 3.3$  V
- ◆ Low Power Consumption, 10  $\mu$ A (Max.  $I_{CC}$ )
- ◆  $\pm 24$  mA Output Drive at  $V_{CC} = 3.3$  V
- ◆ Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ◆ ESD Protection Exceeds JESD 22
  - 2000 V Human-Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- ◆ Operating temperature Range :  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$
- ◆ Available Package : SOT23-5 and SC70-5

## Applications

- ◆ Active Noise Cancellation (ANC)
- ◆ Blood Pressure Monitor
- ◆ Embedded PC
- ◆ Solid State Drive (SSD) : Client and Enterprise
- ◆ TV : LCD/Digital and High-Definition (HDTV)
- ◆ Tablet : Enterprise
- ◆ Video Analytics : Server
- ◆ Wireless Headset, Keyboard, and Mouse
- ◆ Power Supply : Telecom/Server AC/DC Controller

## Ordering Information

### Ordering Information

Order number	Marking ID	Package	MSL	Description
PJ74LVC1G86S5	AD DNN	SOT23-5	Level-3	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel
PJ74LVC1G86C5	A9 W	SC70-5	Level-3	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel

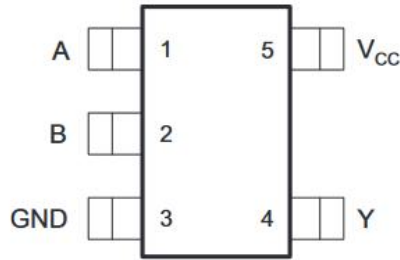
Note:

(1) MetaWells can meet RoHS 2.0/REACH requirement. So most package types MetaWells offers only states halogen free, instead of lead free.

### Marking Information

Marking	Package	Definition
AD DNN	SOT23-5	AD: Product code D: Date code NN: Serial number
A9 W	SC70-5	A9: Product code W: Week code

## Pin Configuration



SOT23-5 and SC70-5 (Top View)

## Pin Description

Pin		Function
Num	Name	
1	A	Data Input
2	B	Data Input
3	GND	Ground
4	Y	Data Output
5	V <sub>CC</sub>	Supply Power Input

## Function Table

*H = HIGH voltage level; L = LOW voltage level*

INPUTs		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

## Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

Parameter	Symbol	Value	Units
Supply Voltage	$V_{CC}$	-0.5 to 6.5	V
Input Voltage	$V_I$	-0.5 to 6.5	V
Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	$V_O$	-0.5 to 6.5	V
Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	$V_O$	-0.5 to $V_{CC}+0.5$	V
Input clamp current, $V_I < 0$	$I_{IK}$	-50	mA
Output clamp current, $V_O < 0$	$I_{OK}$	-50	mA
Continuous output current	$I_O$	$\pm 50$	mA
Storage temperature range	$T_{STG}$	-65 to 150	$^{\circ}C$
ESD HBM, ANSI/ESDA/JEDEC JS-001 <sup>(4)</sup>	$ESD_{HBM}$	$\pm 2000$	V
ESD CDM, JESD22-C101 <sup>(5)</sup>	$ESD_{CDM}$	$\pm 1000$	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of  $V_{CC}$  is provided in the Recommended Operating Conditions table.

(4) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(5) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	$V_{CC}$	Operating	1.65		5.5	V
		Data retention only	1.5			
Input voltage	$V_I$		0		5.5	V
Output voltage	$V_O$				$V_{CC}$	V
High-level input voltage	$V_{IH}$	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$			V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7			
		$V_{CC} = 3\text{ V to }3.6\text{ V}$	2			
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$	$0.7 \times V_{CC}$			
Low-level input voltage	$V_{IL}$	$V_{CC} = 1.65\text{ V to }1.95\text{ V}$			$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$			0.7	
		$V_{CC} = 3\text{ V to }3.6\text{ V}$			0.8	
		$V_{CC} = 4.5\text{ V to }5.5\text{ V}$			$0.3 \times V_{CC}$	
High-level output current	$I_{OH}$	$V_{CC} = 1.65\text{ V}$			-4	mA
		$V_{CC} = 2.3\text{ V}$			-8	
		$V_{CC} = 3\text{ V}$			-16	
		$V_{CC} = 3\text{ V}$			-24	
		$V_{CC} = 4.5\text{ V}$			-32	
Low-level output current	$I_{OL}$	$V_{CC} = 1.65\text{ V}$			4	mA
		$V_{CC} = 2.3\text{ V}$			8	
		$V_{CC} = 3\text{ V}$			16	
		$V_{CC} = 3\text{ V}$			24	
		$V_{CC} = 4.5\text{ V}$			32	
Input transition rise or fall rate	$\Delta T/\Delta V$	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, 2.5\text{ V} \pm 0.2\text{ V}$			20	ns/V
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$			10	
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$			5	
Operating temperature	$T_A$		-40		125	°C

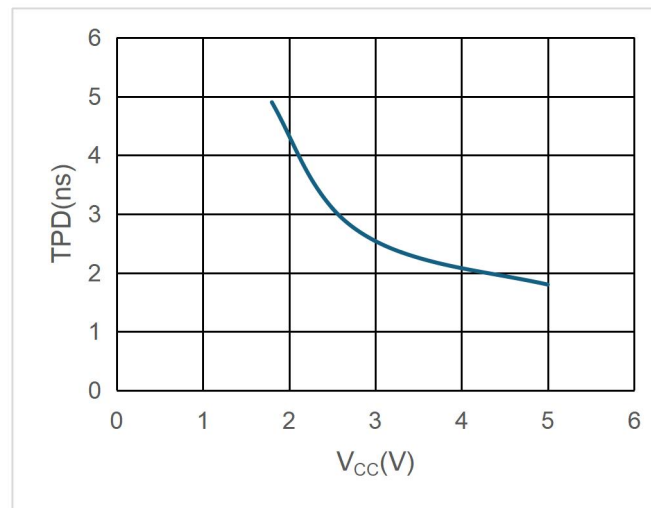
## Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High-level output voltage	$V_{OH}$	$V_{CC} = 1.65\sim 5.5\text{ V}, I_{OH} = -100\ \mu\text{A}$	$V_{CC}-0.1$			V
		$V_{CC} = 1.65\text{ V}, I_{OH} = -4\text{ mA}$	1.2			
		$V_{CC} = 2.3\text{ V}, I_{OH} = -8\text{ mA}$	1.9			
		$V_{CC} = 3\text{ V}, I_{OH} = -16\text{ mA}$	2.4			
		$V_{CC} = 3\text{ V}, I_{OH} = -24\text{ mA}$	2.3			
		$V_{CC} = 4.5\text{ V}, I_{OH} = -32\text{ mA}$	3.8			
Low-level output voltage	$V_{OL}$	$V_{CC} = 1.65\sim 5.5\text{ V}, I_{OL} = 100\ \mu\text{A}$			0.1	V
		$V_{CC} = 1.65\text{ V}, I_{OL} = 4\text{ mA}$			0.45	
		$V_{CC} = 2.3\text{ V}, I_{OL} = 8\text{ mA}$			0.3	
		$V_{CC} = 3\text{ V}, I_{OL} = 16\text{ mA}$			0.4	
		$V_{CC} = 3\text{ V}, I_{OL} = 24\text{ mA}$			0.55	
		$V_{CC} = 4.5\text{ V}, I_{OL} = 32\text{ mA}$			0.55	
Input leakage current	$I_L$	$V_{IN} = 5.5\text{ V or GND}, V_{CC} = 0\sim 5.5\text{ V}$			$\pm 5$	$\mu\text{A}$
Power off leakage current	$I_{OFF}$	$V_{IN} \text{ or GND}, V_{CC} = 0\sim 5.5\text{ V}$			$\pm 10$	$\mu\text{A}$
Quiescent supply current	$I_Q$	$V_{IN} = V_{CC} \text{ or GND}, I_{OUT} = 0,$ $V_{CC} = 1.65\sim 5.5\text{ V}$			10	$\mu\text{A}$
Additional quiescent supply current per input pin	$\Delta I_Q$	$V_{CC} = 3\sim 5.5\text{ V},$ one input at $V_{CC}-0.6\text{ V},$ other input at $V_{CC} \text{ or GND}$			500	$\mu\text{A}$

## Switching Characteristics

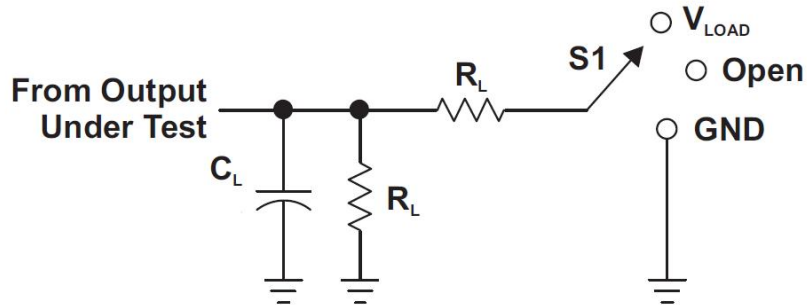
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	
Propagation delay from input (A or B) to output (Y)	$T_{PD}$	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$	$C_L = 15\text{ pF}$ $R_L = 1\text{ M}\Omega$		9.1	nS	
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$					2.1
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$					1
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$					0.6
			0.8		3.3	nS	

## Typical Performance Characteristics



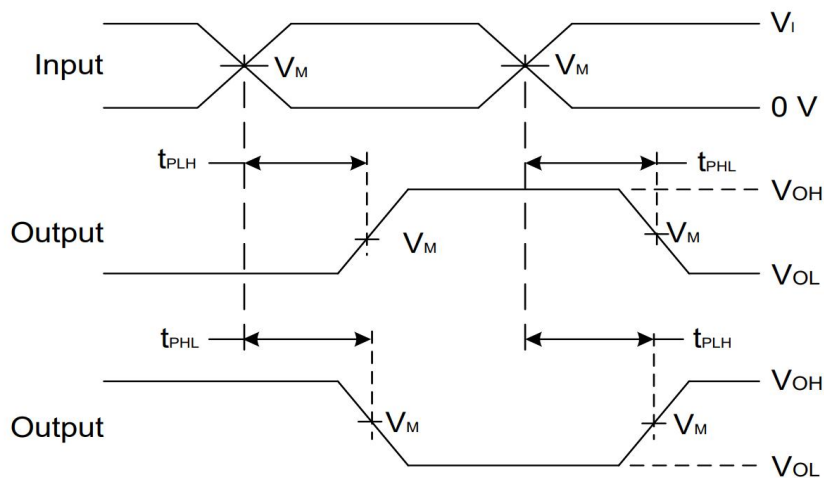
**Figure 1. T<sub>PD</sub> across V<sub>CC</sub> at 25°C**

## Parameter Measurement Information



**LOAD CIRCUIT**

$V_{CC}$	INPUTS		$V_M$	$C_L$	$R_L$
	$V_I$	$t_r/t_f$			
1.8 V $\pm$ 0.15 V	$V_{CC}$	$\cong 2$ ns	$V_{CC}/2$	15 pF	1 M $\Omega$
2.5 V $\pm$ 0.2 V	$V_{CC}$	$\cong 2$ ns	$V_{CC}/2$	15 pF	1 M $\Omega$
3.3 V $\pm$ 0.3 V	3 V	$\cong 2.5$ ns	1.5 V	15 pF	1 M $\Omega$
5 V $\pm$ 0.5 V	$V_{CC}$	$\cong 2.5$ ns	$V_{CC}/2$	15 pF	1 M $\Omega$



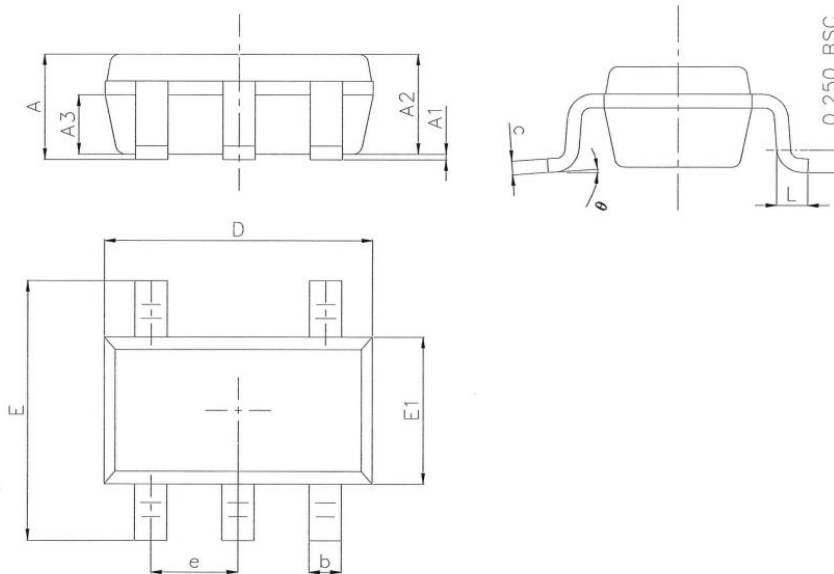
**Figure 2. Voltage waveform propagation delay times,  
Inverting and non-inverting outputs**

**Notes:**

- (1)  $C_L$  includes probe and jig capacitance.
- (2) All pulses and supplied at pulse repetition rate  $\leq 10$  MHz.
- (3) The Inputs are measured separately one transition per measurement.
- (4)  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PD}$ .

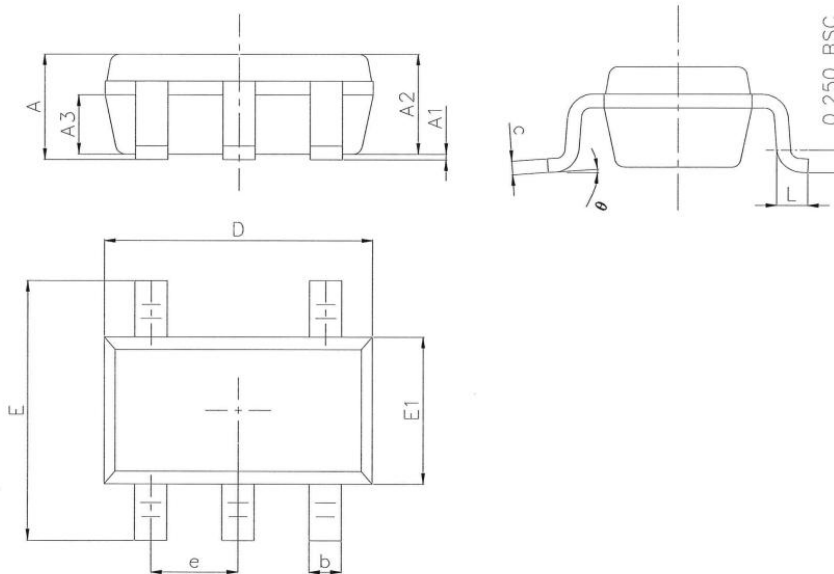
## Package Outline Dimension-SOT23-5

### SOT23-5 Unit (mm)



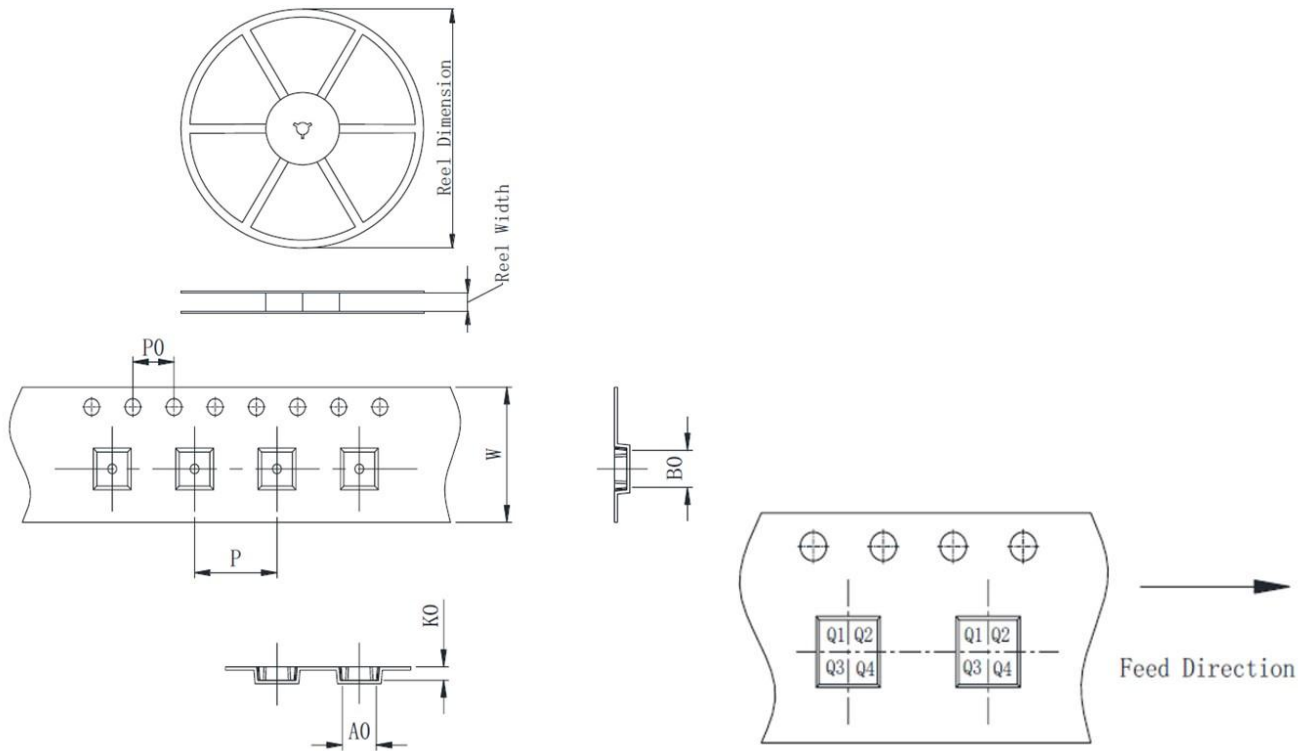
Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	1.050	1.150	1.250
A1	0.000	0.060	0.100
A2	1.000	1.100	1.200
A3	0.550	0.650	0.750
D	2.820	2.920	3.020
E1	1.510	1.610	1.700
E	2.650	2.800	2.950
b	0.300	0.400	0.500
e	0.950BSC		
θ	0°	4°	8°
L	0.300	0.420	0.570
c	0.100	0.152	0.200

## Package Outline Dimension-SC70-5

**SC70-5 Unit (mm)**


Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	0.90	0.95	1.00
A1	0.00	0.05	0.10
A2		0.9	
A3		0.55	
D	2.00	2.10	2.20
E1	1.15	1.25	1.35
E	2.00	2.10	2.20
b	0.15	0.225	0.30
e	0.65BSC		
$\theta$	0°	4°	8°
L	0.26	0.35	0.46
c	0.10	0.15	0.20

## Packing information



Package type	Reel size	Reel dimension (±3.0mm)	Reel width (±1.0mm)	A0 (±0.1mm)	B0 (±0.1mm)	K0 (±0.1mm)	P (±0.1mm)	P0 (±0.1mm)	W (±0.3mm)	Pin1
SOT23-5	7'	180	8.4	3.23	3.17	1.32	4.0	4.0	8.0	Q3
SC70-5	7'	180	8.4	3.23	3.17	1.32	4.0	4.0	8.0	Q3

## Version History

Version	Date	Changes
Rev.1.0	2025-11-11	Initial release

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