PJ74LV1T08 Datasheet

Single 2 Input Positive AND Gate CMOS Logic Level Shifter In a SOT23-5 and SC70-5 Package

Version：Rev.1.0

Release Date：2025-10-23

MetaWells Co., Ltd.

www.MetaWells.com

General Description

The PJ74LV1T08 is a single 2 input AND gate with reduced input thresholds to support voltage translation applications.

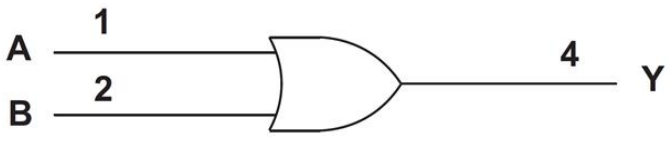
The PJ74LV1T08 device is a low-voltage CMOS gate logic that operates at a wider voltage range for industrial, portable, telecom, and automotive applications. The output level is referenced to the supply voltage and is able to support 1.8 V, 2.5 V, 3.3 V, and 5 V CMOS levels. The input is designed with a lower threshold circuit to match 1.8 V input logic at V_{CC} = 3.3 V and can be used in 1.8 V to 3.3 V level-up translation. In addition, the 5 V tolerant input pins enable down translation (that is, 3.3 V to 2.5 V output at V_{CC} = 2.5 V). The wide V_{CC} range of 1.8 V to 5.5 V allows generation of desired output levels to connect to controllers or processors. The PJ74LV1T08 device is designed with current-drive capability of 8 mA to reduce line reflections, overshoot, and undershoot caused by high-drive outputs.

The PJ74LV1T08 is available in SOT23-5 and SC70-5 packages.

Features

- Wide Operating Range : 1.8 V to 5.5 V
- Single-supply voltage translator at 5.0 V, 3.3 V, 2.5 V, and 1.8 V V_{CC}
- Up translation :
  - 1.2 V to 1.8 V at 1.8 V_{CC}
  - 1.5 V to 2.5 V at 2.5 V_{CC}
  - 1.8 V to 3.3 V at 3.3 V_{CC}
  - 3.3 V to 5.0 V at 5.0 V_{CC}
- Down translation :
  - 3.3 V to 1.8 V at 1.8 V_{CC}
  - 3.3 V to 2.5 V at 2.5 V_{CC}
  - 5.0 V to 3.3 V at 3.3 V_{CC}
- Logic output is referenced to V_{CC}
- Output Driver :
  - 8 mA Output Drive at 5 V
  - 7 mA Output Drive at 3.3 V
  - 3 mA Output Drive at 1.8 V
- Characterized up to 50 MHz at 3.3 V V_{CC}
- 5 V tolerance on input pins
- Supports standard logic pinouts
- Latch-up performance exceeds 250mA per JESD 17
- Operating temperature Range : -40°C to 125°C

Simplified Schematic



Applications

- Telecom
- Portable applications
- Servers
- PC and Notebooks

Ordering Information

Ordering Information

Order number	Marking ID	Package	MSL	Description
PJ74LV1T08S5	BT DNN	SOT23-5	Level-3	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel
PJ74LV1T08C5	AJ W	SC70-5	Level-3	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel

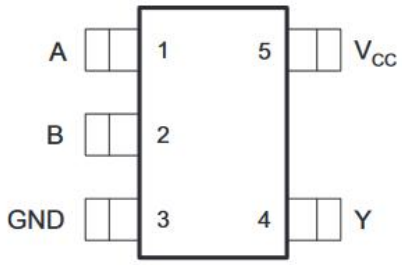
Note:

(1) MetaWells can meet RoHS 2.0/REACH requirement. So most package types MetaWells offers only states halogen free, instead of lead free.

Marking Information

Marking	Package	Definition
BT DNN	SOT23-5	BT: Product code D: Date code NN: Serial number
AJ W	SC70-5	AJ: Product code W: Week code

Pin Configuration



SOT23-5 and SC70-5 (Top View)

Pin Description

Pin		Function
Num	Name	
1	A	Data Input A
2	B	Data Input B
3	GND	Ground
4	Y	Data Output Y
5	V_{CC}	Supply Power Pin

Function Table

H = HIGH voltage level; L = LOW voltage level; X = do not care; Hi-Z = High impedance

INPUTs (Lower Level input)		**OUTPUT (V_{CC} CMOS)**
A	**B**	**Y**
H	H	H
L	X	L
X	L	L
SUPPLY V_{CC} = 3.3 V		
A	**B**	**Y**
V_{IH}(min) = 1.35 V V_{IL}(max) = 0.08 V		V_{OH}(min) = 2.9 V V_{OL}(max) = 0.2 V

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

Parameter	Symbol	Value	Units
Supply Voltage Range	V_{CC}	-0.5 to 7.0	V
Input Voltage Range(2)	V_I	-0.5 to 7.0	V
Voltage range applied to any output in the high-impedance or power-off state(2)	V_O	-0.5 to 4.6	V
Voltage range applied to any output in the high or low state(2)(3)	V_O	-0.5 to V_{CC}+0.5	V
Input clamp current, V_I < 0	I_{IK}	-20	mA
Output clamp current, V_O < 0 or V_O > V_{CC}	I_{OK}	±20	mA
Continuous output current	I_O	±25	mA
Junction temperature (Max.)	T_J	150	°C
Storage temperature range	T_{STG}	-65 to 150	°C
ESD HBM, ANSI/ESDA/JEDEC JS-001(4)	ESD_{HBM}	±2000	V
ESD CDM, ANSI/ESDA/JEDEC JS-002(5)	ESD_{CDM}	±1000	V

(1) Stresses beyond those listed under ***absolute maximum ratings*** may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ***recommended operating conditions*** is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the *Recommended Operating Conditions* table.

(4) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(5) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	1.6		5.5	V
Input voltage	V_I		0		5.5	V
Output voltage	V_O		0		V_{CC}	V
High-level output current	I_{OH}	V_{CC} = 1.8 V			-3	mA
		V_{CC} = 2.5 V			-5	
		V_{CC} = 3.3 V			-7	
		V_{CC} = 5.0 V			-8	
Low-level output current	I_{OL}	V_{CC} = 1.8 V			3	mA
		V_{CC} = 2.5 V			5	
		V_{CC} = 3.3 V			7	
		V_{CC} = 5.0 V			8	
Input transition rise or fall rate	△T/△V	V_{CC} = 1.8 V			20	ns/V
		V_{CC} = 3.3 V or 2.5 V			20	
		V_{CC} = 5.0 V			20	
Operating temperature	T_A		-40		125	°C

Electrical Characteristics for T_A = 25°C

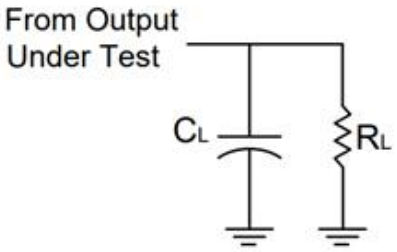
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High-level input voltage	V_{IH}	V_{CC} = 1.65 V to 1.8 V	0.94			V
		V_{CC} = 2.0 V	1.02			
		V_{CC} = 2.25 V to 2.5 V	1.135			
		V_{CC} = 2.75 V	1.21			
		V_{CC} = 3 V to 3.3 V	1.35			
		V_{CC} = 3.6 V	1.47			
		V_{CC} = 4.5 V to 5.0 V	2.02			
		V_{CC} = 5.5 V	2.1			
Low-level input voltage	V_{IL}	V_{CC} = 1.65 V to 2.0 V			0.58	V
		V_{CC} = 2.25 V to 2.75 V			0.75	
		V_{CC} = 3 V to 3.6 V			0.8	
		V_{CC} = 4.5 V to 5.5 V			0.8	
High-level output voltage	V_{OH}	V_{CC} = 1.65 V to 5.5 V, I_{OH} = -20 μA	V_{CC}-0.1			V
		V_{CC} = 1.65 V, I_{OH} = -2.0 mA	1.28			
		V_{CC} = 1.8 V, I_{OH} = -2.0 mA	1.5			
		V_{CC} = 2.3 V, I_{OH} = -2.3 mA	2.0			
		V_{CC} = 2.3 V, I_{OH} = -3.0 mA	2.0			
		V_{CC} = 2.5 V, I_{OH} = -3.0 mA	2.25			
		V_{CC} = 3.0 V, I_{OH} = -3.0 mA	2.78			
		V_{CC} = 3.0 V, I_{OH} = -5.5 mA	2.6			
		V_{CC} = 3.3 V, I_{OH} = -5.5 mA	2.9			
		V_{CC} = 4.5 V, I_{OH} = -4.0 mA	4.2			
		V_{CC} = 4.5 V, I_{OH} = -8.0 mA	4.1			
		V_{CC} = 5.0 V, I_{OH} = -8.0 mA	4.6			
Low-level output voltage	V_{OL}	V_{CC} = 1.65 V to 5.5 V, I_{OL} = 20 μA			0.1	V
		V_{CC} = 1.65 V, I_{OL} = 1.9 mA			0.2	
		V_{CC} = 2.3 V, I_{OL} = 2.3 mA			0.1	
		V_{CC} = 2.3 V, I_{OL} = 3.0 mA			0.15	
		V_{CC} = 3 V, I_{OL} = 3.0 mA			0.1	
		V_{CC} = 3 V, I_{OL} = 5.5 mA			0.2	
		V_{CC} = 4.5 V, I_{OL} = 4.0 mA			0.15	
		V_{CC} = 4.5 V, I_{OL} = 8.0 mA			0.3	
A input	I_{IN}	V_I = GND or V_{CC} V_{CC} = 0 V, 1.8 V, 2.5 V, 3.3 V, 5.5 V			0.12	μA
Supply current	I_{CC}	V_I = GND or V_{CC}, I_{OUT} = 0, V_{CC} = 1.8 V, 2.5 V, 3.3 V, and 5.5 V			1	μA

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Additional supply current per input pin	$\triangle I_{CC}$	V_{CC} = 5.5 V, I_{OUT} = 0, one input at 0.3 V or 3.4 V, other input at V_{CC} or GND			1.35	μA
		V_{CC} = 1.8 V, I_{OUT} = 0, one input at 0.3 V or 1.1 V, other input at V_{CC} or GND			10	μA

Switching Characteristics for T_A = 25°C

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Propagation delay from input (A or B) to output (Y)	T_{PD}	V_{CC} = 1.8 V ±0.15 V	C_L = 15 pF R_L = 1 MΩ		10.5	11	nS
		V_{CC} = 2.5 V ±0.2 V			6	6.5	nS
		V_{CC} = 3.3 V ±0.3 V			4.8	5	nS
		V_{CC} = 5 V ±0.5 V			4	5	nS

Parameter Measurement Information



V_{CC}	INPUTS		V_M	C_L	R_L
	V_I	t_r/t_f			
1.8 V ±0.15 V	V_{CC}	≦2 ns	$V_{CC}/2$	15 pF	1 MΩ
2.5 V ±0.2 V	V_{CC}	≦2 ns	$V_{CC}/2$	15 pF	1 MΩ
3.3 V ±0.3 V	3 V	≦2.5 ns	1.5 V	15 pF	1 MΩ
5 V ±0.5 V	V_{CC}	≦2.5 ns	$V_{CC}/2$	15 pF	1 MΩ

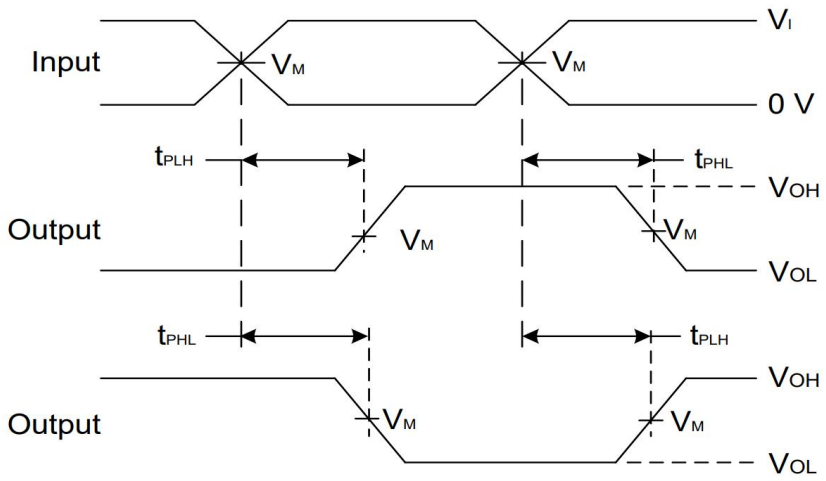


Figure 1. Voltage waveforms propagation delay times, Inverting and non-inverting outputs

Notes:

A. C_L includes probe and jig capacitance

B. All input pulses are supplied at pulse repetition rate ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns

C. The outputs are measured one at a time with one transition per measurement

D. For the open drain device t_{PLZ} and t_{PZL} are the same as t_{PD}

Application Information

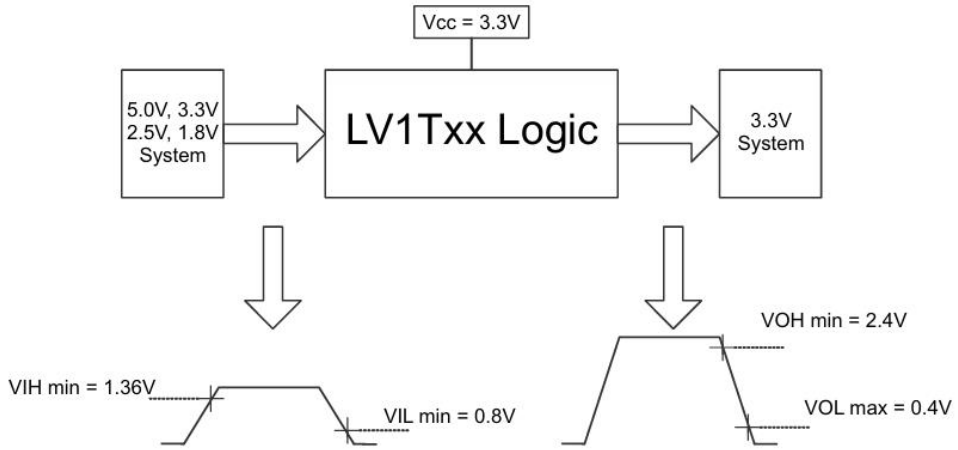


Figure 2. Switching Thresholds for 1.8 V to 3.3 V Translation

Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term balanced indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the Absolute Maximum Ratings must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

Up Translation

Input signals can be up translated using the PJ74LV1T08. The voltage applied at V_{CC} will determine the output voltage and the input thresholds as described in the Recommended Operating Conditions and Electrical Characteristics tables. When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels, which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5 V supply will have a $V_{IH(MIN)}$ of 3.5 V. For the PJ74LV1T08, $V_{IH(MIN)}$) with a 5 V supply is only 2 V, which would allow for up-translation from a typical 2.5 V to 5 V signals.

Ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in Figure 3.

Up Translation Combinations are as follows:

• 1.8 V V_{CC} – Inputs from 1.2 V

• 2.5 V V_{CC} – Inputs from 1.8 V

• 3.3 V V_{CC} – Inputs from 1.8 V and 2.5 V

• 5.0 V V_{CC} – Inputs from 2.5 V and 3.3 V

Down Translation

Signals can be translated down using the PJ74LV1T08. The voltage applied at the V_{CC} will determine the output voltage and the input thresholds as described in the Recommended Operating Conditions and Electrical Characteristics tables.

For example, standard CMOS inputs for devices operating at 5.0 V, 3.3 V or 2.5 V can be down-translated to match 1.8 V CMOS signals when operating from 1.8 V V_{CC}. See Figure 3.

Down Translation Combinations are as follows:

• 1.8 V V_{CC} – Inputs from 2.5 V, 3.3 V, and 5.0 V

• 2.5 V V_{CC} – Inputs from 3.3 V and 5.0 V

• 3.3 V V_{CC} – Inputs from 5.0 V

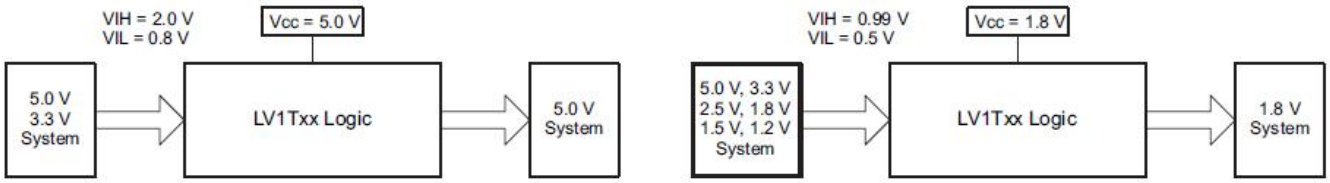


Figure 3. LVxT Up and Down Translation Example

Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

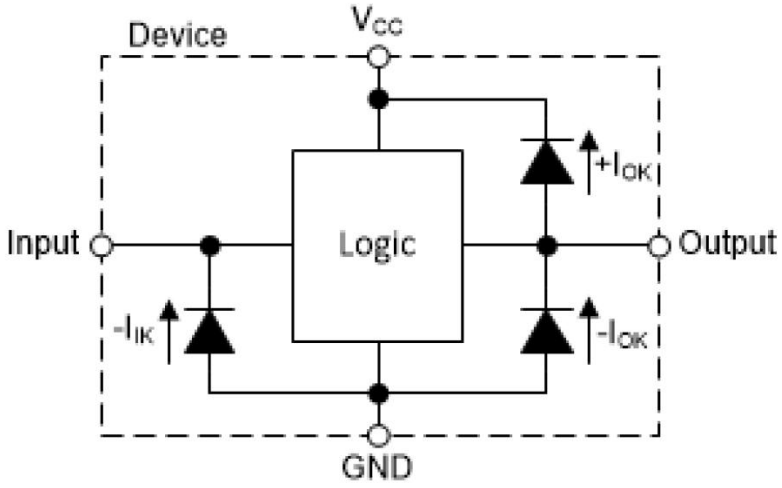


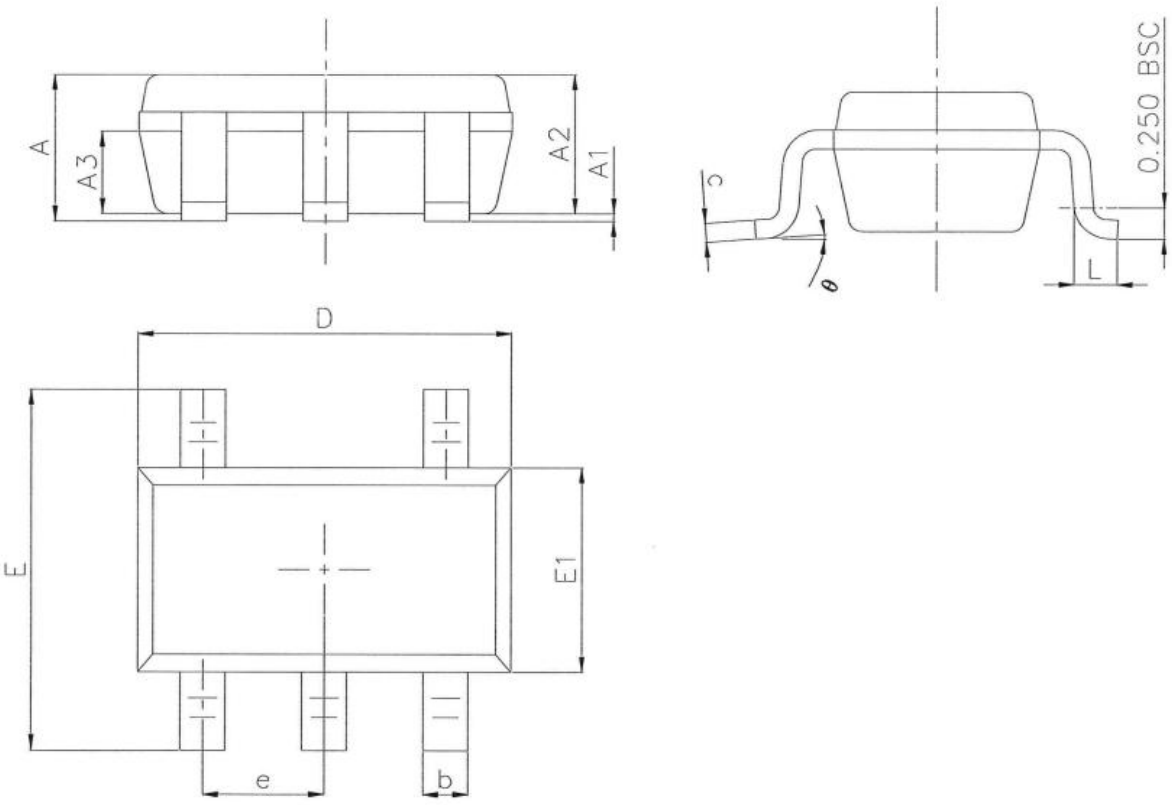
Figure 4. Electrical Placement of Clamping Diodes for Each Input and Output

Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table. Each Vcc pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF capacitor is recommended and if there are multiple Vcc pins then 0.01 μF or 0.022 μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1 μF and 1 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

Package Outline Dimension-SOT23-5

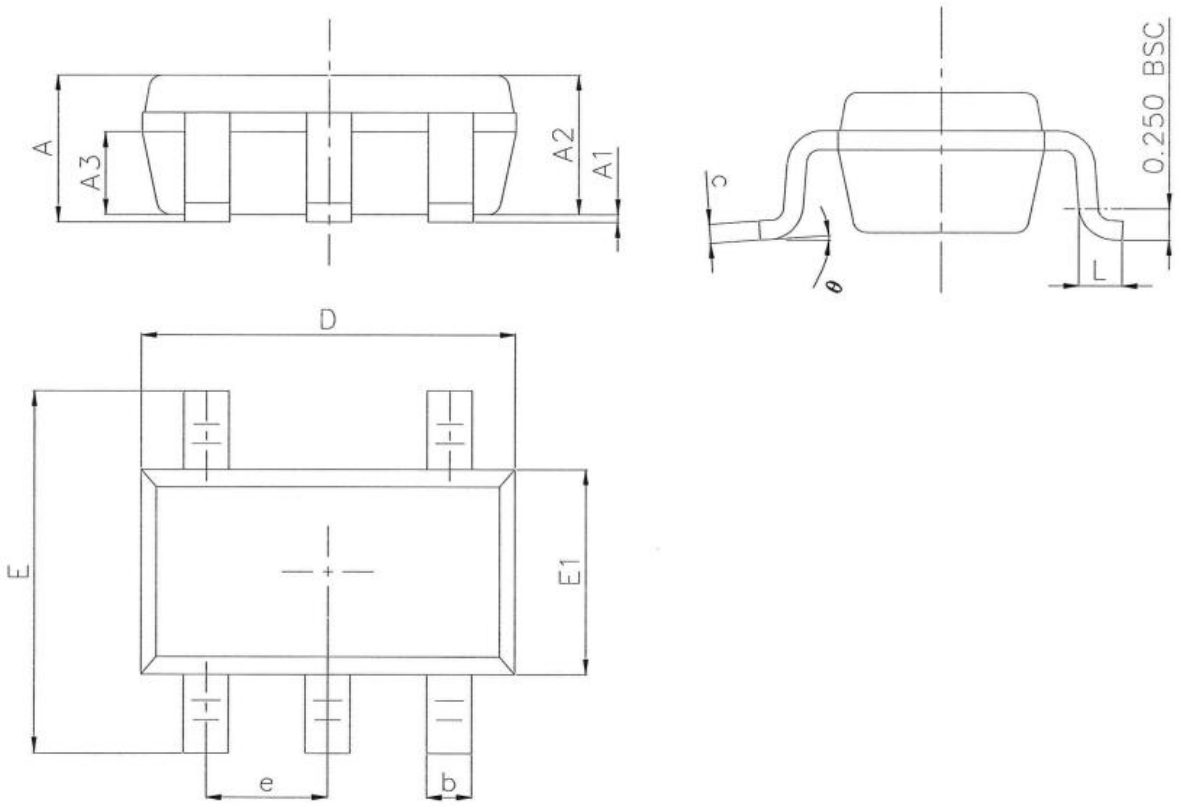
SOT23-5 Unit (mm)



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	1.050	1.150	1.250
A1	0.000	0.060	0.100
A2	1.000	1.100	1.200
A3	0.550	0.650	0.750
D	2.820	2.920	3.020
E1	1.510	1.610	1.700
E	2.650	2.800	2.950
b	0.300	0.400	0.500
e	0.950BSC		
θ	0°	4°	8°
L	0.300	0.420	0.570
c	0.100	0.152	0.200

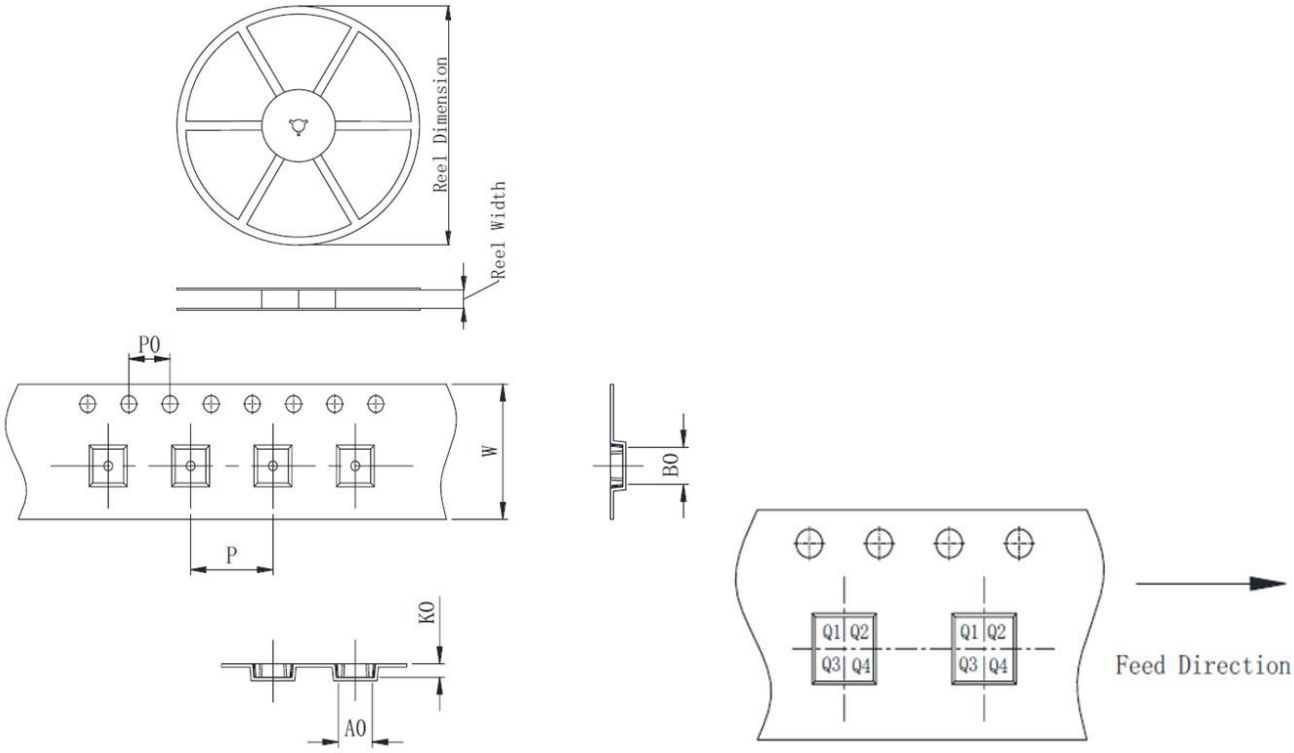
Package Outline Dimension-SC70-5

SC70-5 Unit (mm)



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	0.90	0.95	1.00
A1	0.00	0.05	0.10
A2		0.9	
A3		0.55	
D	2.00	2.10	2.20
E1	1.15	1.25	1.35
E	2.00	2.10	2.20
b	0.15	0.225	0.30
e	0.65BSC		
θ	0°	4°	8°
L	0.26	0.35	0.46
c	0.10	0.15	0.20

Packing information



Package type	Reel size	Reel dimension (±3.0mm)	Reel width (±1.0mm)	A0 (±0.1mm)	B0 (±0.1mm)	K0 (±0.1mm)	P (±0.1mm)	P0 (±0.1mm)	W (±0.3mm)	Pin1
SOT23-5	7'	180	8.4	3.23	3.17	1.32	4.0	4.0	8.0	Q3
SC70-5	7'	180	8.4	3.23	3.17	1.32	4.0	4.0	8.0	Q3

Version History

Version	Date	Changes
Rev.1.0	2025-10-23	Initial release

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