

PJ74LV1T32 Datasheet

Single Power Supply 2-input Positive OR Gate CMOS Logic Level Shifter

Version: Rev.1.0

Release Date: 2025-12-03

MetaWells Co., Ltd.

www.MetaWells.com

General Description

The PJ74LV1T32 is a single 2-input OR gate with reduced input thresholds to support voltage translation applications.

Applications

- ◆ Telecom
- ◆ Portable applications
- ◆ Servers
- ◆ PC and Notebooks

Simplified Schematic



Features

- ◆ Single-supply voltage translator at 5.0V, 3.3V, 2.5V, and 1.8V V_{CC}
- ◆ Operating range of 1.8V to 5.5V
- ◆ Up translation:
 - 1.2V to 1.8V at 1.8V V_{CC}
 - 1.5V to 2.5V at 2.5V V_{CC}
 - 1.8V to 3.3V at 3.3V V_{CC}
 - 3.3V to 5.0V at 5.0V V_{CC}
- ◆ Down translation:
 - 3.3V to 1.8V at 1.8V V_{CC}
 - 3.3V to 2.5V at 2.5V V_{CC}
 - 5.0V to 3.3V at 3.3V V_{CC}
- ◆ Output drive:
 - 8mA output drive at 5V
 - 7mA output drive at 3.3V
 - 3mA output drive at 1.8V
- ◆ Characterized up to 50MHz at 3.3V V_{CC}
- ◆ 5V tolerance on input pins
- ◆ -40°C to +125°C operating temperature range
- ◆ Supports standard logic pinouts

Ordering Information

Ordering Information

Order number	Marking ID	Package	MSL	Description
PJ74LV1T32S5	AKDNN	SOT23-5	Level-3	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel
PJ74LV1T32C5	BUW	SC70-5	Level-3	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel

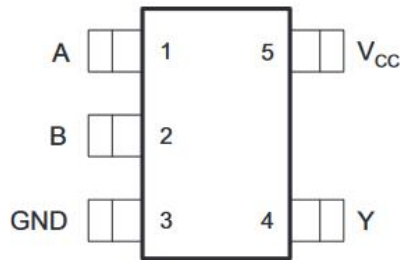
Note:

(1) MetaWells can meet RoHS 2.0/REACH requirement. So most package types MetaWells offers only states halogen free, instead of lead free.

Marking Information

Marking	Package	Definition
AKDNN	SOT23-5	AK: Product code D: Date code NN: Serial number
BUW	SC70-5	BU: Product code W: Week code

Pin Configuration



SOT23-5 and SC70-5 (Top View)

Pin Description

Pin		Function
Num	Name	
1	A	Data Input
2	B	Data Input
3	GND	Ground
4	Y	Output
5	V _{cc}	Power pin

Function Table

H = HIGH voltage level; L = LOW voltage level

INPUTs		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

Absolute Maximum Ratings

Parameter	Value	Units
V _{CC}	-0.5 to 7	V
V _I	-0.5 to 7	V
V _O (Voltage range applied to any output in the high-impedance or power-off state)	-0.5 to 4.6	V
V _O (Voltage range applied to any output in the high or slow state)	-0.5 to V _{CC} +0.5V	V
Input clamp current	-20	mA
Output clamp current	±20	mA
Continuous output current	±25	mA
Storage temperature	-65 to 150	°C

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V _{CC}	Operating	1.6		5.5	V
Input voltage	V _I		0		5.5	V
Output voltage	V _O		0		V _{CC}	V
High- level output current	I _{OH}	V _{CC} = 1.8V			-3	mA
		V _{CC} = 2.5V			-5	
		V _{CC} = 3.3V			-7	
		V _{CC} = 5.0V			-8	
Low- level output current	I _{OL}	V _{CC} = 1.8V			3	mA
		V _{CC} = 2.5V			5	
		V _{CC} = 3.3V			7	
		V _{CC} = 5.0V			8	
Input transition rise or fall rate	ΔT/ΔV	V _{CC} = 1.8V			20	ns/V
		V _{CC} = 3.3V or 2.5V			20	
		V _{CC} = 5V			20	
Operating temperature	T _A		-40		125	°C

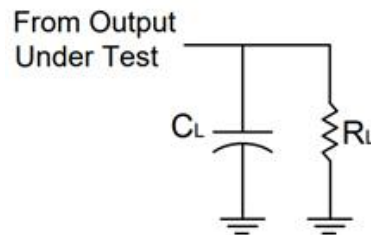
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
High- level input voltage	V_{IH}	$V_{CC} = 1.65\sim 1.8V$	0.95			V
		$V_{CC} = 2.0V$	0.99			
		$V_{CC} = 2.25\sim 2.5V$	1.135			
		$V_{CC} = 2.75V$	1.21			
		$V_{CC} = 3\sim 3.3V$	1.35			
		$V_{CC} = 3.6V$	1.47			
		$V_{CC} = 4.5V\sim 5.0V$	2.02			
		$V_{CC} = 5.5V$	2.1			
Low- level input voltage	V_{IL}	$V_{CC} = 1.65\sim 2.0V$			0.58	V
		$V_{CC} = 2.25\sim 2.75V$			0.75	
		$V_{CC} = 3\sim 3.6V$			0.8	
		$V_{CC} = 4.5V\sim 5.5V$			0.8	
High- level output voltage	V_{OH}	$V_{CC} = 1.65\sim 5.5V, I_{OH} = -20\mu A$	$V_{CC}-0.1$			V
		$V_{CC} = 1.65V, I_{OH} = -2mA$	1.28			
		$V_{CC} = 1.8V, I_{OH} = -2mA$	1.5			
		$V_{CC} = 2.3V, I_{OH} = -3mA$	2.0			
		$V_{CC} = 2.5V, I_{OH} = -3mA$	2.25			
		$V_{CC} = 3.0V, I_{OH} = -3mA$	2.78			
		$V_{CC} = 3.0V, I_{OH} = -5.5mA$	2.6			
		$V_{CC} = 3.3V, I_{OH} = -5.5mA$	2.9			
		$V_{CC} = 4.5V, I_{OH} = -4mA$	4.2			
		$V_{CC} = 4.5V, I_{OH} = -8mA$	4.1			
		$V_{CC} = 5.0V, I_{OH} = -8mA$	4.6			
Low- level output voltage	V_{OL}	$V_{CC} = 1.65\sim 5.5V, I_{OL} = 20\mu A$			0.1	V
		$V_{CC} = 1.65V, I_{OL} = 2.0mA$			0.2	
		$V_{CC} = 2.3V, I_{OL} = 3mA$			0.15	
		$V_{CC} = 3V, I_{OL} = 3mA$			0.1	
		$V_{CC} = 3V, I_{OL} = 5.5mA$			0.2	
		$V_{CC} = 4.5V, I_{OL} = 4mA$			0.15	
		$V_{CC} = 4.5V, I_{OL} = 8mA$			0.3	
Input leakage current	I_I	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 0\sim 5.5V$			0.1	μA
Supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0, V_{CC} = 1.8\sim 5.0V$			1	μA
Additional supply current per input pin	ΔI_{CC}	$V_{CC} = 5.5V$, one input at 0.3V or 3.4V, other input at V_{CC} or GND, $I_{OUT} = 0$			1.35	μA
		$V_{CC} = 1.8V$, one input at 0.3V or 1.1V, other input at V_{CC} or GND, $I_{OUT} = 0$			10	

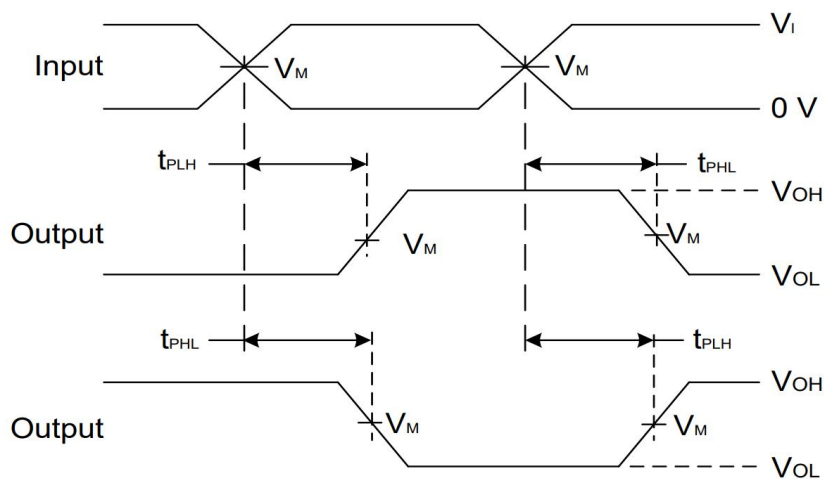
Switching Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	
Propagation delay from input(A) to output(Y)	T_{PD}	$V_{CC} = 5.0V$		4	5	nS	
		$V_{CC} = 3.3V$	$C_L = 15pF$ $R_L = 1M\Omega$		4.8	5	nS
		$V_{CC} = 2.5V$			6	6.5	nS
		$V_{CC} = 1.8V$			10.5	11	nS

Parameter Measurement Information



V_{CC}	INPUTS		V_M	C_L	R_L
	V_I	t_r/t_f			
$1.8 V \pm 0.15 V$	V_{CC}	$\cong 2 ns$	$V_{CC}/2$	15 pF	1 M Ω
$2.5 V \pm 0.2 V$	V_{CC}	$\cong 2 ns$	$V_{CC}/2$	15 pF	1 M Ω
$3.3 V \pm 0.3 V$	3 V	$\cong 2.5 ns$	1.5 V	15 pF	1 M Ω
$5 V \pm 0.5 V$	V_{CC}	$\cong 2.5 ns$	$V_{CC}/2$	15 pF	1 M Ω



**Figure 1. Voltage Waveform Propagation Delay Times
Inverting and Non Inverting Outputs**

Notes:

- (1) C_L includes probe and jig capacitance.
- (2) All pulses are supplied at pulse repetition rate $\leq 10MHz$.
- (3) t_{PLH} and t_{PHL} are the same as t_{PD} .

Application Information

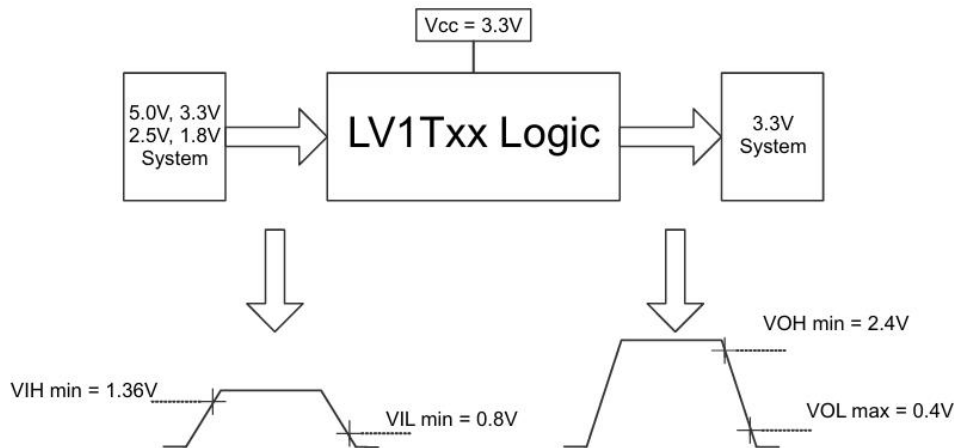


Figure 2. Switching Thresholds for 1.8 V to 3.3 V Translation

Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term balanced indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important to limit the output power of the device to avoid damage due to overcurrent. The electrical and thermal limits defined in the Absolute Maximum Ratings must be followed at all times.

Unused push-pull CMOS outputs must be left disconnected.

Up Translation

Input signals can be up translated using the PJ74LV1T32. The voltage applied at V_{CC} will determine the output voltage and the input thresholds as described in the Recommended Operating Conditions and Electrical Characteristics tables. When connected to a high-impedance input, the output voltage will be approximately V_{CC} in the HIGH state, and 0 V in the LOW state.

The inputs have reduced thresholds that allow for input HIGH state levels, which are much lower than standard values. For example, standard CMOS inputs for a device operating at a 5 V supply will have a $V_{IH(MIN)}$ of 3.5 V. For the PJ74LV1T32, $V_{IH(MIN)}$ with a 5 V supply is only 2 V, which would allow for up-translation from a typical 2.5 V to 5 V signals.

Ensure that the input signals in the HIGH state are above $V_{IH(MIN)}$ and input signals in the LOW state are lower than $V_{IL(MAX)}$ as shown in Figure 3.

Up Translation Combinations are as follows:

- 1.8 V V_{CC} – Inputs from 1.2 V
- 2.5 V V_{CC} – Inputs from 1.8 V
- 3.3 V V_{CC} – Inputs from 1.8 V and 2.5 V
- 5.0 V V_{CC} – Inputs from 2.5 V and 3.3 V

Down Translation

Signals can be translated down using the PJ74LV1T32. The voltage applied at the V_{CC} will determine the output voltage and the input thresholds as described in the Recommended Operating Conditions and Electrical Characteristics tables.

For example, standard CMOS inputs for devices operating at 5.0 V, 3.3 V or 2.5 V can be down-translated to match 1.8 V CMOS signals when operating from 1.8 V V_{CC} . See Figure 3.

Down Translation Combinations are as follows:

- 1.8 V V_{CC} – Inputs from 2.5 V, 3.3 V, and 5.0 V
- 2.5 V V_{CC} – Inputs from 3.3 V and 5.0 V
- 3.3 V V_{CC} – Inputs from 5.0 V

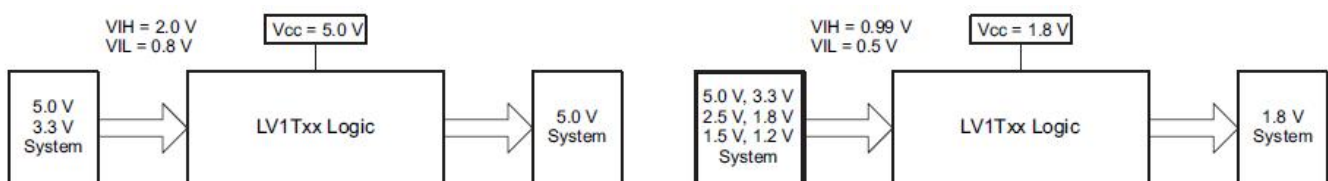


Figure 3. LV1Txx Up and Down Translation Example

Clamp Diode Structure

The outputs to this device have both positive and negative clamping diodes, and the inputs to this device have negative clamping diodes only.

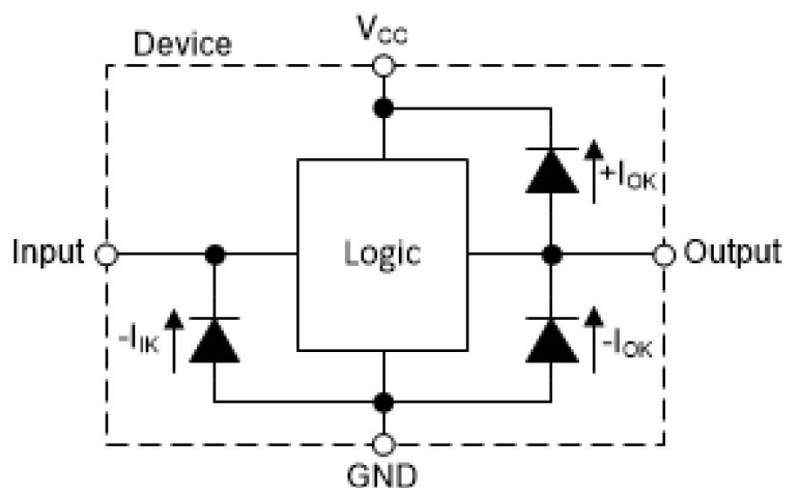


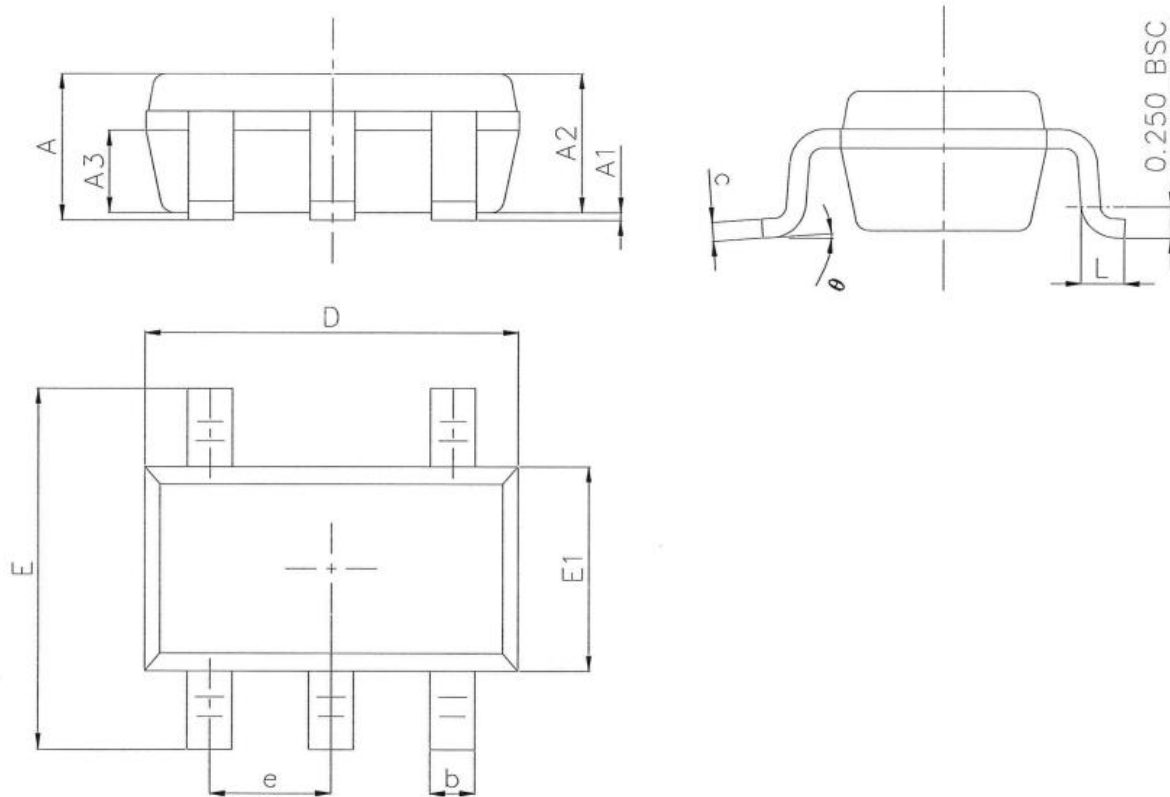
Figure 4. Electrical Placement of Clamping Diodes for Each Input and Output

Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table. Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF capacitor is recommended and if there are multiple V_{CC} pins then 0.01 μF or 0.022 μF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1 μF and 1 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

Package Outline Dimension-SOT23-5

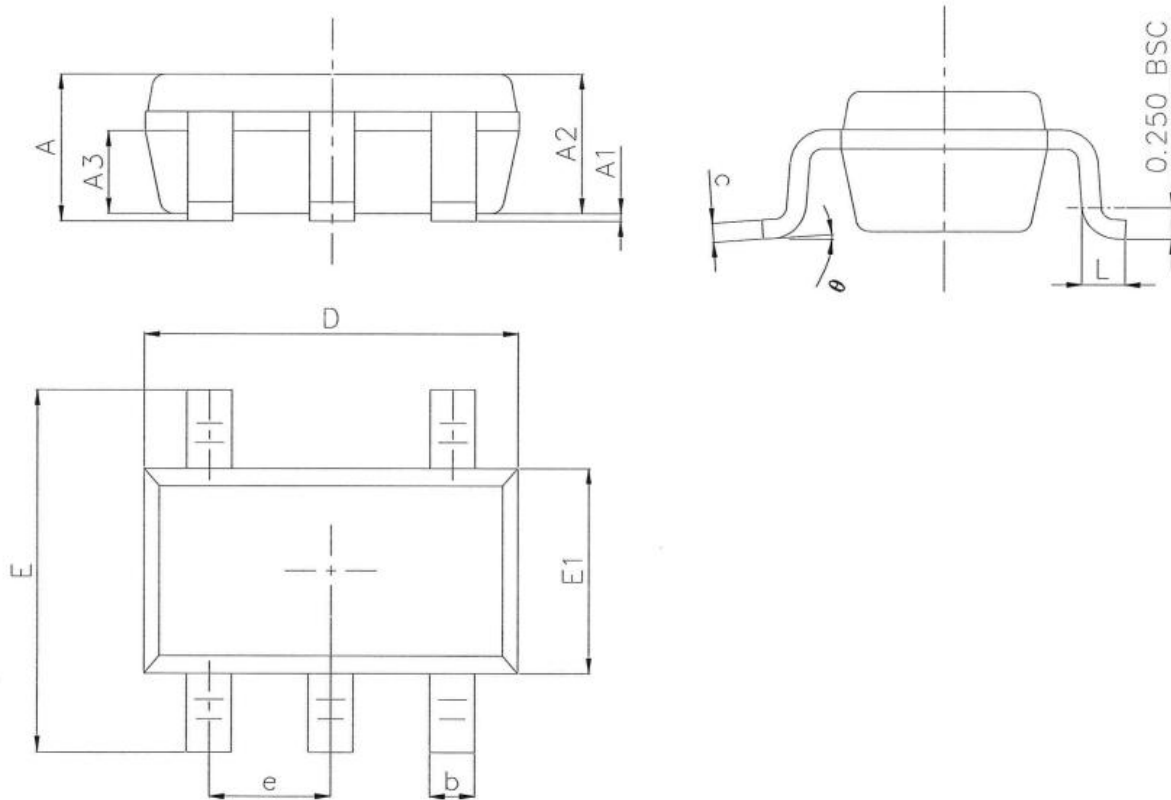
SOT23-5 Unit (mm)



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	1.050	1.150	1.250
A1	0.000	0.060	0.100
A2	1.000	1.100	1.200
A3	0.550	0.650	0.750
D	2.820	2.920	3.020
E1	1.510	1.610	1.700
E	2.650	2.800	2.950
b	0.300	0.400	0.500
e	0.950BSC		
θ	0°	4°	8°
L	0.300	0.420	0.570
c	0.100	0.152	0.200

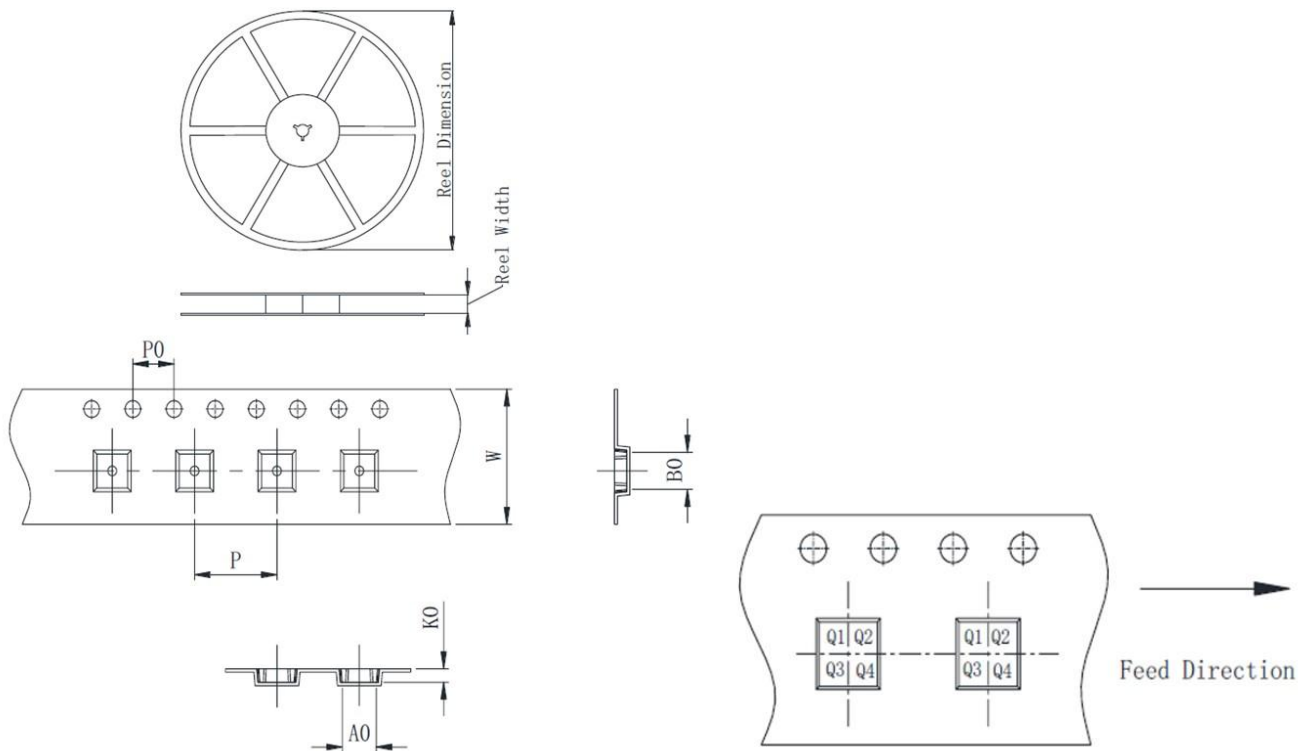
Package Outline Dimension-SC70-5

SC70-5 Unit (mm)



Symbol	Dimension in mm		
	Min.	Nom.	Max.
A	0.90	0.95	1.00
A1	0.00	0.05	0.10
A2		0.9	
A3		0.55	
D	2.00	2.10	2.20
E1	1.15	1.25	1.35
E	2.00	2.10	2.20
b	0.15	0.225	0.30
e	0.65BSC		
θ	0°	4°	8°
L	0.26	0.35	0.46
c	0.10	0.15	0.20

Packing information



Package type	Reel size	Reel dimension (±3.0mm)	Reel width (±1.0mm)	A0 (±0.1mm)	B0 (±0.1mm)	K0 (±0.1mm)	P (±0.1mm)	P0 (±0.1mm)	W (±0.3mm)	Pin1
SOT23-5	7'	180	8.4	3.23	3.17	1.32	4.0	4.0	8.0	Q3
SC70-5	7'	180	8.4	3.23	3.17	1.32	4.0	4.0	8.0	Q3

Version History

Version	Date	Changes
Rev.1.0	2025-12-03	Initial release

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