PJ74LVC2G07 Datasheet

Dual Buffer and Driver With Open-Drain Outputs In a SOT23-6 and SC70-6 Package

Version：Rev.1.0

Release Date：2025-11-20

MetaWells Co., Ltd.

www.MetaWells.com

General Description

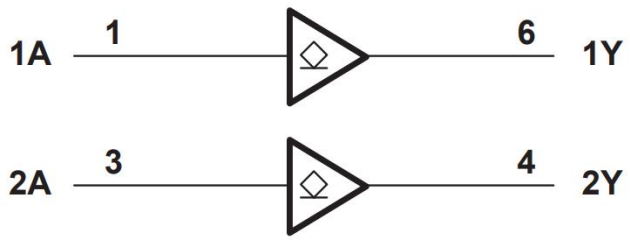
This dual buffer and driver is designed for 1.65 V to 5.5 V V_{CC} operation.

The output of PJ74LVC2G07 device is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

This device is fully specified for partial-power-down applications using Ioff. The Ioff circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The PJ74LVC2G07 is available in SOT23-6 and SC70-6 packages.

Simplified Schematic



Features

- Wide Supply Voltage Range : 1.65 V to 5.5 V
- Max. T_{PD} of 3.7 ns at V_{CC} = 3.3 V
- Low Power Consumption, 10 μA (Max. I_{CC})
- -24 mA Output Drive at V_{CC} = 3.3 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- Typical V_{OHV} (Output $_{VOH}$ Undershoot) > 2 V at V_{CC} = 3.3 V, T_A = 25°C
- Support Translation-Up and Down
- Ioff Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000 V Human-Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- Operating temperature Range : -40°C to 125°C

Applications

- Desktop or Notebook PCs
- Embedded PC
- Portable Media Players and Audio Dock
- Mobile Phones and Tablet : Enterprise
- Solid State Drive (SSD) : Enterprise
- TV : LCD/Digital and High-Definition (HDTV)
- Network Projector Front-Ends
- DLP Front Projection Systems
- GPS : Personal Navigation Devices

Ordering Information

Order number	Marking ID	Package	MSL	Description
PJ74LVC2G07S6	AA DNN	SOT23-6	Level-3	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel
PJ74LVC2G07C6	A5 W	SC70-6	Level-3	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel

Note:

(1) MetaWells can meet RoHS 2.0/REACH requirement. So most package types MetaWells offers only states halogen free, instead of lead free.

Marking Information

Marking ID	Package	Definition
AA DNN	SOT23-6	AA: Product code D: Date code NN: Serial number
A5 W	SC70-6	A5: Product code W: Week code

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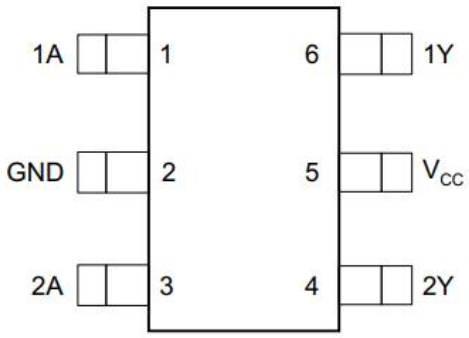
Pin Configuration



SOT23-6 and SC70-6 (Top View)

Functional Pin Description

Pin		Description
Name	**Num**	
1A	1	Data Input 1
GND	2	Ground
2A	3	Data Input 2
2Y	4	Data Output 2, Open-Drain Output
V_{CC}	5	Supply Power Pin
1Y	6	Data Output 1, Open-Drain Output

Function Table

H = HIGH voltage level; L = LOW voltage level; Hi-Z = High impedance

INPUTs	OUTPUT
A	**Y**
L	L
H	Hi-Z

Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

Parameter	Symbol	Value	Units
Supply Voltage	V_{CC}	-0.5 to 6.5	V
Input Voltage	V_I	-0.5 to 6.5	V
Voltage range applied to any output in the high-impedance or power-off state(2)	V_O	-0.5 to 6.5	V
Voltage range applied to any output in the high or low state(2)(3)	V_O	-0.5 to 6.5	V
Input clamp current, $V_I < 0$	I_{IK}	-50	mA
Output clamp current, $V_O < 0$	I_{OK}	-50	mA
Continuous output current	I_O	±50	mA
Storage temperature range	T_{STG}	-65 to 150	°C
ESD HBM, ANSI/ESDA/JEDEC JS-001(4)	ESD_{HBM}	±2000	V
ESD CDM, JESD22-C101(5)	ESD_{CDM}	±1000	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V_{CC} is provided in the Recommended Operating Conditions table.

(4) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(5) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Supply voltage	V_{CC}	Operating	1.65		5.5	V
		Data retention only	1.5			
Input voltage	V_I		0		5.5	V
Output voltage	V_O		0		5.5	V
High-level input voltage	V_{IH}	V_{CC} = 1.65 V to 1.95 V	0.65 x V_{CC}			V
		V_{CC} = 2.3 V to 2.7 V	1.7			
		V_{CC} = 3 V to 3.6 V	2			
		V_{CC} = 4.5 V to 5.5 V	0.7 x V_{CC}			
Low-level input voltage	V_{IL}	V_{CC} = 1.65 V to 1.95 V			0.35 x V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V			0.7	
		V_{CC} = 3 V to 3.6 V			0.8	
		V_{CC} = 4.5 V to 5.5 V			0.3 x V_{CC}	
Low-level output current	I_{OL}	V_{CC} = 1.65 V			4	mA
		V_{CC} = 2.3 V			8	
		V_{CC} = 3 V			16	
		V_{CC} = 3 V			24	
		V_{CC} = 4.5 V			32	
Input transition rise or fall rate	△T/△V	V_{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V			20	ns/V
		V_{CC} = 3.3 V ± 0.3 V			10	
		V_{CC} = 5.0 V ± 0.5 V			5	
Operating temperature	T_A		-40		125	°C

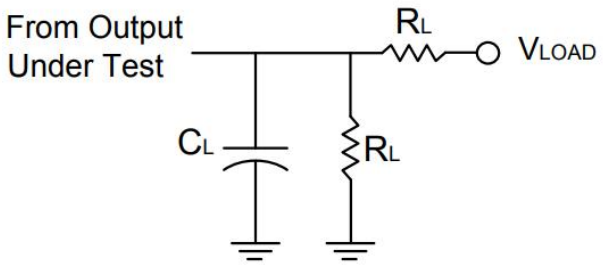
Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Low-level output voltage	V_{OL}	V_{CC} = 1.65 V to 5.5 V, I_{OL} = 100 μA			0.1	V
		V_{CC} = 1.65 V, I_{OL} = 4 mA			0.45	
		V_{CC} = 2.3 V, I_{OL} = 8 mA			0.3	
		V_{CC} = 3 V, I_{OL} = 16 mA			0.4	
		V_{CC} = 3 V, I_{OL} = 24 mA			0.55	
		V_{CC} = 4.5 V, I_{OL} = 32 mA			0.55	
Input leakage current	I_L	V_I = 5.5 V or GND, V_{CC} = 0 V to 5.5 V			±5	μA
Power off leakage current	I_{OFF}	V_I or GND, V_{CC} = 0 V to 5.5 V			±10	μA
Supply current	I_{CC}	V_I = V_{CC} or GND, I_{OUT} = 0, V_{CC} = 1.65 V to 5.5 V			10	μA
Additional supply current per input pin	$\triangle I_{CC}$	V_{CC} = 3 V to 5.5 V, one input at V_{CC} – 0.6 V, other input at V_{CC} or GND			500	μA

Switching Characteristics for -40°C to 85°C

Parameter	Symbol	Test Conditions		Min	Typ	Max	Units
Propagation delay from input (A) to output (Y)	T_{PD}	V_{CC} = 1.8 V ± 0.15 V, R_L = 1 KΩ	C_L = 30 pF	1.5		8.6	nS
		V_{CC} = 2.5 V ± 0.2 V R_L = 500 Ω		1		4.4	nS
		V_{CC} = 3.3 V ± 0.3 V R_L = 500 Ω	C_L = 50 pF	1		3.7	nS
		V_{CC} = 5 V ± 0.5 V R_L = 500 Ω		1		2.9	nS

Parameter Measurement Information



Test	Condition
t_{PLZ}	V_{LOAD}
t_{PZL}	V_{LOAD}

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≦2 ns	$V_{CC}/2$	2 x V_{CC}	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	V_{CC}	≦2 ns	$V_{CC}/2$	2 x V_{CC}	30 pF	500 Ω	0.15 V
3.3 V ± 0.3 V	3 V	≦2.5 ns	1.5 V	6 V	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≦2.5 ns	$V_{CC}/2$	2 x V_{CC}	50 pF	500 Ω	0.3 V

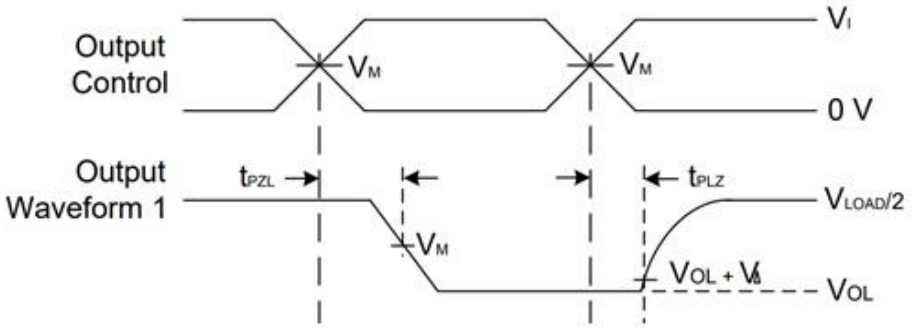


Figure 1. Voltage Waveform Enable and Disable Times
Low- and High-Level Enabling

Notes:

(1) C_L includes probe and jig capacitance.

(2) All pulses and supplied at pulse repetition rate ≤ 10 MHz.

(3) The Inputs are measured one at a time with one transition per measurement.

(4) For the open drain device t_{PLZ} and t_{PZL} are the same as t_{PD}.

(5) t_{PZL} is measured at V_M.

(6) t_{PLZ} is measured at $V_{OL} + V_\Delta$.

Application Information

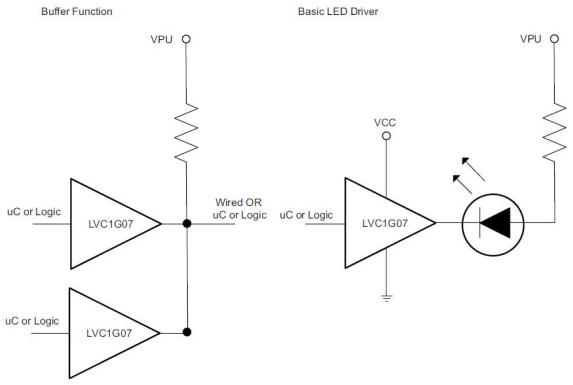


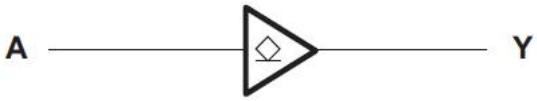
Figure 2. Typical Application Circuit

Basic Operation

The PJ74LVC2G07 is a high drive CMOS device that can be used to implement a high output drive buffer, such as an LED application. It can produce 32 mA of drive current at 4.5 V making it Ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to V_{CC}.

The open drain configuration means that the device cannot provide its own output drive current; instead, it relies on pull-up resistors to provide the "high" bus state. It can only drive the bus low. In the "Hi-Z" state, the PJ74LVC2G07 acts as an open circuit and allows the external pull-up to pull the bus high. Therefore, the pull-up voltage determines the output level and therefore the PJ74LVC2G07 can be used for up or down-translation. The device can sink 24 mA at 3 V while retaining an output voltage (V_{OL}) of 0.55 V or lower.

Function Block Diagram



Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

Recommended Input Conditions

1) Rise time and fall time specs. See ($\Delta t/\Delta V$) in the Recommended Operating Conditions table.
2) Specified high and low levels. See (V_{IH} and V_{IL}) in the Recommended Operating Conditions table.
3) Inputs are overvoltage tolerant allowing them to go as high as (V_I max) in the Recommended Operating Conditions table at any valid V_{CC}.

Recommended Output Conditions

1) Load currents should not exceed (I_O max) per output and should not exceed total current (continuous current through V_{CC} or GND) for the part. These limits are located in the Absolute Maximum Ratings table.
2) Outputs should not be pulled above V_{CC}.

Application Curves

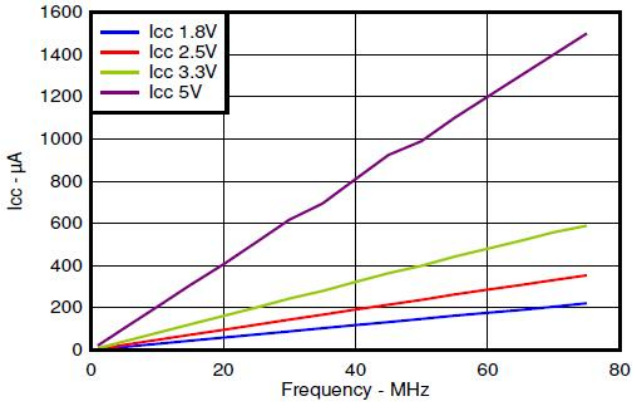


Figure 3. I_{CC} vs. Frequency

Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

Each V_{CC} pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 µF capacitor is recommended and if there are multiple V_{CC} pins then 0.01 µF or 0.022 µF capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 µF and 1 µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

Layout Considerations

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input buffer gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

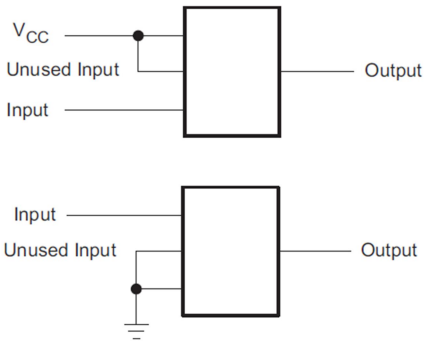
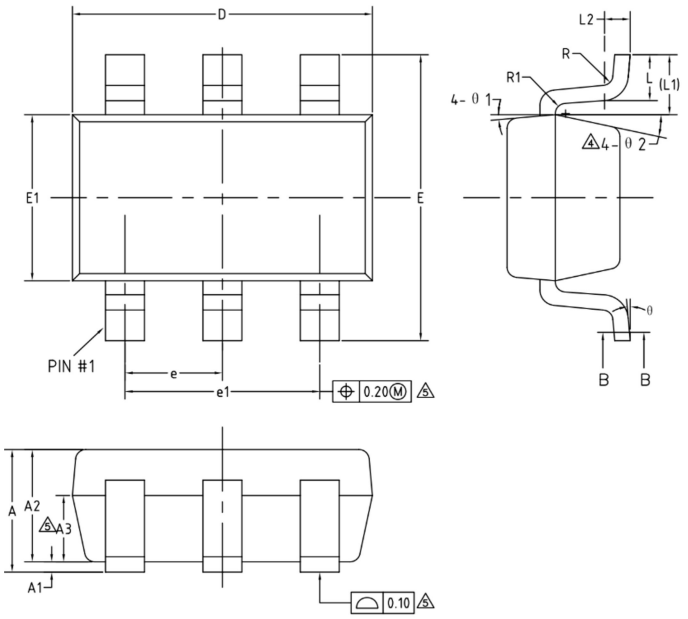


Figure 4. Layout Recommendation

Package Outline Dimensions - SOT23-6

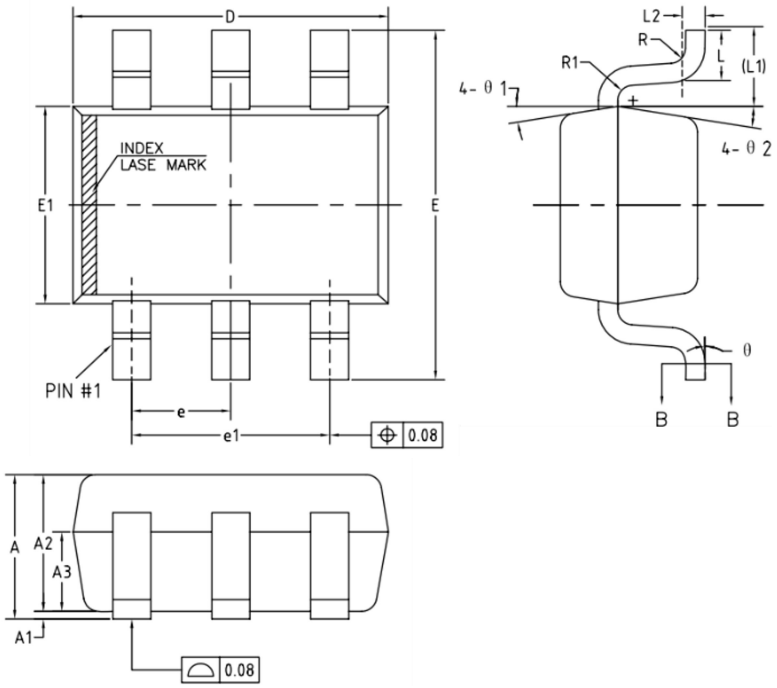
SOT23-6 Unit (mm)



Dimension in mm			
Symbol	**Min**	**Nom**	**Max**
A	-	-	1.25
A1	0	-	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	-	0.50
b1	0.36	0.38	0.45
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.35	0.45	0.60
L1	0.59 REF		
L2	0.25 BSC		
R	0.10	-	-
R1	0.10	-	0.25
θ	0°	-	8°
θ1	3°	5°	7°
θ2	6°	-	14°

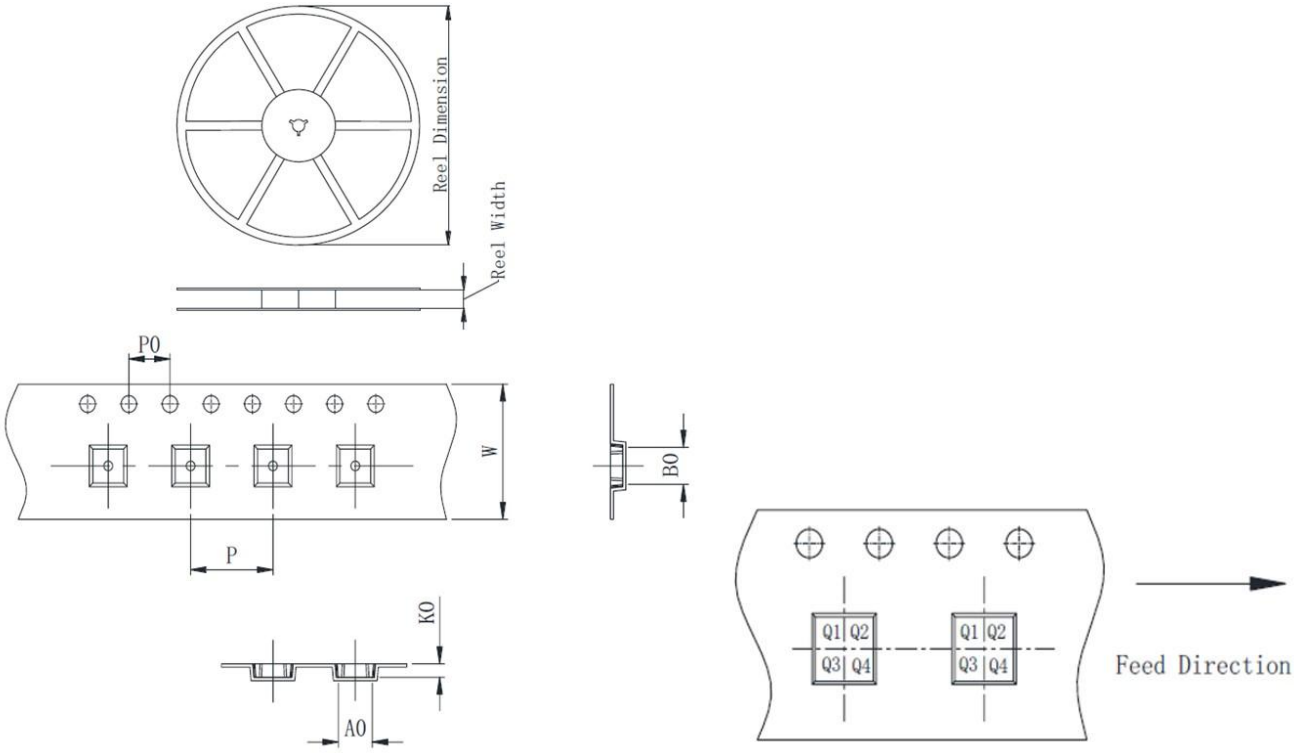
Package Outline Dimensions - SC70-6

SC70-6 Unit (mm)



Dimension in mm			
Symbol	**Min**	**Nom**	**Max**
A	0.85	-	1.05
A1	0	-	0.10
A2	0.80	0.90	1.00
A3	0.47	0.52	0.57
c	0.115	-	0.15
c1	0.115	0.13	0.14
D	2.02	2.07	2.12
E	2.20	2.30	2.40
E1	1.25	1.30	1.35
e	0.65 BSC		
e1	1.30 BSC		
L	0.28	0.33	0.38
L1	0.50 REF		
L2	0.15 BSC		
R	0.10	-	-
R1	0.10	-	0.25
θ	0°	-	8°
θ1	6°	9°	12°
θ2	6°	9°	12°

Packing information



Package type	Reel size	Reel dimension (±3.0mm)	Reel width (±1.0mm)	A0 (±0.1mm)	B0 (±0.1mm)	K0 (±0.1mm)	P (±0.1mm)	P0 (±0.1mm)	W (±0.3mm)	Pin1
SOT23-6	7'	180	8.4	3.23	3.17	1.32	4.0	4.0	8.0	Q3
SC70-6	7'	180	8.4	3.23	3.17	1.32	4.0	4.0	8.0	Q3

Version History

Version	Date	Changes
Rev.1.0	2025-11-20	Initial release

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