

# **PJ74LVC2G17 Datasheet**

## **Dual Schmitt-Trigger Buffer In a SOT23-6 and SC70-6 Package**

**Version: Rev.1.0**

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MetaWells Co., Ltd.

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## General Description

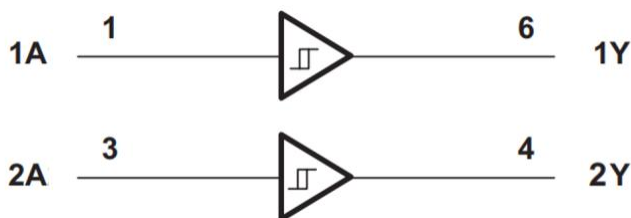
This dual Schmitt Trigger buffer is designed for 1.65 V to 5.5 V  $V_{CC}$  operation.

The PJ74LVC2G17 device contains two buffers and performs the Boolean function  $Y = A$ . The device functions as two independent buffers, but because of Schmitt action, it may have different input threshold levels for positive-going ( $V_{T+}$ ) and negative-going ( $V_{T-}$ ) signals.

This device is fully specified for partial power down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The PJ74LVC2G17 is available in SOT23-6 and SC70-6 packages.

## Simplified Schematic



## Features

- ◆ Wide Supply Voltage Range : 1.65 V to 5.5 V
- ◆ Max.  $T_{PD}$  of 5.4 ns at  $V_{CC} = 3.3$  V
- ◆ Low Power Consumption, 10  $\mu$ A ( $I_{CC}$  Max.)
- ◆  $\pm 24$  mA Output Drive at  $V_{CC} = 3.3$  V
- ◆ Schmitt-Trigger inputs provide hysteresis
- ◆ Typical  $V_{OLP}$  (Output Ground Bounce) < 0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- ◆ Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) > 2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- ◆  $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- ◆ Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ◆ ESD Protection Exceeds JESD 22
  - 2000 V Human-Body Model (A114-A)
  - 1000 V Charged-Device Model (C101)
- ◆ Operating temperature Range :-40°C to 125°C

## Applications

- ◆ Desktop or Notebook PCs
- ◆ Embedded PC
- ◆ Portable Media Players and Audio Dock
- ◆ Mobile Phones and Tablet : Enterprise
- ◆ Solid State Drive (SSD) : Enterprise
- ◆ TV : LCD/Digital and High-Definition (HDTV)
- ◆ Network Projector Front-Ends
- ◆ DLP Front Projection Systems
- ◆ GPS : Personal Navigation Devices

## Ordering Information

Order number	Marking ID	Package	MSL	Description
PJ74LVC2G17S6	A0 DNN	SOT23-6	Level-3	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel
PJ74LVC2G17C6	A4 W	SC70-6	Level-3	Halogen free RoHS compliant in T/R, 3,000 pcs/Reel

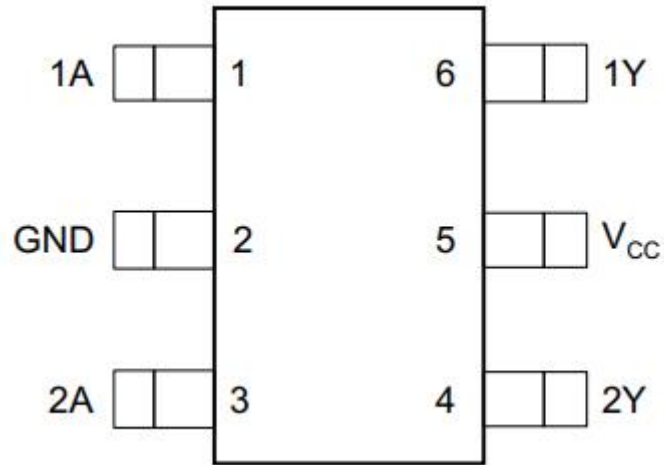
Note:

(1) MetaWells can meet RoHS 2.0/REACH requirement. So most package types MetaWells offers only states halogen free, instead of lead free.

## Marking Information

Marking ID	Package	Definition
A0 DNN	SOT23-6	A0: Product code   D: Date code   NN: Serial number
A4 W	SC70-6	A4: Product code   W: Week code

## Pin Configuration



SOT23-6 and SC70-6 (Top View)

## Functional Pin Description

Pin		Description
Name	Num	
1A	1	Data Input 1
GND	2	Ground
2A	3	Data Input 2
2Y	4	Data Output 2, Push-Pull
V <sub>cc</sub>	5	Supply Power Pin
1Y	6	Data Output 1, Push-Pull

## Function Table

*H = HIGH voltage level; L = LOW voltage level*

INPUTs	OUTPUT
A	Y
L	L
H	H

## Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

Parameter	Symbol	Value	Unit
Supply Voltage	V <sub>CC</sub>	-0.5 to 6.5	V
Input Voltage	V <sub>I</sub>	-0.5 to 6.5	V
Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	V <sub>O</sub>	-0.5 to 6.5	V
Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	V <sub>O</sub>	-0.5 to V <sub>CC</sub> +0.5	V
Input clamp current, V <sub>I</sub> < 0	I <sub>IK</sub>	-50	mA
Output clamp current, V <sub>O</sub> < 0	I <sub>OK</sub>	-50	mA
Continuous output current	I <sub>O</sub>	±50	mA
Storage temperature range	T <sub>STG</sub>	-65 to 150	°C
ESD HBM, ANSI/ESDA/JEDEC JS-001 <sup>(4)</sup>	ESD <sub>HBM</sub>	±2000	V
ESD CDM, JESD22-C101 <sup>(5)</sup>	ESD <sub>CDM</sub>	±1000	V

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The value of V<sub>CC</sub> is provided in the Recommended Operating Conditions table.

(4) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(5) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## Recommended Operating Conditions

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply voltage	V <sub>CC</sub>	Operating	1.65		5.5	V
Input voltage	V <sub>I</sub>		0		5.5	V
Output voltage	V <sub>O</sub>		0		V <sub>CC</sub>	V
High-level output current	I <sub>OH</sub>	V <sub>CC</sub> = 1.65 V			-4	mA
		V <sub>CC</sub> = 2.3 V			-8	
		V <sub>CC</sub> = 3 V			-16	
		V <sub>CC</sub> = 3 V			-24	
		V <sub>CC</sub> = 4.5 V			-32	
Low-level output current	I <sub>OL</sub>	V <sub>CC</sub> = 1.65 V			4	mA
		V <sub>CC</sub> = 2.3 V			8	
		V <sub>CC</sub> = 3 V			16	
		V <sub>CC</sub> = 3 V			24	
		V <sub>CC</sub> = 4.5 V			32	
Operating temperature	T <sub>A</sub>		-40		125	°C

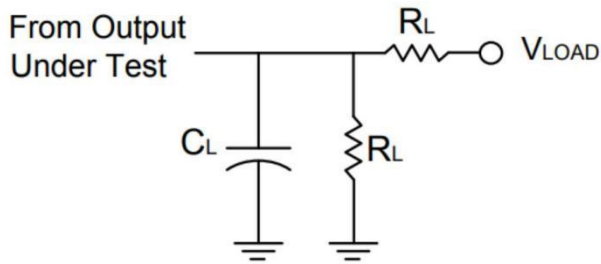
## Electrical Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Positive-going input threshold voltage	$V_{T+}$	$V_{CC} = 1.65\text{ V}$	0.7		1.4	V
		$V_{CC} = 2.3\text{ V}$	1.0		1.7	
		$V_{CC} = 3\text{ V}$	1.3		2.0	
		$V_{CC} = 4.5\text{ V}$	1.9		3.1	
		$V_{CC} = 5.5\text{ V}$	2.2		3.7	
Negative-going input threshold voltage	$V_{T-}$	$V_{CC} = 1.65\text{ V}$	0.3		0.7	V
		$V_{CC} = 2.3\text{ V}$	0.4		1.0	
		$V_{CC} = 3\text{ V}$	0.8		1.3	
		$V_{CC} = 4.5\text{ V}$	1.1		2.0	
		$V_{CC} = 5.5\text{ V}$	1.4		2.5	
Hysteresis Voltage	$\Delta V_T$	$V_{CC} = 1.65\text{ V}$	0.3		0.8	V
		$V_{CC} = 2.3\text{ V}$	0.4		0.9	
		$V_{CC} = 3\text{ V}$	0.4		1.1	
		$V_{CC} = 4.5\text{ V}$	0.6		1.3	
		$V_{CC} = 5.5\text{ V}$	0.7		1.4	
High-level output voltage	$V_{OH}$	$V_{CC} = 1.65\text{ V to } 5.5\text{ V}, I_{OH} = -100\text{ }\mu\text{A}$	$V_{CC}-0.1$			V
		$V_{CC} = 1.65\text{ V}, I_{OH} = -4\text{ mA}$	1.2			
		$V_{CC} = 2.3\text{ V}, I_{OH} = -8\text{ mA}$	1.9			
		$V_{CC} = 3\text{ V}, I_{OH} = -16\text{ mA}$	2.4			
		$V_{CC} = 3\text{ V}, I_{OH} = -24\text{ mA}$	2.3			
		$V_{CC} = 4.5\text{ V}, I_{OH} = -32\text{ mA}$	3.8			
Low-level output voltage	$V_{OL}$	$V_{CC} = 1.65\text{ V to } 5.5\text{ V}, I_{OL} = 100\text{ }\mu\text{A}$			0.1	V
		$V_{CC} = 1.65\text{ V}, I_{OL} = 4\text{ mA}$			0.45	
		$V_{CC} = 2.3\text{ V}, I_{OL} = 8\text{ mA}$			0.3	
		$V_{CC} = 3\text{ V}, I_{OL} = 16\text{ mA}$			0.4	
		$V_{CC} = 3\text{ V}, I_{OL} = 24\text{ mA}$			0.55	
		$V_{CC} = 4.5\text{ V}, I_{OL} = 32\text{ mA}$			0.55	

## Switching Characteristics for $-40^{\circ}\text{C}$ to $85^{\circ}\text{C}$

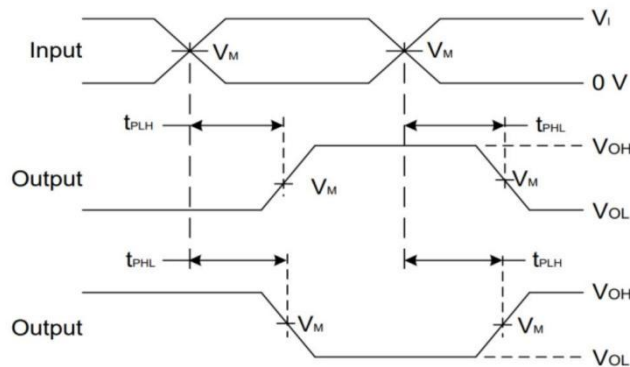
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation delay from input (A) to output (Y)	$T_{PD}$	$V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}, R_L = 1\text{ K}\Omega$	3.9		9.3	nS
		$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}, R_L = 500\text{ }\Omega$				
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}, R_L = 500\text{ }\Omega$	2.2		5.4	nS
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}, R_L = 500\text{ }\Omega$				

## Parameter Measurement Information



Test	Condition
$t_{PLZ}$	$V_{LOAD}$
$t_{PZL}$	$V_{LOAD}$

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_i$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V

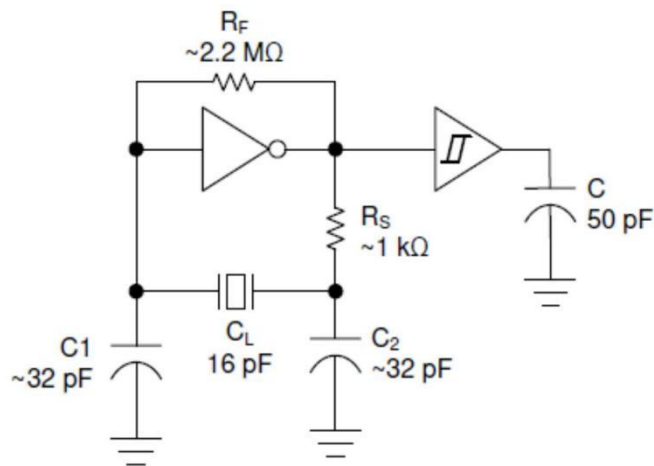


**Figure 1. Voltage Waveform Propagation Delay Times**  
**Inverting and Non Inverting Outputs**

Notes:

- (1)  $C_L$  includes probe and jig capacitance.
- (2) All pulses and supplied at pulse repetition rate  $\leq 10\text{ MHz}$ .
- (3) The Inputs are measured separately one transition per measurement.

## Operation Information



**Figure 2. Typical Application Circuit**

### Overview

The PJ74LVC2G17 is a high drive CMOS device that can be used for a multitude of buffer type functions where the input is slow or noisy. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5 V tolerant allowing it to translate down to  $V_{CC}$ .

### Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

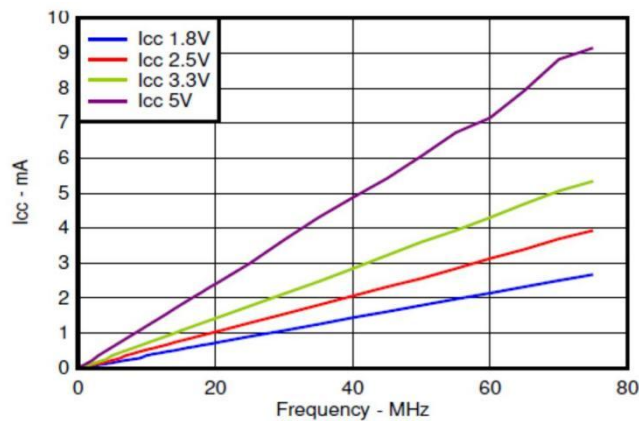
### Recommended Input Conditions

- 1) Rise time and fall time specs. See  $(\Delta t/\Delta V)$  in the Recommended Operating Conditions table.
- 2) Specified high and low levels. See  $(V_{IH}$  and  $V_{IL})$  in the Recommended Operating Conditions table.
- 3) Inputs are overvoltage tolerant allowing them to go as high as  $(V_I \text{ max})$  in the Recommended Operating Conditions table at any valid  $V_{CC}$ .

### Recommended Output Conditions

- 1) Load currents should not exceed  $(I_O \text{ max})$  per output and should not exceed total current (continuous current through  $V_{CC}$  or GND) for the part. These limits are located in the Absolute Maximum Ratings table.
- 2) Outputs should not be pulled above  $V_{CC}$ .

## Application Curves



**Figure 3. I<sub>cc</sub> vs. Frequency**

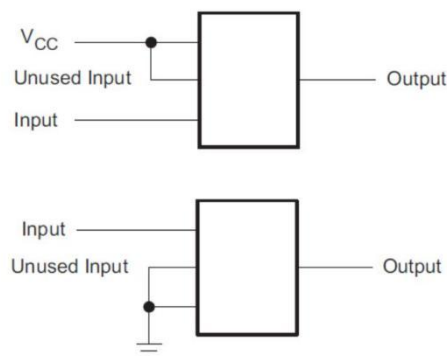
## Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the Recommended Operating Conditions table.

Each V<sub>cc</sub> pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1  $\mu$ F capacitor is recommended and if there are multiple V<sub>cc</sub> pins then 0.01  $\mu$ F or 0.022  $\mu$ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1  $\mu$ F and 1  $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## Layout Considerations

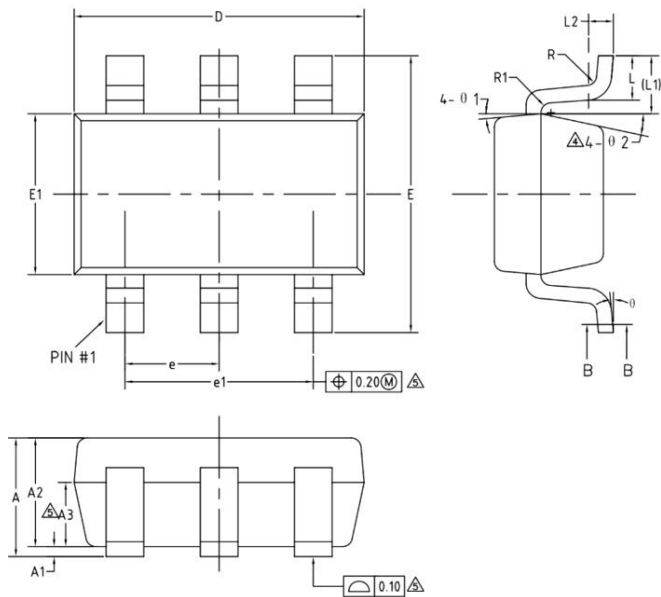
When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input buffer gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V<sub>CC</sub> whichever make more sense or is more convenient.



**Figure 4. Layout Recommendation**

## Package Outline Dimensions - SOT23-6

SOT23-6 Unit (mm)

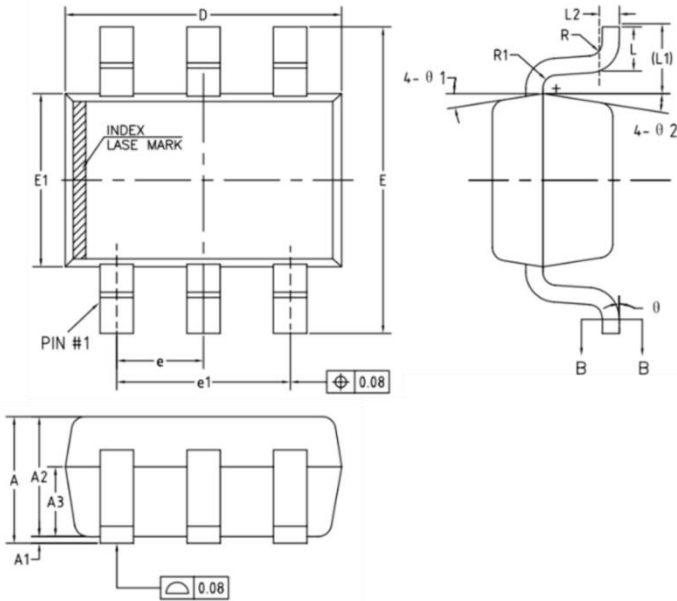


**Common Dimensions (Units of measure = Millimeter)**

Symbol	Min	Nom	Max
A	-	-	1.25
A1	0	-	0.15
A2	1.00	1.10	1.20
A3	0.60	0.65	0.70
b	0.36	-	0.50
b1	0.36	0.38	0.45
c	0.14	-	0.20
c1	0.14	0.15	0.16
D	2.826	2.926	3.026
E	2.60	2.80	3.00
E1	1.526	1.626	1.726
e	0.90	0.95	1.00
e1	1.80	1.90	2.00
L	0.35	0.45	0.60
L1	0.59 REF		
L2	0.25 BSC		
R	0.10	-	-
R1	0.10	-	0.25
$\theta$	0°	-	8°
$\theta1$	3°	5°	7°
$\theta2$	6°	-	14°

## Package Outline Dimensions - SC70-6

SC70-6 Unit (mm)



Common Dimensions (Units of measure = Millimeter)			
Symbol	Min	Nom	Max
A	0.85	-	1.05
A1	0	-	0.10
A2	0.80	0.90	1.00
A3	0.47	0.52	0.57
c	0.115	-	0.15
c1	0.115	0.13	0.14
D	2.02	2.07	2.12
E	2.20	2.30	2.40
E1	1.25	1.30	1.35
e	0.65 BSC		
e1	1.30 BSC		
L	0.28	0.33	0.38
L1	0.50 REF		
L2	0.15 BSC		
R	0.10	-	-
R1	0.10	-	0.25
θ	0°	-	8°
θ1	6°	9°	12°
θ2	6°	9°	12°

## Version History

Version	Date	Changes
Rev.1.0	2025-09-26	Initial release

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