

# **PJ72617 Datasheet**

## **Level Translating FM+ I<sup>2</sup>C-bus Repeater**

**Version: Rev.1.0**

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PANJIT International Inc.

[www.panjit.com.tw](http://www.panjit.com.tw)

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## 1 General Description

The PJ72617 is a CMOS integrated circuit that provides level shifting between low voltage (0.8V to 5.5V) and higher voltage (2.2V to 5.5V) Fast-mode Plus (FM+) I<sup>2</sup>C-bus or SMBus applications. While retaining all the operating modes and features I<sup>2</sup>C-bus system during the level shifts, it also permits extension of the I<sup>2</sup>C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus enabling two buses of 540 pf at 1 MHz or up to 4000 pf at lower speeds. Using the PJ72617 enables the system designer to isolate two halves of a bus for both voltage and capacitance. The SDA and SCL pins are overvoltage tolerant and are high-impedance when the PJ72617 is unpowered.

Available Package: MSOP-8, SOP-8

## 2 Features

- ◆ 2 channel, bidirectional translator for SDA and SCL in mixed-mode I<sup>2</sup>C applications
- ◆ I<sup>2</sup>C and SMBus compatible
- ◆ Voltage level translation from 0.8V to 5.5V and from 2.2V to 5.5V
- ◆ Port A operating supply voltage range of 0.8V to 5.5V with normal levels
- ◆ Port B operating supply voltage range of 2.2V to 5.5V with static offset level
- ◆ 5V tolerant I<sup>2</sup>C-bus and enable pins
- ◆ 0Hz to 1000kHz clock frequency (the maximum system operating frequency may be less than 1000kHz because of the delays added by the repeater)
- ◆ Active HIGH repeater enable input referenced to V<sub>CCB</sub>
- ◆ Open-drain input/outputs
- ◆ Latching free operation
- ◆ Supports arbitration and clock stretching across the repeater
- ◆ Accommodates Standard-mode, Fast-mode and Fast-mode Plus I<sup>2</sup>C-bus devices, SMBus (standard and high power mode), PMBus and multiple masters
- ◆ Powered-off high-impedance I<sup>2</sup>C-bus pins

## 3 Applications

- ◆ Server
- ◆ Routers (Telecom Switching Equipment)
- ◆ Industrial Equipment
- ◆ Products with many I<sup>2</sup>C slaves and/or long PCB traces

## 4 Ordering Information

### 4.1 Ordering Information

Order number	Marking ID	Package	MSL	Description
PJ72617M	72617 YMDNN	MSOP-8	Level-3	Halogen free RoHS compliant in T/R,3,000 pcs/Reel
PJ72617P	72617 YMDNN	SOP-8	Level-3	Halogen free RoHS compliant in T/R,4,000 pcs/Reel

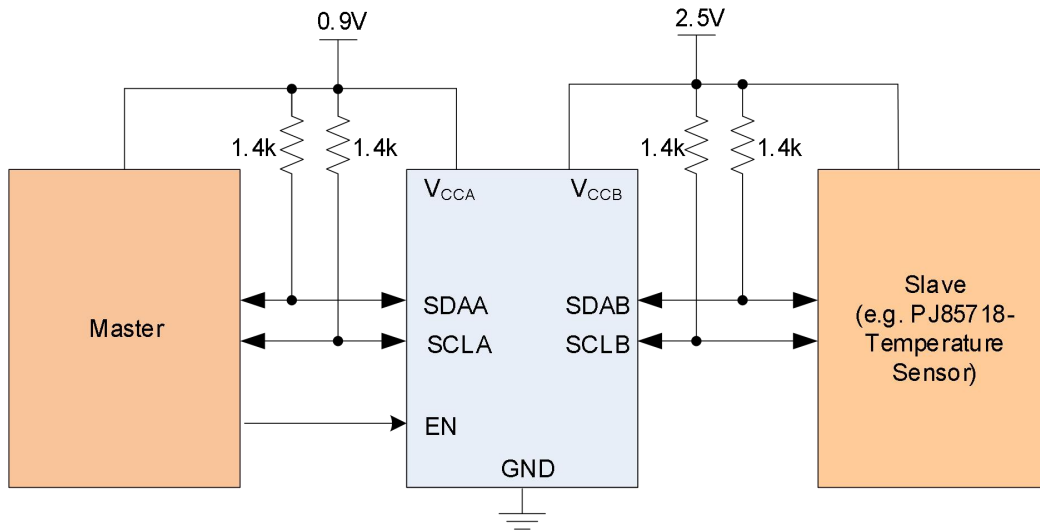
Note:

(1) Panjit can meet RoHS 2.0/REACH requirement. So most package types Panjit offers only states halogen free, instead of lead free.

### 4.2 Marking Information

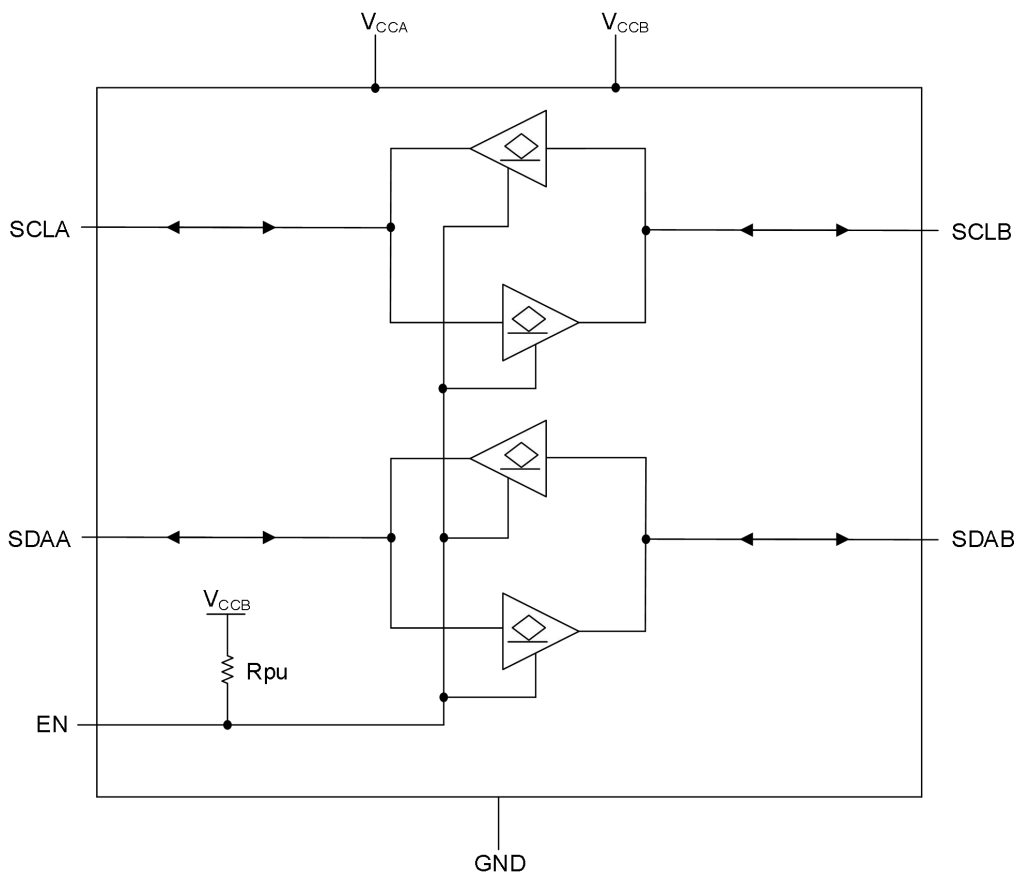
Marking	Package	Definition
72617 YMDNN	MSOP-8	72617:Product code YMDNN : Y : Year code M : Month code D : Day code ,NN: Serial Number
72617 YMDNN	SOP-8	72617:Product code YMDNN : Y : Year code M : Month code D : Day code ,NN: Serial Number

## 5 Typical Application



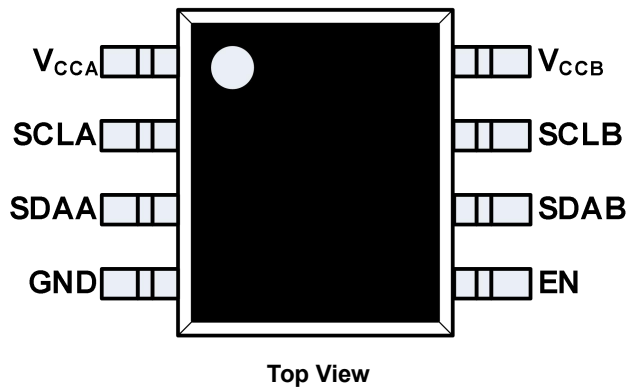
**Figure 1 Typical Application Circuit**

## 6 Function Block



**Figure 2 Function Block**

## 7 Pin Configuration



## 8 Pin Description

PIN Name	Pin No	Description
V <sub>CCA</sub>	1	A-side supply voltage (0.8V to 5.5V); Power
SCLA	2	I <sup>2</sup> C SCL line, A side. Connect to V <sub>CCA</sub> through a pull-up resistor; I/O
SDAA	3	I <sup>2</sup> C SDA line, A side. Connect to V <sub>CCA</sub> through a pull-up resistor; I/O
GND	4	Ground; GND
EN	5	Active-high repeater enable input with an internal pull-up to V <sub>CCB</sub> ; Input
SDAB	6	I <sup>2</sup> C SDA line, B side. Connect to V <sub>CCB</sub> through a pull-up resistor; I/O
SCLB	7	I <sup>2</sup> C SCL line, B side. Connect to V <sub>CCB</sub> through a pull-up resistor; I/O
V <sub>CCB</sub>	8	B-side and device supply voltage (2.2V to 5.5V); Power

## 9 Specification

### 9.1 Absolute Maximum Ratings<sup>1</sup>

Parameter	Symbol	Value	Unit
Supply Voltage Port A	$V_{CCA}$	-0.5 to 7	V
Supply Voltage Port B	$V_{CCB}$	-0.5 to 7	V
Voltage on port A, port B and EN	$V_{I/O}$	-0.5 to 7	V
Input/output current	$I_{I/O}$	50	mA
EN, $V_{CCA}$ , $V_{CCB}$ , GND input current	$I_i$	50	mA
Storage Temperature Range	$T_{stg}$	-65 to 150	°C
ESD HBM	$ESD_{HBM}$	±5500	V
ESD CDM	$ESD_{CDM}$	±1000	V

(1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at the "Absolute Maximum Ratings" conditions or any other conditions beyond those indicated under "Recommended Operating Conditions" is not recommended. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 9.2 Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply voltage port A	$V_{CCA}$	0.8 to 5.5	V
Supply voltage port B	$V_{CCB}$	2.2 to 5.5	V
Operating free-air temperature	$T_A$	-40 to 85	°C

### 9.3 Electrical Characteristics

$V_{CCB} = 2.2V$  to  $5.5V$ ,  $GND = 0V$ ,  $T = -40^{\circ}C$  to  $85^{\circ}C$  (unless otherwise noted). All limits are 100% tested at  $T_A = 25^{\circ}C$ .

Parameter	Symbol	Test Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>Supplies</b>						
Supply voltage port A	$V_{CCA}$		0.8		5.5 <sup>1</sup>	V
Supply voltage port B	$V_{CCB}$		2.2		5.5	V
Supply current port A	$I_{CCA}$	$V_{CCA} = 0.95V$			8	$\mu A$
		$V_{CCA} = 5.5V$			50	$\mu A$
Port B HIGH-level supply current	$I_{CCHB}$	$V_{CCB} = 5.5V$ ; $SDAn = SCLn = V_{CCn}$		1.5	2.5	mA
Port B LOW-level supply current	$I_{CCLB}$	$V_{CCB} = 5.5V$ ; one SDA and one SCL = GND; other SDA and SCL open (with pull-up resistors)		1.7	2.9	mA
<b>Input and output SDAB and SCLB</b>						
High-level input voltage	$V_{IH}$		$0.7 \cdot V_{CCB}$		5.5	V
Low-level input voltage	$V_{IL}$		-0.5		0.4	V
Input clamp voltage	$V_{IK}$	$I_I = -18 \text{ mA}$ ;	-1.2		-0.3	V
Low-level output voltage	$V_{OL}$	$I_{OL} = 150\mu A$ at $V_{CCB} = 2.2V$	$0.47^2$			V
		$I_{OL} = 13\text{mA}$ at $V_{CCB} = 2.2V$		0.54	0.63	V
Input leakage current	$I_{LI}$	$V_I = 5.5V$	-1		+1	$\mu A$
Difference between LOW-level output and LOW-level input voltage	$V_{OL} - V_{IL}$	$V_{OL}$ at $I_{OL} = 1 \text{ mA}$ ; guaranteed by design	60	90	160	mV
<b>Input and output SDAA and SCLA</b>						
Low-level input voltage	$V_{IL}^3$		-0.5		$0.25 \cdot V_{CCA}$	V
High-level input voltage	$V_{IH}$		$0.7 \cdot V_{CCA}$		5.5	V
Input clamp voltage	$V_{IK}$	$I_I = -18 \text{ mA}$ ;	-1.2		-0.3	V
Low-level output voltage	$V_{OL}$	$I_{OL} = 13\text{mA}$ at $V_{CCB} = 2.2V$		0.1	0.2	V
Input leakage current	$I_{LI}$	$V_I = 5.5V$	-1		+1	$\mu A$
<b>Enable</b>						
LOW-level input voltage	$V_{IL}$		-0.5		$0.3 \cdot V_{CCB}$	V
HIGH-level input voltage	$V_{IH}$		$0.7 \cdot V_{CCB}$		5.5	V
LOW-level input current on pin EN	$I_{IL(EN)}$	$V_I = 0.2V$ , EN; $V_{CCB} = 2.2V$	-18	-7	-4	$\mu A$
Input leakage current	$I_{LI}$	$V_I = V_{CCB}$	-1		+1	$\mu A$

**Notes**

- (1)  $V_{CCA}$  may be as high as 5.5 V for overvoltage tolerance but  $0.4V_{CCA} + 0.8V \leq V_{CCB}$  for the channels to be enabled and functional normally.
- (2) Pull-up should result in  $I_{OL} \geq 150\mu A$ .
- (3)  $V_{IL}$  for port A with envelope noise must be below  $0.3V_{CCA}$  for stable performance.

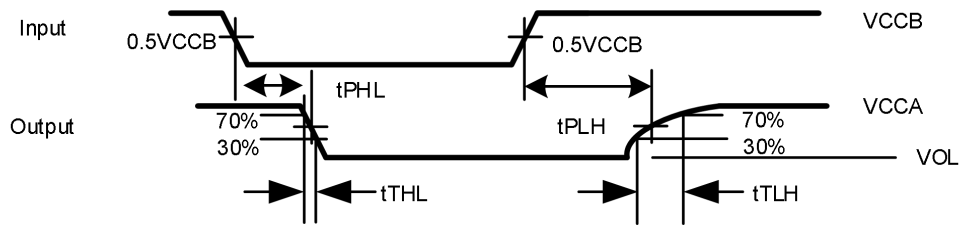
## 9.4 Interface Timing Requirements

Parameter	Symbol	Test Conditions	Min	Typ <sup>1</sup>	Max	Unit
LOW to HIGH propagation delay	$t_{PLH}$	port A to port B;	40	60	150	ns
		port B to port A;	-42	-65	-155	ns
LOW to HIGH propagation delay 2	$t_{PLH2}$	port B to port A; <sup>2</sup>	67	94	160	ns
HIGH to LOW propagation delay	$t_{PHL}$	port A to port B;	63	80	173	ns
		port B to port A;	46	76	200	ns
LOW to HIGH output transition time	$t_{TLH}$ <sup>3</sup>	A side ;From 30% to 70%		60		ns
		B side ;From 30% to 70%				
Falling slew rate	$SR_f$	port A; 0.7V <sub>CCA</sub> to 0.3V <sub>CCA</sub>	0.007	0.037	0.09	V/ns
		port B; 0.7V <sub>CCB</sub> to 0.3V <sub>CCB</sub>	0.029	0.056	0.12	V/ns
Enable time	$t_{en}$ <sup>4</sup>	quiescent - 0.3 V; EN HIGH to enable;			100	ns
Disable time	$t_{dis}$ <sup>4</sup>	quiescent + 0.3 V; EN LOW to disable;			100	ns

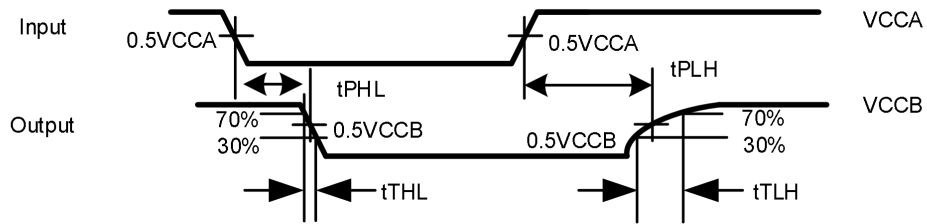
### Notes

- (1) typical values were measured with V<sub>CCA</sub> = 0.95V, V<sub>CCB</sub> = 2.5V at Tamb = 25°C, unless otherwise noted.
- (2) The  $t_{PLH2}$  delay data from port B to port A is measured at 0.45V on port B to 0.5V<sub>CCA</sub> on port A.
- (3) The  $t_{TLH}$  of the bus is determined by the pull-up resistance (1.35kΩ) and the total capacitance (50pf).
- (4) The enable pin, EN, should only change state when the global bus and the repeater port are in an idle state.

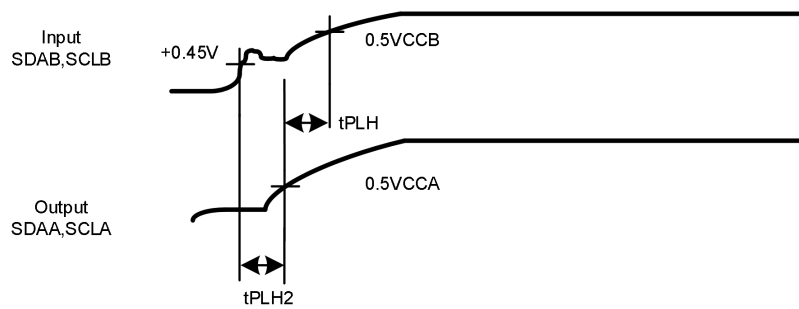
**9.4.1 AC waveforms**



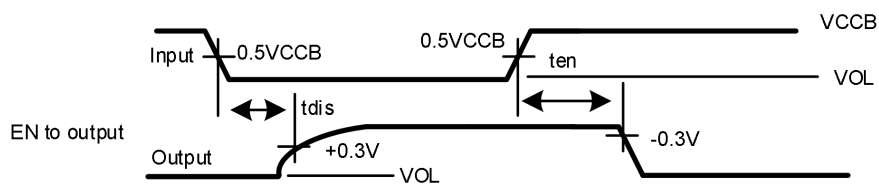
**Figure 3 Propagation Delay And Transition Times(B to A)**



**Figure 4 Propagation Delay And Transition Times(A to B)**



**Figure 5 Propagation delays**



**Figure 6 Enable and disable times**

### 9.4.2 Test information

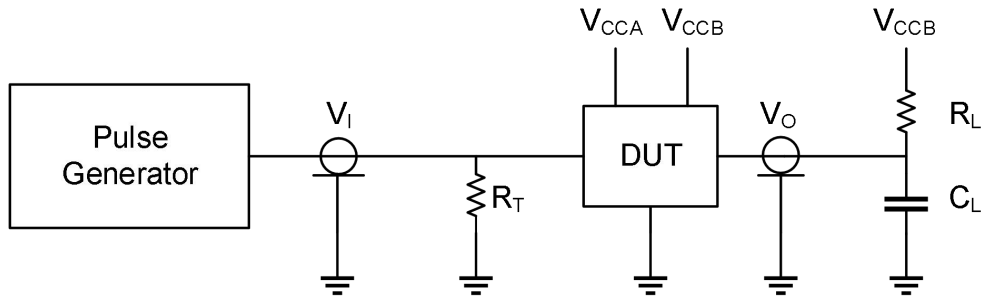


Figure 7 Test circuit for open-drain outputs

#### Notes

- (1)  $R_L$  = load resistor; 1.35 k $\Omega$  on port A and port B.
- (2)  $C_L$  = load capacitance includes jig and probe capacitance; 50 pf.
- (3)  $R_T$  = termination resistance should be equal to  $Z_o$  of pulse generators.

### 9.5 Typical Characteristics

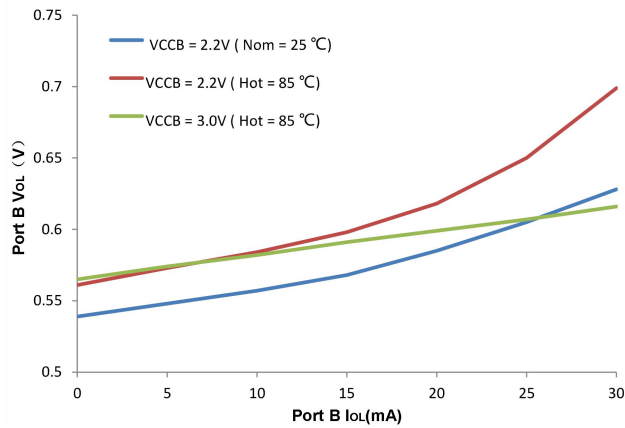


Figure 8 Port B  $V_{OL}$  versus  $I_{OL}$

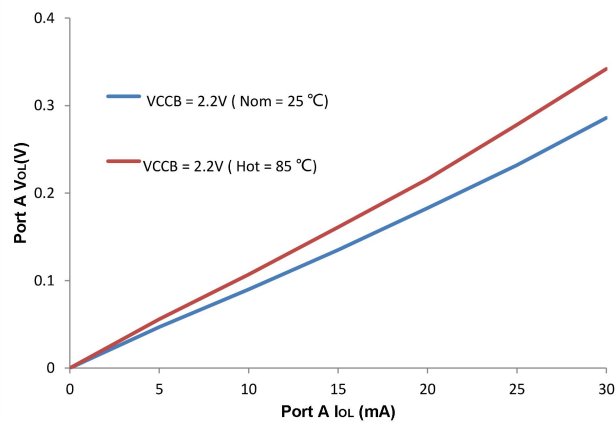


Figure 9 Port A  $V_{OL}$  versus  $I_{OL}$

## 10 Detailed Descriptions

### 10.1 Overview

The PJ72617 enables I<sup>2</sup>C-bus or SMBus translation down to  $V_{CCA}$  as low as 0.8V without degradation of system performance. The PJ72617 contains two bidirectional open-drain buffers specifically designed to support up-translation/down-translation between the low voltage (as low as 0.8V) and 2.5V, 3.3V or 5V I<sup>2</sup>C-bus or SMBus. All inputs and I/Os are overvoltage tolerant to 5.5V even when the device is unpowered ( $V_{CCB}$  and/or  $V_{CCA} = 0V$ ). The PJ72617 includes a power-up circuit that keeps the output drivers turned off until  $V_{CCB}$  is above 2.2V and until after the internal reference circuits have settled 400 $\mu$ s, and the  $V_{CCA}$  is above 0.8V.  $V_{CCB}$  and  $V_{CCA}$  can be applied in any sequence at power-up. After power-up and with the enable (EN) HIGH, a LOW level on port A (below 0.3 $V_{CCA}$ ) turns the corresponding port B driver (either SDA or SCL) on and drives port B down to about 0.55V. When port A rises above 0.3 $V_{CCA}$ , the port B pull-down driver is turned off and the external pull-up resistor pulls the pin HIGH. When port B falls first and goes below 0.4V, the port A driver is turned on and port A pulls down to 0V. The port A pull-down is not enabled unless the port B voltage goes below 0.4V. If the port B low voltage goes below 0.4V, the port B pull-down driver is enabled and port B will only be able to rise to 0.55V until port A rises above 0.3 $V_{CCA}$ , then port B will continue to rise being pulled up by the external pull-up resistor. The  $V_{CCA}$  is only used to provide the 0.35 $V_{CCA}$  reference to the port A input comparators and for the power good detect circuit. The PJ72617 includes a  $V_{CCA}$  overvoltage disable that turns the channel off if  $0.4V_{CCA} + 0.8V > V_{CCB}$ . The PJ72617 logic and all I/Os are powered by the  $V_{CCB}$  pin.

### 10.2 Enable

The EN pin is active HIGH with thresholds referenced to  $V_{CCB}$  and an internal pull-up to  $V_{CCB}$  that maintains the device active unless the user selects to disable the repeater to isolate a badly behaved slave on power-up until after the system power-up reset. It should never change state during an I<sup>2</sup>C-bus operation because disabling during a bus operation will hang the bus and enabling part way through a bus cycle could confuse the I<sup>2</sup>C-bus parts being enabled. The enable does not switch the internal reference circuits so the ~400 $\mu$ s delay is only seen when  $V_{CCB}$  comes up.

The enable pin should only change state when the global bus and the repeater port are in an idle state to prevent system failures.

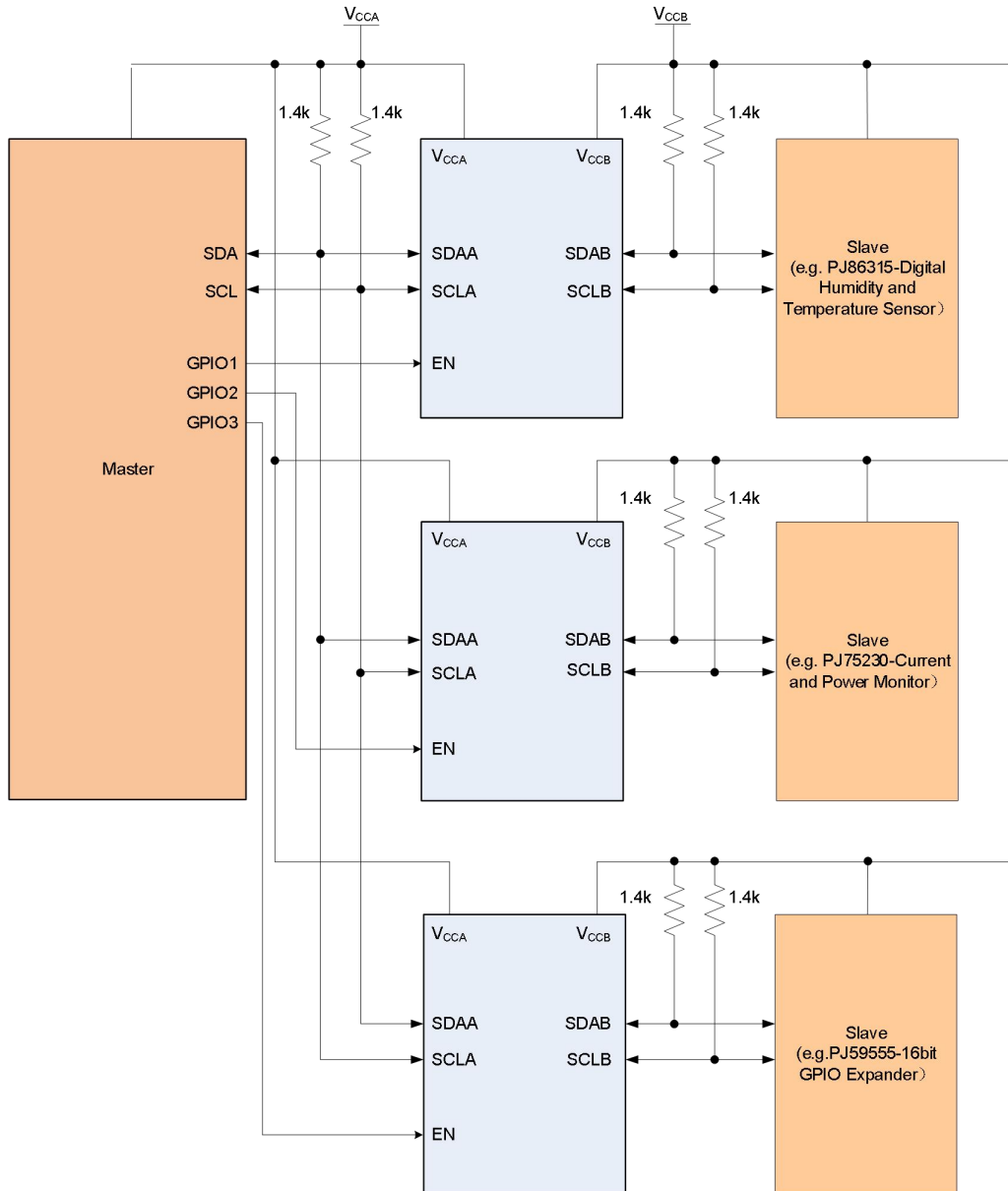
### 10.3 I<sup>2</sup>C-bus systems

As with the standard I<sup>2</sup>C-bus system, pull-up resistors are required to provide the logic HIGH levels on the buffered bus (standard open-collector configuration of the I<sup>2</sup>C-bus). The size of these pull-up resistors depends on the system, but each side of the repeater must have a pull-up resistor. This part designed to work with Standard mode, Fast-mode and Fast-mode Plus I<sup>2</sup>C-bus devices in addition to SMBus devices. Standard mode and Fast-mode I<sup>2</sup>C-bus devices only specify 3mA output drive; this limits the termination current to 3mA in a generic I<sup>2</sup>C-bus system where Standard-mode devices, Fast-mode devices and multiple masters are possible. When only Fast-mode Plus devices are used with 30mA at 5V drive strength, then lower value pull-up resistors can be used. The B-side RC should not be less than 67.5ns because shorter RCs increase the turnaround bounce when the B-side transitions from being externally driven to pulled down by its offset buffer.

## 10.4 Application Implementation

### 10.4.1 Star Application

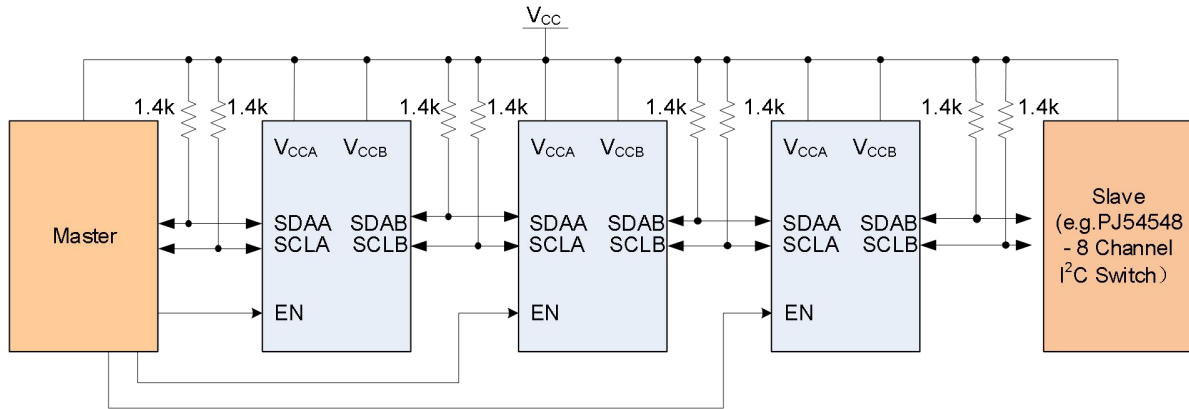
Multiple PJ72617 A sides can be connected in a star configuration, allowing all nodes to communicate with each other.



**Figure 10 Star Application**

### 10.4.2 Series Application

Multiple PJ72617s can be connected in series as long as the A side is connected to the B side. I<sup>2</sup>C bus slave devices can be connected to any of the bus segments. The number of devices that can be connected in series is limited by repeater delay/time-of-flight considerations on the maximum bus speed requirements.



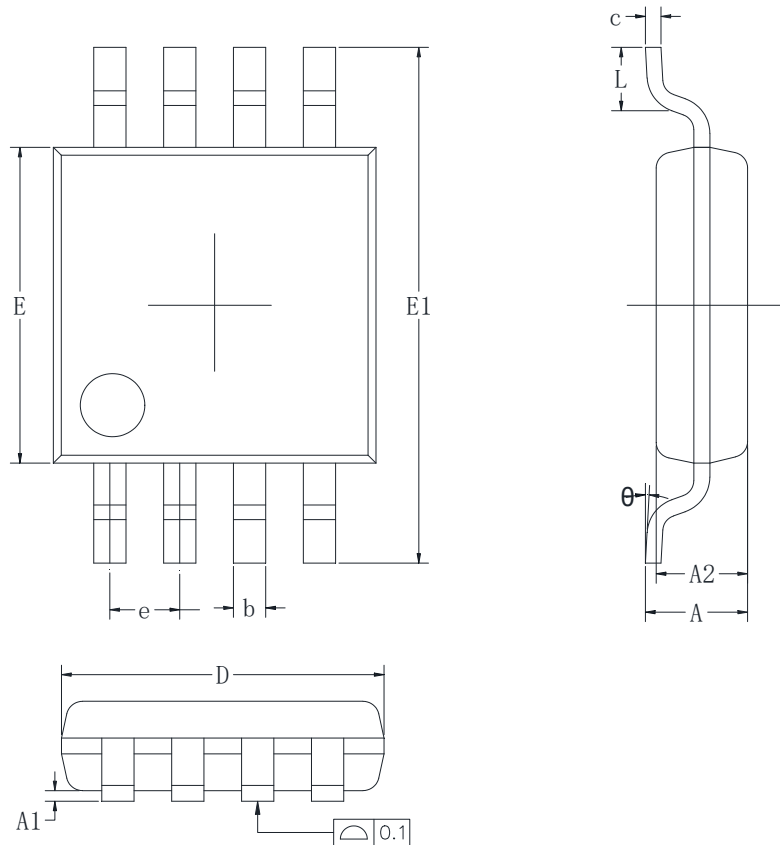
**Figure 11 Series Application**

# 11 Package Outline Dimensions and Recommend Land Pattern Layout

## 11.1 MSOP-8

### Package Outline Dimensions

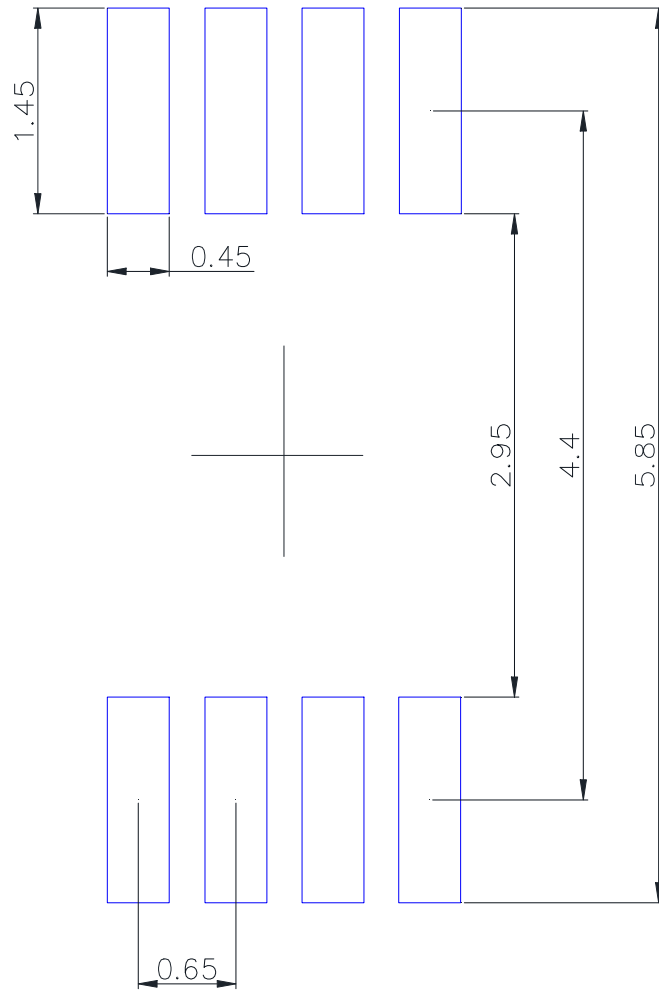
MSOP-8 Unit (mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
C	0.090	0.250	0.004	0.010
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
e	0.650(BSC)		0.026(BSC)	
L	0.400	0.800	0.016	0.031
θ	0°	8°	0°	8°

Recommended Land Pattern Layout

MSOP-8 Unit (mm)



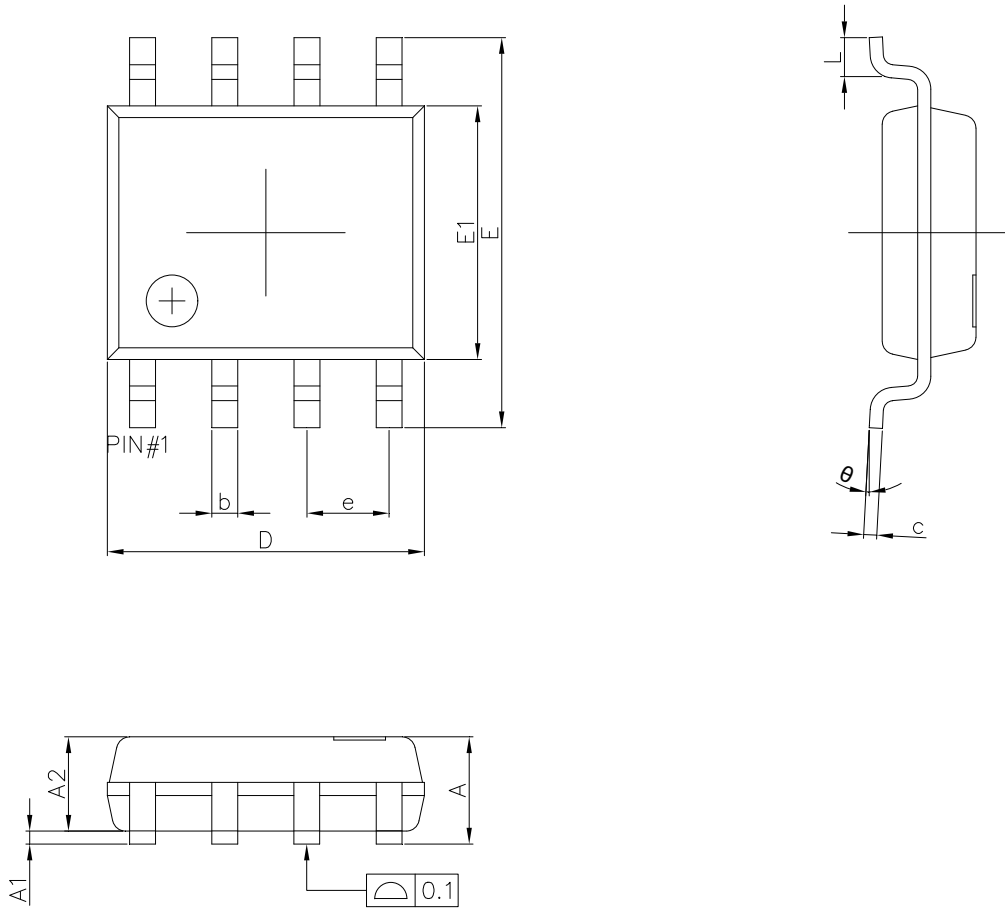
Notes:

- (1) All dimensions are in millimeter.
- (2) Recommend tolerance is within  $\pm 0.1\text{mm}$ .

**11.2 SOP-8**

**Package Outline Dimensions**

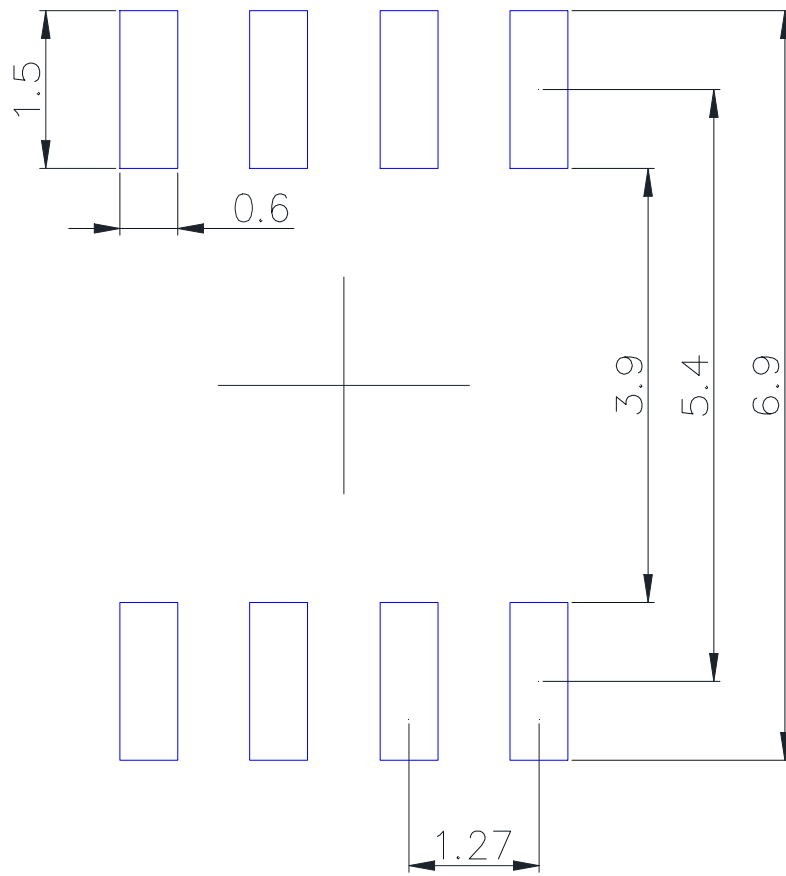
**SOP-8 Unit (mm)**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.650	0.049	0.065
b	0.33	0.51	0.013	0.020
C	0.17	0.25	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.700	4.100	0.146	0.161
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

Recommended Land Pattern Layout

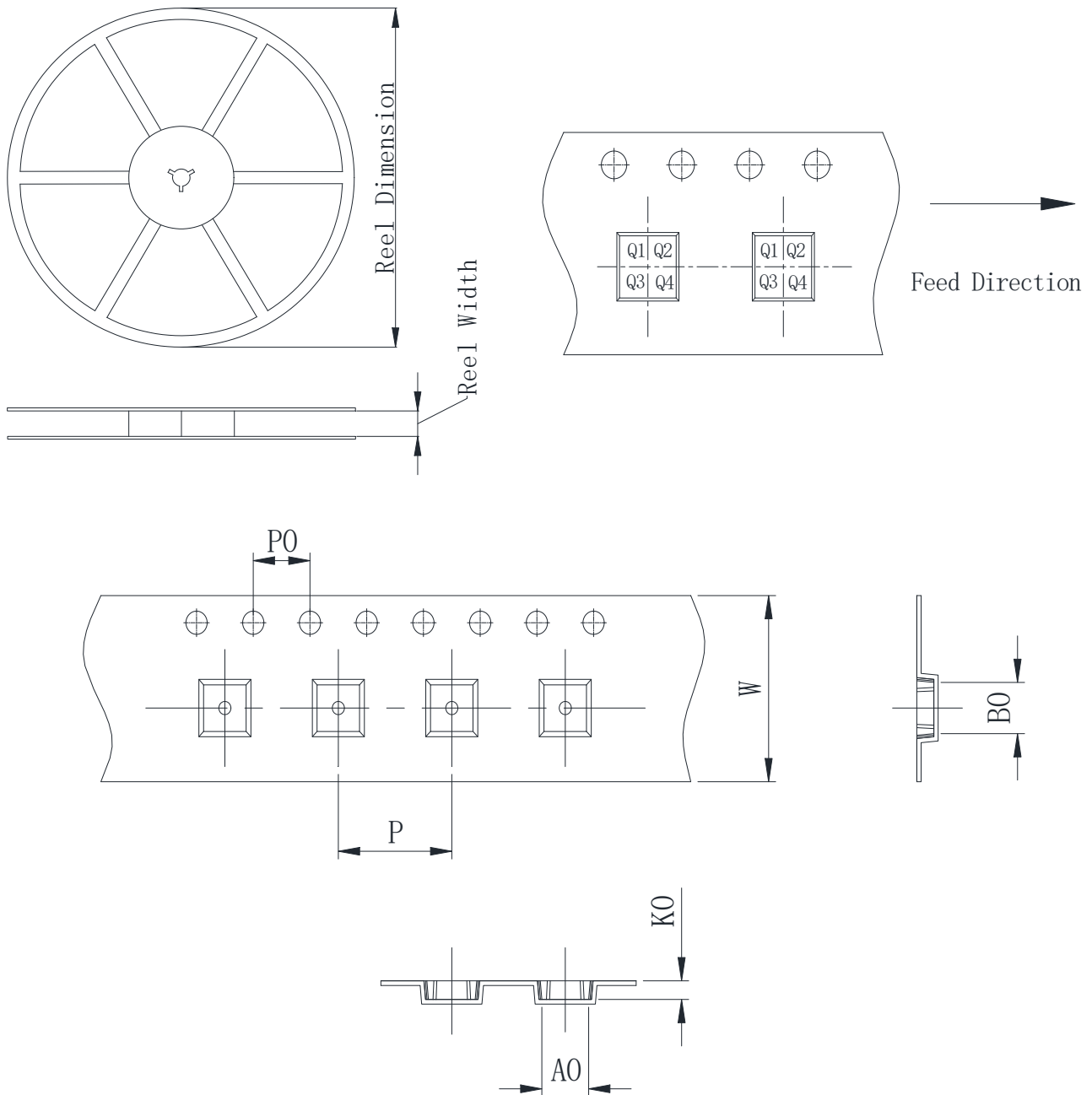
SOP-8 Unit (mm)



Notes:

- (1) All dimensions are in millimeter.
- (2) Recommend tolerance is within  $\pm 0.1$ mm.

## 12 Packing information



Package type	Reel size	Reel dimension (±3.0mm)	Reel width (±1.0mm)	A0 (±0.1mm)	B0 (±0.1mm)	K0 (±0.1mm)	P (±0.1mm)	P0 (±0.1mm)	W (±0.3mm)	Pin1
MSOP-8	13'	330	12.4	5.2/5.4	3.3/3.4	1.5/1.4	8.0	4.0	12.0	Q1
SOP-8	13'	330	12.4	6.4/6.6	5.4/5.3	2.1/1.9	8.0	4.0	12.0	Q1

## 13 Version History

Version	Date	Changes
Rev.1.0	2026-04-02	Initial release

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