

# PJ75238 Datasheet

## 85V, 16-Bit, High-Precision Power Monitor With I2C Interface

**Version: Preliminary Datasheet**

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## 1 General Description

The PJ75238 is an ultra-precise digital power monitor with a 16-bit delta-sigma ADC specifically designed for current-sensing applications. The device can measure a full-scale differential input of  $\pm 163.84$  mV or  $\pm 40.96$  mV across a resistive shunt sense element with common-mode voltage support from -0.3V to +85V. The PJ75238 reports current, bus voltage, temperature, and power. The integrated temperature sensor is  $\pm 1^\circ\text{C}$  accurate for die temperature measurement and is useful in monitoring the system ambient temperature.

The device allows for selectable ADC conversion times from 50  $\mu\text{s}$  to 4.12 ms as well as sample averaging from 1x to 1024x, which further helps reduce the noise of the measured data.

## 2 Features

- ◆ High-resolution, 16-bit delta-sigma ADC
- ◆ Current monitoring accuracy:
  - Offset voltage:  $\pm 5$   $\mu\text{V}$  (maximum)
  - Offset drift:  $\pm 0.02$   $\mu\text{V}/^\circ\text{C}$  (maximum)
  - Gain error:  $\pm 0.1\%$  (maximum)
  - Gain error drift:  $\pm 25$  ppm/ $^\circ\text{C}$  (maximum)
- ◆ Power monitoring accuracy:
  - 0.7% full scale,  $-40^\circ\text{C}$  to  $+125^\circ\text{C}$  (maximum)
- ◆ Wide common-mode range: -0.3 V to +85 V
- ◆ Shunt full-scale differential range:  
 $\pm 163.84$  mV /  $\pm 40.96$  mV
- ◆ Input bias current: 2.5 nA (maximum)
- ◆ Fast alert response: 75  $\mu\text{s}$
- ◆ Temperature sensor:  $\pm 1^\circ\text{C}$  (maximum at  $25^\circ\text{C}$ )
- ◆ 2.94-MHz high-speed I2C interface with 16 pin selectable addresses
- ◆ Operates from 2.7-V to 5.5-V

## 3 Applications

- ◆ Industrial battery packs
- ◆ Power-over-ethernet (PoE)
- ◆ Telecom equipment
- ◆ Enterprise servers

## 4 Ordering Information

### 4.1 Ordering Information

Order number	Marking ID	Package	MSL	Description
PJ75238M	A3YM DNN	MSOP-10	Level-3	Halogen free RoHS compliant in T/R, 3,000pcs/Reel

### 4.2 Marking Information

Marking	Package	Definition
A3YM DNN	MSOP-10	A3: Product code ; Y: Year code M: Month code D: Date code ; NN: Serial number

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## 5 Pin Configuration

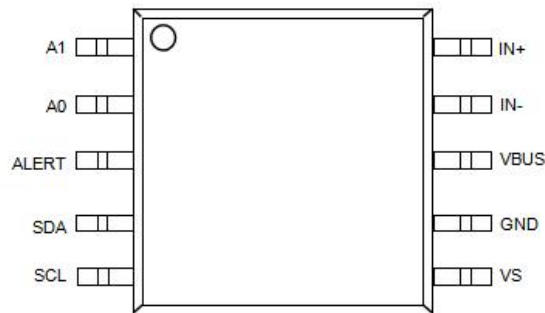


Figure 1 MSOP-10 Pin configuration (Top View)

## 6 Typical Application

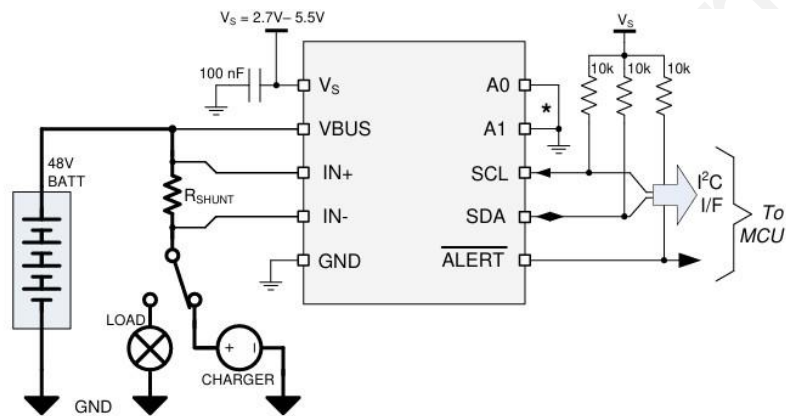


Figure 2 Typical Application of PJ75238

## 7 Functional Pin Description

Pin		Type	Description
Num	Name		
1	A1	Digital input	I2C address pin. Connect to GND, SCL, SDA, or VS.
2	A0	Digital input	I2C address pin. Connect to GND, SCL, SDA, or VS.
3	ALERT	Digital output	Open-drain alert output, default state is active low.
4	SDA	Digital input/output	Open-drain bidirectional I2C data.
5	SCL	Digital input	I2C clock input.
6	VS	Power supply	Power supply, 2.7 V to 5.5 V.
7	GND	Ground	Ground.
8	VBUS	Analog input	Bus voltage input.
9	IN-	Analog input	Negative input to the device. For high-side applications, connect to load side of sense resistor. For low-side applications, connect to ground side of sense resistor.
10	IN+	Analog input	Positive input to the device. For high-side applications, connect to power supply side of sense resistor. For low-side applications, connect to load side of sense resistor.

## 8 Function Block

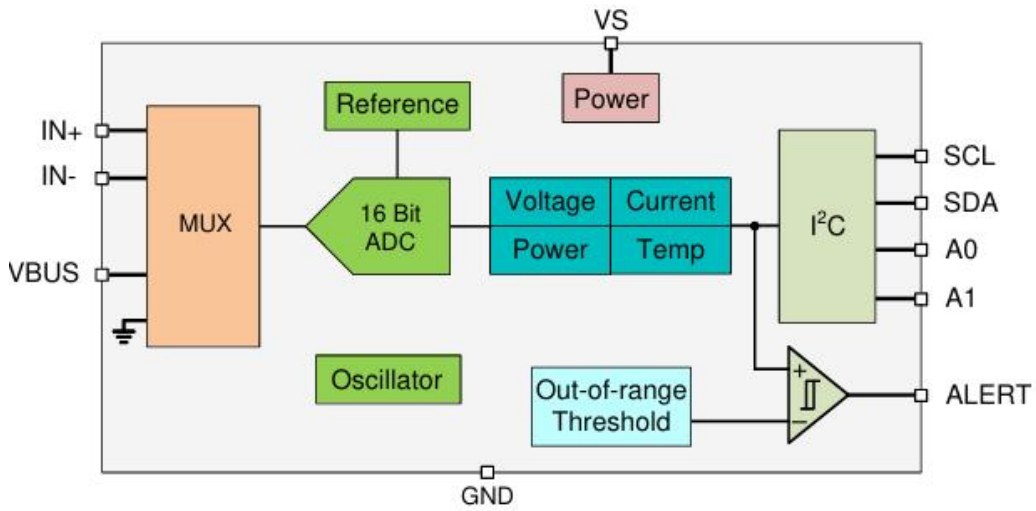


Figure 3 PJ75238 Function Block

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## 9 Specification

### 9.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

Parameter	Symbol	Min	Max	Unit
Supply Voltage	$V_S$		6	V
Analog Inputs, VIN+, VIN-,	Differential (VIN+) – (VIN-)	-40	40	V
Common-mode Voltage	$V_{cm}$	-0.3	85	V
Bus Input	$V_{BUS}$	-0.3	85	V
Alert Output	$V_{Alert}$	-0.3	$V_S+0.3$	V
Pin Sink	$I_{IN}$		5	mA
Pin Source	$I_{OUT}$		10	mA
Junction temperature	$T_J$		150	°C
Storage temperature	$T_{stg}$	-65	150	°C

Note:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at the "Absolute Maximum Ratings" conditions or any other conditions beyond those indicated under "Recommended Operating Conditions" is not recommended. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

### 9.2 Handling Ratings

Parameter	Description	Rating	Unit
ESD <sup>(1)</sup>	Human Body Model (HBM) ESD stress voltage <sup>(2)</sup>	±2000	V
	Charged Device Model (CDM) ESD stress voltage <sup>(3)</sup> , all pins	±1000	V

1. Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

2. Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

3. Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250- V CDM allows safe manufacturing with a standard ESD control process.

### 9.3 Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Supply Voltage	$V_S$	2.7	5.5	V
Common-mode Input Range	$V_{CM}$	-0.3	85	V
Operation Temperature Range	$T_A$	-40	125	°C

## 9.4 Electrical Characteristics

 at  $T_A = 25\text{ }^\circ\text{C}$ ,  $V_S = 3.3\text{ V}$ ,  $V_{\text{SENSE}} = V_{\text{IN}+} - V_{\text{IN}-} = 0\text{ V}$ ,  $V_{\text{CM}} = V_{\text{IN}-} = 48\text{ V}$  (unless otherwise noted)

Parameter		Test Conditions	Min	Typ	Max	Unit
<b>INPUT</b>						
$V_{\text{CM}}$	Common-mode input range	$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$	-0.3		85	V
$V_{\text{VBUS}}$	Bus voltage input range		0		85	V
CMRR	Common-mode rejection	$-0.3\text{ V} < V_{\text{CM}} < 85\text{ V}$ , $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$	140	160		dB
$V_{\text{DIFF}}$	Shunt voltage input range	$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$ , ADCRANGE = 0	-163.84		163.84	mV
		$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$ , ADCRANGE = 1	-40.96		40.96	mV
$V_{\text{os}}$	Shunt offset voltage	$V_{\text{CM}} = 48\text{ V}$		$\pm 1.5$	$\pm 5$	$\mu\text{V}$
		$V_{\text{CM}} = 0\text{ V}$		$\pm 1.5$	$\pm 5$	$\mu\text{V}$
$dV_{\text{os}}/dT$	Shunt offset voltage drift	$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$		$\pm 2$	$\pm 20$	nV/ $^\circ\text{C}$
PSRR	Shunt offset voltage vs power supply	$V_S = 2.7\text{ V}$ to $5.5\text{ V}$ , $T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$		$\pm 0.1$	$\pm 1$	$\mu\text{V}/\text{V}$
$V_{\text{os\_bus}}$	$V_{\text{BUS}}$ offset voltage	$V_{\text{BUS}} = 20\text{ mV}$		$\pm 1$	$\pm 5$	mV
$dV_{\text{os}}/dT$	$V_{\text{BUS}}$ offset voltage drift	$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$		$\pm 4$	$\pm 40$	$\mu\text{V}/\text{ }^\circ\text{C}$
PSRR	$V_{\text{BUS}}$ offset voltage vs power supply	$V_S = 2.7\text{ V}$ to $5.5\text{ V}$		$\pm 1.1$		mV/V
$I_B$	Input bias current	Either input, IN+ or IN-, $V_{\text{CM}} = 85\text{ V}$		0.1	2.5	nA
$Z_{\text{VBUS}}$	VBUS pin input impedance	Active mode	0.8	1	1.2	M $\Omega$
$I_{\text{VBUS}}$	VBUS pin leakage current	Shutdown mode, $V_{\text{BUS}} = 85\text{ V}$		10		nA
$R_{\text{DIFF}}$	Input differential impedance	Active mode, $V_{\text{IN}+} - V_{\text{IN}-} < 164\text{ mV}$		92		k $\Omega$
<b>DC ACCURACY</b>						
$G_{\text{SERR}}$	Shunt voltage gain error			$\pm 0.01$	$\pm 0.1$	%
$G_{\text{S\_DRFT}}$	Shunt voltage gain error drift				$\pm 25$	ppm/ $^\circ\text{C}$
$G_{\text{BERR}}$	$V_{\text{BUS}}$ voltage gain error			$\pm 0.01$	$\pm 0.1$	%
$G_{\text{B\_DRFT}}$	$V_{\text{BUS}}$ voltage gain error drift				$\pm 25$	ppm/ $^\circ\text{C}$
$P_{\text{TME}}$	Power total measurement error (TME)	$T_A = -40\text{ }^\circ\text{C}$ to $+125\text{ }^\circ\text{C}$ , at full scale			$\pm 0.7$	%
	ADC resolution			16		Bits
	1 LSB step size	Shunt voltage, ADCRANGE = 0		5		$\mu\text{V}$
		Shunt voltage, ADCRANGE = 1		1.25		$\mu\text{V}$
		Bus voltage		3.125		mV
		Temperature		125		m $^\circ\text{C}$
$T_{\text{CT}}$	ADC conversion-time <sup>(1)</sup>	Conversion time field = 0h		50		$\mu\text{s}$
		Conversion time field = 1h		84		
		Conversion time field = 2h		150		
		Conversion time field = 3h		280		
		Conversion time field = 4h		540		
		Conversion time field = 5h		1052		
		Conversion time field = 6h		2074		
Conversion time field = 7h		4120				
INL	Integral Non-Linearity			$\pm 2$		m%
DNL	Differential Non-Linearity			0.2		LSB

Parameter		Test Conditions	Min	Typ	Max	Unit
<b>CLOCK SOURCE</b>						
F <sub>OSC</sub>	Internal oscillator frequency			1		MHz
F <sub>OSC_TOL</sub>	Internal oscillator frequency tolerance	T <sub>A</sub> = 25°C			±0.5	%
		T <sub>A</sub> = -40°C to +125°C			±1	%
<b>TEMPERATURE SENSOR</b>						
	Measurement range		-40		+125	°C
	Temperature accuracy	T <sub>A</sub> = 25°C		±0.15	±1	°C
		T <sub>A</sub> = -40°C to +125°C		±0.2	±2	°C
<b>POWER SUPPLY</b>						
V <sub>S</sub>	Supply voltage		2.7		5.5	V
I <sub>Q</sub>	Quiescent current	V <sub>SENSE</sub> = 0 V		640	750	μA
		V <sub>SENSE</sub> = 0 V, T <sub>A</sub> = -40°C to +125°C			1.1	mA
I <sub>QSD</sub>	Quiescent current, shutdown	Shutdown mode		2.8	5	μA
T <sub>POR</sub>	Device start-up time	Power-up (NPOR)		300		μs
		From shutdown mode		60		
<b>DIGITAL INPUT / OUTPUT</b>						
V <sub>IH</sub>	Logic input level, high	SDA, SCL	1.2		5.5	V
V <sub>IL</sub>	Logic input level, low		GND		0.4	V
V <sub>OL</sub>	Logic output level, low	I <sub>OL</sub> = 3 mA	GND		0.4	V
I <sub>IO_LEAK</sub>	Digital leakage input current	0 ≤ V <sub>IN</sub> ≤ V <sub>S</sub>	-1		1	μA

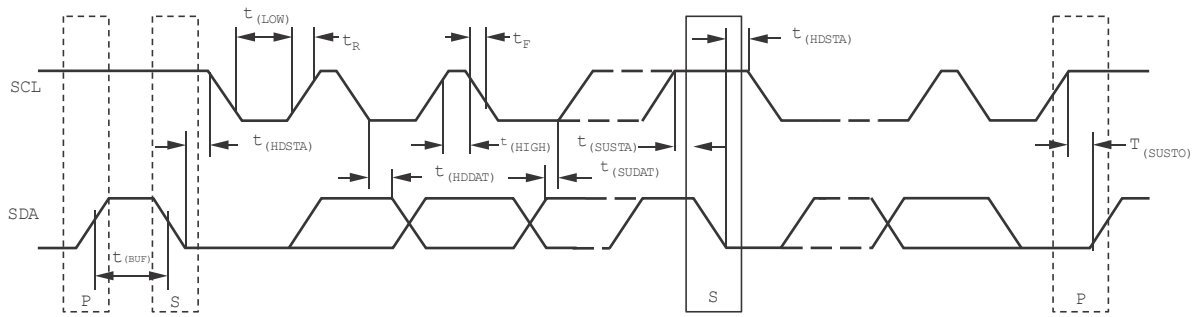
**Note:**

1. Subject to oscillator accuracy and drift.

**9.5 Timing Requirements (I2C)**

		Min	Nom	Max	Unit
<b>I2C BUS (FAST MODE)</b>					
F(SCL)	I2C clock frequency	1		400	kHz
t(BUF)	Bus free time between STOP and START conditions	600			ns
t(HDSTA)	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
t(SUSTA)	Repeated START condition setup time	100			ns
t(SUSTO)	STOP condition setup time	100			ns
t(HDDAT)	Data hold time	10		900	ns
t(SUDAT)	Data setup time	100			ns
t(LOW)	SCL clock low period	1300			ns
t(HIGH)	SCL clock high period	600			ns
tF	Data fall time			300	ns
tF	Clock fall time			300	ns
tR	Clock rise time			300	ns
<b>I2C BUS (HIGH-SPEED MODE)</b>					
F(SCL)	I2C clock frequency	10		2940	kHz
t(BUF)	Bus free time between STOP and START conditions	160			ns
t(HDSTA)	Hold time after a repeated START condition. After this period, the first clock is generated.	100			ns
t(SUSTA)	Repeated START condition setup time	100			ns
t(SUSTO)	STOP condition setup time	100			ns
t(HDDAT)	Data hold time	10		125	ns
t(SUDAT)	Data setup time	20			ns
t(LOW)	SCL clock low period	200			ns
t(HIGH)	SCL clock high period	60			ns
tF	Data fall time			80	ns
tF	Clock fall time			40	ns
tR	Clock rise time			40	ns

**9.6 Timing Diagram**



**Figure 4 I2C Timing Diagram**

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## 10 Function Description

### 10.1 Overview

The PJ75238 device is a digital current sense amplifier with an I<sup>2</sup>C digital interface. It measures shunt voltage, bus voltage and internal temperature while calculating current, power necessary for accurate decision making in precisely controlled systems. Programmable registers allow flexible configuration for measurement precision as well as continuous or triggered operation.

### 10.2 Feature Description

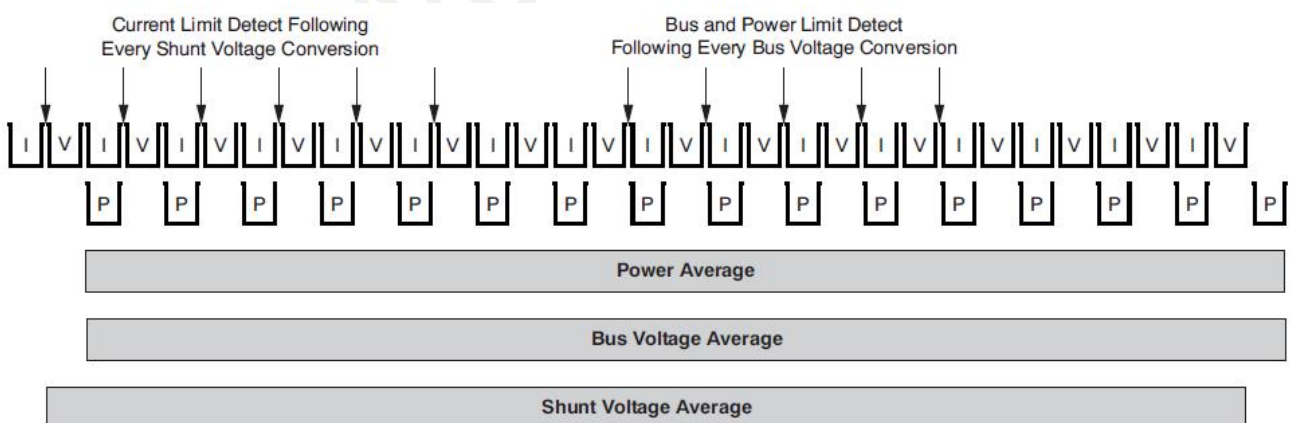
#### 10.2.1 Versatile High Voltage Measurement Capability

The PJ75238 operates off a 2.7 V to 5.5 V supply but can measure voltage and current on rails as high as 85 V. The current is measured by sensing the voltage drop across external shunt resistor at the IN+ and IN- pins. The input stage is designed such that the input common-mode voltage can be higher than the device supply voltage, V<sub>s</sub>. The supported common-mode voltage range at the input pins is -0.3 V to +85 V, which makes the device well suited for both high-side and low-side current measurements.

The device also measures the bus supply voltage through the V<sub>BUS</sub> pin and temperature through the integrated temperature sensor. The differential shunt voltage is measured between the IN+ and IN- pins, while the bus voltage is measured with respect to device ground. Monitored bus voltages can range from 0 V to 85 V, while monitored temperatures can range from -40 °C to +125 °C.

#### 10.2.2 Power Calculation

The current and power are calculated after a shunt voltage and bus voltage measurement as shown in Figure 5. Power is calculated based on the previous current calculation and the latest bus voltage measurement. If the value loaded into the SHUNT\_CAL register is zero, the power value reported is also zero. The current and power values are considered intermediate results (unless the averaging is set to 1) and are stored in an internal accumulation register. Following every measured sample, the newly-calculated values for current and power are appended to this accumulation register until all of the samples have been measured and averaged. After all of the samples have been measured and the corresponding current and power calculations have been made, the accumulated average for each of these parameters is then loaded to the corresponding output registers where they can then be read.



**Figure 5 Power Calculation Scheme**

### **10.2.3 Low Bias Current**

The PJ75238 features very low input bias current which provides several benefits. The low input bias current of the PJ75238 reduces the current consumed by the device in both active and shutdown state. Another benefit of low bias current is that it allows the use of input filters to reject high-frequency noise before the signal is converted to digital data. In traditional digital current-sense amplifiers, the addition of input filters comes at the cost of reduced accuracy. However, as a result of the low bias current, the reduction in accuracy due to input filters is minimized. An additional benefit of low bias current is the ability to use a larger shunt resistor to accurately sense smaller currents. Use of a larger value for the shunt resistor allows the device to accurately monitor currents in the sub-mA range.

### **10.2.4 High-Precision Delta-Sigma ADC**

The integrated ADC is a high-performance, low-offset, low-drift, delta-sigma ADC designed to support bidirectional current flow at the shunt voltage measurement channel. The measured inputs are selected through the high-voltage input multiplexer to the ADC inputs. The ADC architecture enables lower drift measurement across temperature and consistent offset measurements across the common-mode voltage, temperature, and power supply variations. A low-offset ADC is preferred in current sensing applications to provide near 0-V offset voltage that maximizes useful dynamic range of the system.

### **10.2.5 Integrated Precision Oscillator**

The internal time-base of the device is provided by an internal oscillator that is trimmed to less than 0.5% tolerance at room temperature. The precision oscillator is the timing source for ADC conversions. The digital filter response varies with conversion time; therefore, the precise clock ensures filter response and notch frequency consistency across temperature. On power up, the internal oscillator and ADC take roughly 300  $\mu$ s to reach <1% error stability. Once the clock stabilizes, the ADC data output will be accurate to the electrical specifications.

### **10.2.6 Multi-Alert Monitoring and Fault Detection**

The PJ75238 includes a multipurpose, open-drain ALERT output pin that can be used to report multiple diagnostics or as an indicator that the ADC conversion is complete when the device is operating in both triggered and continuous conversion mode. The diagnostics are constantly monitored and can be reported through the ALERT pin whenever the monitored output value crosses its associated out-of-range threshold. The diagnostic includes Shunt Under Voltage Limit 、 Shunt Over Voltage Limit 、 Bus Voltage Over-Limit 、 Bus Voltage Under-Limit 、 Temperature Over-Limit 、 Power Over-Limit.

The diagnostics listed in Table 1 are constantly monitored and can be reported through the ALERT pin whenever the monitored output value crosses its associated out-of-range threshold

**Table 1. ALERT Diagnostics Description**

PJ75238 DIAGNOSTIC	STATUS BIT IN DIAG_ALERT REGISTER (RO)	OUT-OF-RANGE THRESHOLD REGISTER (R/W)	REGISTER DEFAULT VALUE
Shunt Under Voltage Limit	SHNTUL	SUVL	0x8000 h (two's complement)
Shunt Over Voltage Limit	SHNTOL	SOVL	0x7FFF h (two's complement)
Bus Voltage Over-Limit	BUSOL	BOVL	0x7FFF h (two's complement, positive values only)
Bus Voltage Under-Limit	BUSUL	BUVL	0x0000 h (two's complement, positive values only)
Temperature Over-Limit	TMPO	TEMP_LIMIT	0xFFFF h (two's complement, positive values only)
Power Over-Limit	POL	PWR_LIMIT	0x7FFF h (two's complement)

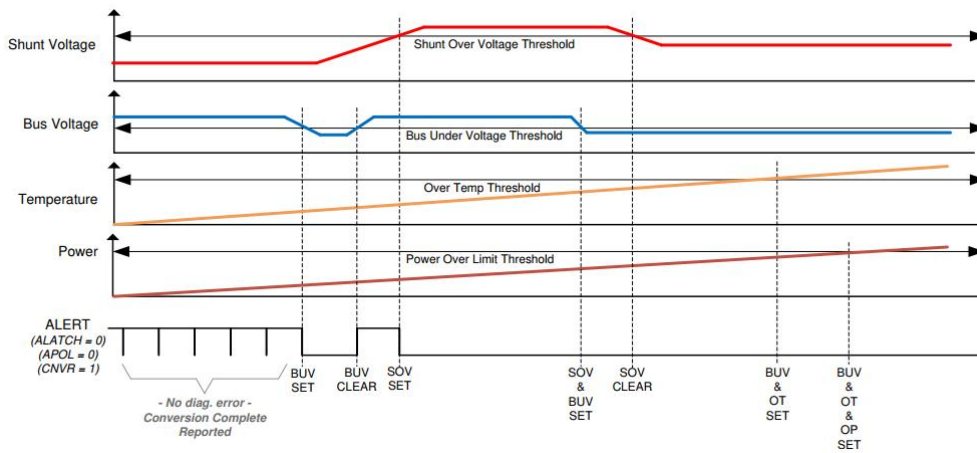
A read of the DIAG\_ALERT register is used to determine which diagnostic has triggered the ALERT pin. This register is also used to monitor other associated diagnostics as well as configure some ALERT pin functions.

- Alert latch enable — In case the ALERT pin is triggered, this function will hold the value of the pin even after all diagnostic conditions have cleared. A read of the DIAG\_ALERT register will reset the status of the ALERT pin. This function is enabled by setting the ALATCH bit.
- Conversion ready enable — Enables the ALERT pin to assert when an ADC conversion has completed and output values are ready to be read through the digital interface. This function is enabled by setting the CNVR bit. The conversion completed events can also be read through the CNVRF bit regardless of the CNVR bit setting.
- Alert comparison on averaged output — Allows the out-of-range threshold value to be compared to the averaged data values produced by the ADC. This helps to additionally remove noise from the output data when compared to the out-of-range threshold to avoid false alerts due to noise. However, the diagnostic will be delayed due to the time needed for averaging. This function is enabled by setting the SLOWALERT bit.
- Alert polarity — Allows the device to invert the active state of the ALERT pin. Note that the ALERT pin is an open-drain output that must be pulled-up by a resistor. The ALERT pin is active-low by default and can be configured for active high function using the APOL control bit.

Other diagnostic functions that are not reported by the ALERT pin but are available by reading the DIAG\_ALERT register:

- Math overflow — Indicated by the MATHOF bit, reports when an arithmetic operation has caused an internal register overflow.
- Memory status — Indicated by the MEMSTAT bit, monitors the health of the device non-volatile trim memory. This bit should always read '1' when the device is operating properly.

When the ALERT pin is configured to report the ADC conversion complete event, the ALERT pin becomes a multipurpose reporting output. Figure 6 shows an example where the device reports ADC conversion complete events while the PJ75238 device is subject to shunt over voltage (over current) event, bus under voltage event, over temperature event and over power-limit event.



**Figure 6 Multi – Alert Configuration**

## 10.3 Programming

### 10.3.1 I2C Serial Interface

The PJ75238 operates only as a secondary device on both the SMBus and I<sup>2</sup>C interfaces. Connections to the bus are made through the open-drain SDA and SCL lines. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. Although the device integrates spike suppression into the digital I/O lines, proper layout techniques help minimize the amount of coupling into the communication lines.

The PJ75238 supports the transmission protocol for fast mode (1 kHz to 400 kHz) and high-speed mode (1 kHz to 2.94 MHz). All data bytes are transmitted most significant byte first and follow the SMBus 3.0 transfer protocol.

To communicate with the PJ75238, the main device must first address secondary devices through a secondary device address byte. The secondary device address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

The device has two address pins, A0 and A1. Table 2 lists the pin logic levels for each of the 16 possible addresses. The device samples the state of pins A0 and A1 on every bus communication. Establish the pin states before any activity on the interface occurs. When connecting the SDA pin to either A0 or A1 to set the device address, additional hold time of 100 ns is needed on the MSB of the I2C address to insure correct device addressing.

**Table 2. Address Pins and Secondary Device Addresses**

A1	A0	Secondary Device Address
GND	GND	1000000
GND	VS	1000001
GND	SDA	1000010
GND	SCL	1000011
VS	GND	1000100
VS	VS	1000101
VS	SDA	1000110
VS	SCL	1000111
SDA	GND	1001000
SDA	VS	1001001
SDA	SDA	1001010
SDA	SCL	1001011

A1	A0	Secondary Device Address
SCL	GND	1001100
SCL	VS	1001101
SCL	SDA	1001110
SCL	SCL	1001111

### 10.3.2 Writing to and Reading Through the I2C Serial Interface

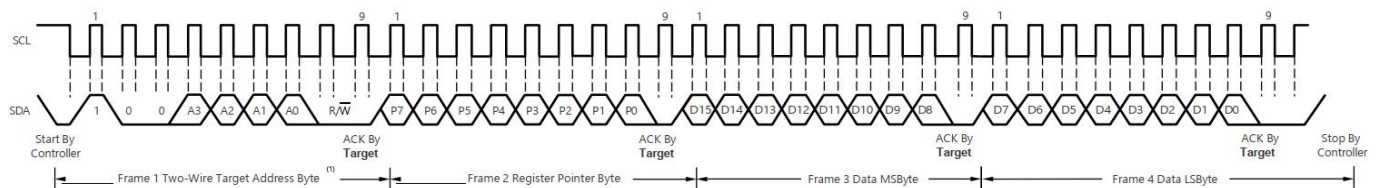
Accessing a specific register on the PJ75238 is accomplished by writing the appropriate value to the register pointer. Refer to Section 10.4 for a complete list of registers and corresponding addresses. The value for the register pointer (as shown in Figure 9) is the first byte transferred after the secondary device address byte with the R/W bit low. Every write operation to the device requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the main device. This byte is the secondary device address, with the R/W bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the main device is the address of the register to be accessed. This register address value updates the register pointer to the desired internal device register. The next two bytes are written to the register addressed by the register pointer. The device acknowledges receipt of each data byte. The main device may terminate data transfer by generating a start or stop condition.

When reading from the device, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a secondary device address byte with the R/W bit low, followed by the register pointer byte. No additional data are required. The main device then generates a start condition and sends the address byte for the secondary device with the R/W bit high to initiate the read command. The next byte is transmitted by the secondary device and is the most significant byte of the register indicated by the register pointer. This byte is followed by an Acknowledge from the main device; then the secondary device transmits the least significant byte. The main device may or may not acknowledge receipt of the second data byte. The main device may terminate data transfer by generating a Not-Acknowledge after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the device retains the register pointer value until it is changed by the next write operation.

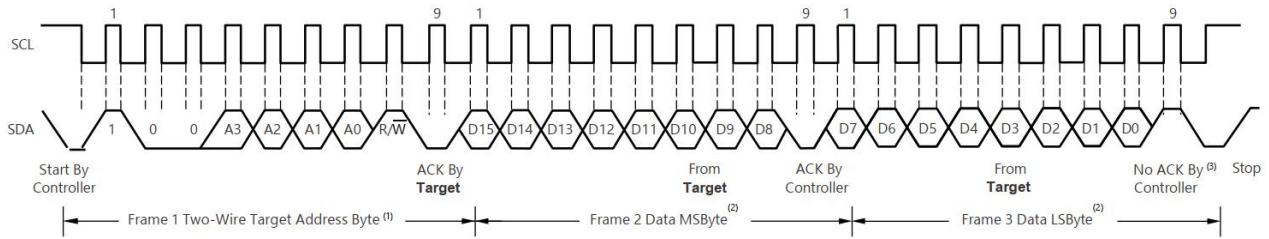
Figure 7 shows the write operation timing diagram. Figure 8 shows the read operation timing diagram. These diagrams are shown for reading/writing to 16 bit registers.

Register bytes are sent most-significant byte first, followed by the least significant byte.



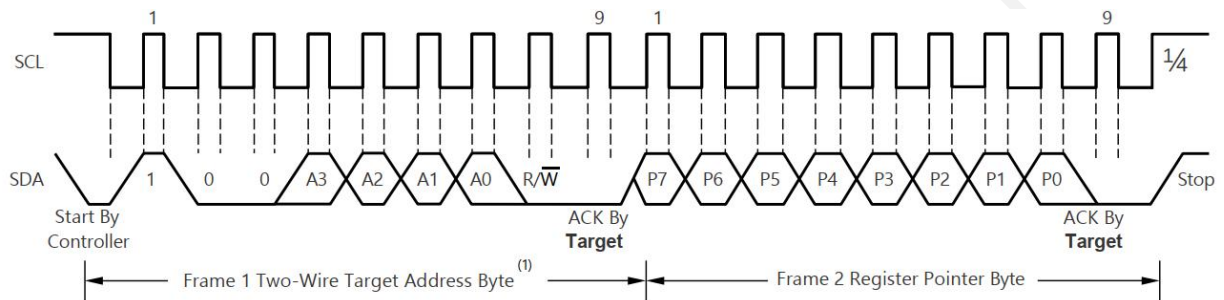
- A. The value of the Secondary Device Address byte is determined by the settings of the A0 and A1 pins.
- B. The device does not support packet error checking (PEC) or perform clock stretching.

**Figure 7 Timing Diagram for Write Word Format**



- A. The value of the Secondary Device Address byte is determined by the settings of the A0 and A1 pins.
- B. Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated.
- C. ACK by the main device can also be sent.
- D. The device does not support packet error checking (PEC) or perform clock stretching.

**Figure 8 Timing Diagram for Read Word Format**



- A. The value of the Secondary Device Address Byte is determined by the settings of the A0 and A1 pins.

**Figure 9 Typical Register Pointer Set**

## 10.4 Register Maps

### 10.4.1 PJ75238 Registers

Table 3 lists the PJ75238 registers. All register locations not listed in Table 3 should be considered as reserved locations and the register contents should not be modified.

**Table 3. PJ75238 Registers**

Address	Acronym	Register Name	Register Size (bits)	Section
0h	CONFIG	Configuration	16	10.4.2.1
1h	ADC_CONFIG	ADC Configuration	16	10.4.2.2
2h	SHUNT_CAL	Shunt Calibration	16	10.4.2.3
4h	VSHUNT	Shunt Voltage Measurement	16	10.4.2.4
5h	VBUS	Bus Voltage Measurement	16	10.4.2.5
6h	DIETEMP	Temperature Measurement	16	10.4.2.6
7h	CURRENT	Current Result	16	10.4.2.7
8h	POWER	Power Result	24	10.4.2.8
Bh	DIAG_ALRT	Diagnostic Flags and Alert	16	10.4.2.9
Ch	SOVL	Shunt Overvoltage Threshold	16	10.4.2.10
Dh	SUVL	Shunt Undervoltage Threshold	16	10.4.2.11
Eh	BOVL	Bus Overvoltage Threshold	16	10.4.2.12
Fh	BUVL	Bus Undervoltage Threshold	16	10.4.2.13
10h	TEMP_LIMIT	Temperature Over-Limit Threshold	16	10.4.2.14
11h	PWR_LIMIT	Power Over-Limit Threshold	16	10.4.2.15
3Eh	MANUFACTURER_ID	Manufacturer ID	16	10.4.2.16
3Fh	DEVICE_ID	Device ID	16	10.4.2.17

Complex bit access types are encoded to fit into small table cells. Table 4 shows the codes that are used for access types in this section.

**Table 4. PJ75238 Access Type Codes**

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

## 10.4.2 Register Description

### 10.4.2.1 Configuration (CONFIG) Register (Address = 0h) [reset = 0h]

The CONFIG register is shown in Table 5.

**Table 5. CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RST	R/W	0h	Reset Bit. Setting this bit to '1' generates a system reset that is the same as power-on reset. Resets all registers to default values. 0h = Normal Operation 1h = System Reset sets registers to default values This bit self-clears.
14	RESERVED	R/W	0h	Reserved. Always reads 0.
13-6	CONVDLY	R/W	0h	Sets the Delay for initial ADC conversion in steps of 2 ms. 0h = 0 s 1h = 2 ms FFh = 510 ms
5	RESERVED	R/W	0h	Reserved. Always reads 0.
4	ADCRANGE	R/W	0h	Shunt full scale range selection across IN+ and IN-. 0h = ±163.84 mV 1h = ± 40.96 mV
3-0	RESERVED	R	0h	Reserved. Always reads 0.

### 10.4.2.2 ADC Configuration (ADC\_CONFIG) Register (Address = 1h) [reset = FB68h]

The ADC\_CONFIG register is shown in Table 6.

**Table 6. ADC\_CONFIG Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-12	MODE	R/W	Fh	The user can set the MODE bits for continuous or triggered mode on bus voltage, shunt voltage or temperature measurement. 0h = Shutdown 1h = Triggered bus voltage, single shot 2h = Triggered shunt voltage, single shot 3h = Triggered shunt voltage and bus voltage, single shot 4h = Triggered temperature, single shot 5h = Triggered temperature and bus voltage, single shot 6h = Triggered temperature and shunt voltage, single shot 7h = Triggered bus voltage, shunt voltage and temperature, single shot 8h = Shutdown 9h = Continuous bus voltage only

Bit	Field	Type	Reset	Description
				Ah = Continuous shunt voltage only Bh = Continuous shunt and bus voltage Ch = Continuous temperature only Dh = Continuous bus voltage and temperature Eh = Continuous temperature and shunt voltage Fh = Continuous bus voltage, shunt voltage and temperature
11-9	VBUSCT	R/W	5h	Sets the conversion time of the bus voltage measurement: 0h = 50 $\mu$ s 1h = 84 $\mu$ s 2h = 150 $\mu$ s 3h = 280 $\mu$ s 4h = 540 $\mu$ s 5h = 1052 $\mu$ s 6h = 2074 $\mu$ s 7h = 4120 $\mu$ s
8-6	VSHCT	R/W	5h	Sets the conversion time of the shunt voltage measurement: 0h = 50 $\mu$ s 1h = 84 $\mu$ s 2h = 150 $\mu$ s 3h = 280 $\mu$ s 4h = 540 $\mu$ s 5h = 1052 $\mu$ s 6h = 2074 $\mu$ s 7h = 4120 $\mu$ s
5-3	VTCT	R/W	5h	Sets the conversion time of the temperature measurement: 0h = 50 $\mu$ s 1h = 84 $\mu$ s 2h = 150 $\mu$ s 3h = 280 $\mu$ s 4h = 540 $\mu$ s 5h = 1052 $\mu$ s 6h = 2074 $\mu$ s 7h = 4120 $\mu$ s
2-0	AVG	R/W	0h	Selects ADC sample averaging count. The averaging setting applies to all active inputs. When >0h, the output registers are updated after the averaging has completed. 0h = 1 1h = 4 2h = 16 3h = 64 4h = 128 5h = 256 6h = 512 7h = 1024

#### 10.4.2.3 Shunt Calibration (SHUNT\_CAL) Register (Address = 2h) [reset = 1000h]

The SHUNT\_CAL register is shown in Table 7

**Table 7. SHUNT\_CAL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	RESERVED	R	0h	Reserved. Always reads 0.
14-0	SHUNT_CAL	R/W	1000h	The register provides the device with a conversion constant value that represents shunt resistance used to calculate current value in Amperes. This also sets the resolution for the CURRENT register. Value calculation under Section 11.2.

#### 10.4.2.4 Shunt Voltage Measurement (VSHUNT) Register (Address = 4h) [reset = 0h]

The VSHUNT register is shown in Table 8.

**Table 8. VSHUNT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	VSHUNT	R	0h	Differential voltage measured across the shunt output. Two's complement value. Conversion factor: 5 $\mu$ V/LSB when <u>ADCRANGE</u> = 0 1.25 $\mu$ V/LSB when <u>ADCRANGE</u> = 1

#### 10.4.2.5 Bus Voltage Measurement (VBUS) Register (Address = 5h) [reset = 0h]

The VBUS register is shown in Table 9.

**Table 9. VBUS Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	VBUS	R	0h	Bus voltage output. Two's complement value, however always positive. Conversion factor: 3.125 mV/LSB

#### 10.4.2.6 Temperature Measurement (DIETEMP) Register (Address = 6h) [reset = 0h]

The DIETEMP register is shown in Table 10.

**Table 10. DIETEMP Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-4	DIETEMP	R	0h	Internal die temperature measurement. Two's complement value. Conversion factor: 125 m°C/LSB
3-0	RESERVED	R	0h	Reserved. Always reads 0.

#### 10.4.2.7 Current Result (CURRENT) Register (Address = 7h) [reset = 0h]

The CURRENT register is shown in Table 11

**Table 11. CURRENT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	CURRENT	R	0h	Calculated current output in Amperes. Two's complement value. Value description under Section 11.2.

#### 10.4.2.8 Power Result (POWER) Register (Address = 8h) [reset = 0h]

The POWER register is shown in Table 12

**Table 12. POWER Register Field Descriptions**

Bit	Field	Type	Reset	Description
23-0	POWER	R	0h	Calculated power output. Output value in watts. Unsigned representation. Positive value. Value description under Section 11.2.

#### 10.4.2.9 Diagnostic Flags and Alert (DIAG\_ALERT) Register (Address = Bh) [reset = 0001h]

The DIAG\_ALERT register is shown in Table 13

**Table 13. DIAG\_ALERT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	ALATCH	R/W	0h	When the Alert Latch Enable bit is set to Transparent mode, the Alert pin and Flag bit reset to the idle state when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the Alert pin and Alert Flag bit remain active following a fault until the DIAG_ALERT Register has been read. 0h = Transparent

Bit	Field	Type	Reset	Description
				1h = Latched
14	CNVR	R/W	0h	Setting this bit high configures the Alert pin to be asserted when the Conversion Ready Flag (bit 1) is asserted, indicating that a conversion cycle has completed. 0h = Disable conversion ready flag on ALERT pin 1h = Enables conversion ready flag on ALERT pin
13	SLOWALERT	R/W	0h	When enabled, ALERT function is asserted on the completed averaged value. This gives the flexibility to delay the ALERT until after the averaged value. 0h = ALERT comparison on non-averaged (ADC) value 1h = ALERT comparison on averaged value
12	APOL	R/W	0h	Alert Polarity bit sets the Alert pin polarity. 0h = Normal (Active-low, open-drain) 1h = Inverted (active-high, open-drain)
11-10	RESERVED	R	0h	Reserved. Always read 0.
9	MATHOF	R	0h	This bit is set to 1 if an arithmetic operation resulted in an overflow error. It indicates that current and power data may be invalid. 0h = Normal 1h = Overflow Must be manually cleared by triggering another conversion.
8	RESERVED	R	0h	Reserved. Always read 0.
7	TMPOL	R/W	0h	This bit is set to 1 if the temperature measurement exceeds the threshold limit in the temperature over-limit register. 0h = Normal 1h = Over Temp Event When ALATCH =1 this bit is cleared by reading this register.
6	SHNTOL	R/W	0h	This bit is set to 1 if the shunt voltage measurement exceeds the threshold limit in the shunt over-limit register. 0h = Normal 1h = Over Shunt Voltage Event When ALATCH =1 this bit is cleared by reading this register.
5	SHNTUL	R/W	0h	This bit is set to 1 if the shunt voltage measurement falls below the threshold limit in the shunt under-limit register. 0h = Normal 1h = Under Shunt Voltage Event When ALATCH =1 this bit is cleared by reading this register.
4	BUSOL	R/W	0h	This bit is set to 1 if the bus voltage measurement exceeds the threshold limit in the bus over-limit register. 0h = Normal 1h = Bus Over-Limit Event When ALATCH =1 this bit is cleared by reading this register.
3	BUSUL	R/W	0h	This bit is set to 1 if the bus voltage measurement falls below the threshold limit in the bus under-limit register. 0h = Normal 1h = Bus Under-Limit Event When ALATCH =1 this bit is cleared by reading this register.
2	POL	R/W	0h	This bit is set to 1 if the power measurement exceeds the threshold limit in the power limit register. 0h = Normal 1h = Power Over-Limit Event When ALATCH =1 this bit is cleared by reading this register.
1	CNVRF	R/W	0h	This bit is set to 1 if the conversion is completed. 0h = Normal 1h = Conversion is complete When ALATCH =1 this bit is cleared by reading this register or starting a new triggered conversion.
0	MEMSTAT	R/W	1h	This bit is set to 0 if a checksum error is detected in the device trim memory space. 0h = Memory Checksum Error 1h = Normal Operation

#### 10.4.2.10 Shunt Overvoltage Threshold (SOVL) Register (Address = Ch) [reset = 7FFFh]

If negative values are entered in this register, then a shunt voltage measurement of 0 V will trip this alarm. When using negative values for the shunt under and overvoltage thresholds be aware that the over voltage threshold must be set to the larger (that is, less negative) of the two values. The SOVL register is shown in Table 14.

**Table 14. SOVL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	SOVL	R/W	7FFFh	Sets the threshold for comparison of the value to detect Shunt Overvoltage (overcurrent protection). Two's complement value. Conversion Factor: 5 $\mu$ V/LSB when ADCRANGE = 0 1.25 $\mu$ V/LSB when ADCRANGE = 1.

#### 10.4.2.11 Shunt Undervoltage Threshold (SUVL) Register (Address = Dh) [reset = 8000h]

The SUVL register is shown in Table 15.

**Table 15. SUVL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	SUVL	R/W	8000h	Sets the threshold for comparison of the value to detect Shunt Undervoltage (undercurrent protection). Two's complement value. Conversion Factor: 5 $\mu$ V/LSB when ADCRANGE = 0 1.25 $\mu$ V/LSB when ADCRANGE = 1.

#### 10.4.2.12 Bus Overvoltage Threshold (BOVL) Register (Address = Eh) [reset = 7FFFh]

The BOVL register is shown in Table 16

**Table 16. BOVL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads 0.
14-0	BOVL	R/W	7FFFh	Sets the threshold for comparison of the value to detect Bus Overvoltage (overvoltage protection). Unsigned representation, positive value only. Conversion factor: 3.125 mV/LSB.

#### 10.4.2.13 Bus Undervoltage Threshold (BUVL) Register (Address = Fh) [reset = 0h]

The BUVL register is shown in Table 17

**Table 17. BUVL Register Field Descriptions**

Bit	Field	Type	Reset	Description
15	Reserved	R	0h	Reserved. Always reads 0.
14-0	BUVL	R/W	0h	Sets the threshold for comparison of the value to detect Bus Undervoltage (undervoltage protection). Unsigned representation, positive value only. Conversion factor: 3.125 mV/LSB.

#### 10.4.2.14 Temperature Over-Limit Threshold (TEMP\_LIMIT) Register (Address = 10h) [reset = 7FFFh]

The TEMP\_LIMIT register is shown Table 18

**Table 18. TEMP\_LIMIT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-4	TOL	R/W	7FFh	Sets the threshold for comparison of the value to detect over temperature measurements. Two's complement value. The value entered in this field compares directly against the value from the DIETEMP register to determine if an over temperature condition exists. Conversion factor: 125 m°C/LSB.
3-0	Reserved	R	0	Reserved, always reads 0

**10.4.2.15 Power Over-Limit Threshold (PWR\_LIMIT) Register (Address = 11h) [reset = FFFFh]**

The PWR\_LIMIT register is shown in Table 19

**Table 19. PWR\_LIMIT Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	POL	R/W	FFFFh	Sets the threshold for comparison of the value to detect power over-limit measurements. Unsigned representation, positive value only. The value entered in this field compares directly against the value from the POWER register to determine if an over power condition exists. Conversion factor: $256 \times$ Power LSB.

**10.4.2.16 Manufacturer ID (MANUFACTURER\_ID) Register (Address = 3Eh) [reset = 5959h]**

The MANUFACTURER\_ID register is shown in Table 20.

**Table 20. MANUFACTURER\_ID Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-0	MANFID	R	5959h	Reads in ASCII.

**10.4.2.17 Device ID (DEVICE\_ID) Register (Address = 3Fh) [reset = 2380h]**

The DEVICE\_ID register is shown in Table 21

**Table 21. DEVICE\_ID Register Field Descriptions**

Bit	Field	Type	Reset	Description
15-4	DIEID	R	238h	Stores the device identification bits.
3-0	REV_ID	R	0h	Device revision identification.

## 11 Application and Implementation

### 11.1 Device Measurement Range and Resolution

The PJ75238 device supports two input ranges for the shunt voltage measurement. The supported full scale differential input across the IN+ and IN– pins can be either  $\pm 163.84$  mV or  $\pm 40.96$  mV depending on the ADCRANGE bit in CONFIG register. The range for the bus voltage measurement is from 0 V to 85 V. The internal die temperature sensor range extends from  $-256$  °C to  $+256$  °C but is limited by the package to  $-40$  °C to  $125$  °C.

Table 22 provides a description of full scale voltage on shunt, bus, and temperature measurements, along with their associated step size.

**Table 22 . ADC Full Scale Values**

Parameter	Full-Scale Value	Resolution
Shunt voltage	$\pm 163.84$ mV (ADCRANGE = 0)	5 $\mu$ V/LSB
	$\pm 40.96$ mV (ADCRANGE = 1)	1.25 $\mu$ V/LSB
Bus voltage	0 V to 85 V	3.125 mV/LSB
Temperature	$-40$ °C to $+125$ °C	125 m°C/LSB

The device shunt voltage measurements, bus voltage, and temperature measurements can be read through the VSHUNT, VBUS, and DIETEMP registers, respectively. The digital output in VSHUNT and VBUS registers is 16-bits. The shunt voltage measurement can be positive or negative due to bidirectional currents in the system; therefore the data value in VSHUNT can be positive or negative. The VBUS data value is always positive. The output data can be directly converted into voltage by multiplying the digital value by its respective resolution size. The digital output in the DIETEMP register is 12-bit and can be directly converted to °C by multiplying by the above resolution size. This output value can also be positive or negative.

Furthermore, the device provides the flexibility to report calculated current in Amperes, power in Watts as described in Section 11.2.

### 11.2 Current and Power Calculations

For the PJ75238 device to report current values in Ampere units, a constant conversion value must be written in the SHUNT\_CAL register that is dependent on the maximum measured current and the shunt resistance used in the application. The SHUNT\_CAL register is calculated based on Equation 1. The term CURRENT\_LSB is the LSB step size for the CURRENT register where the current in Amperes is stored. The value of CURRENT\_LSB is based on the maximum expected current as shown in Equation 2, and it directly defines the resolution of the CURRENT register. While the smallest CURRENT\_LSB value yields highest resolution, it is common to select a higher round-number (no higher than 8x) value for the CURRENT\_LSB in order to simplify the conversion of the CURRENT.

The  $R_{SHUNT}$  term is the resistance value of the external shunt used to develop the differential voltage across the IN+ and IN– pins. Use Equation 1 for ADCRANGE = 0. For ADCRANGE = 1, the value of SHUNT\_CAL must be multiplied by 4.

$$SHUNT\_CAL = 819.2 \times 10^6 \times CURRENT\_LSB \times R_{SHUNT} \quad (1)$$

where

- 819.2 x 106 is an internal fixed value used to ensure scaling is maintained properly.
- the value of SHUNT\_CAL must be multiplied by 4 for ADCRANGE = 1

$$Current\_LSB = \frac{\text{Maximum Expected Current}}{2^{15}} \quad (2)$$

Note that the current is calculated following a shunt voltage measurement based on the value set in the SHUNT\_CAL register. If the value loaded into the SHUNT\_CAL register is zero, the current value reported through the CURRENT register is also zero.

After programming the SHUNT\_CAL register with the calculated value, the measured current in Amperes can be read from the CURRENT register. The final value is scaled by CURRENT\_LSB and calculated in Equation 3:

$$\text{Current [A]} = \text{CURRENT\_LSB} \times \text{CURRENT} \quad (3)$$

where

- CURRENT is the value read from the CURRENT register

The power value can be read from the POWER register as a 24-bit value and converted to Watts by using Equation 4:

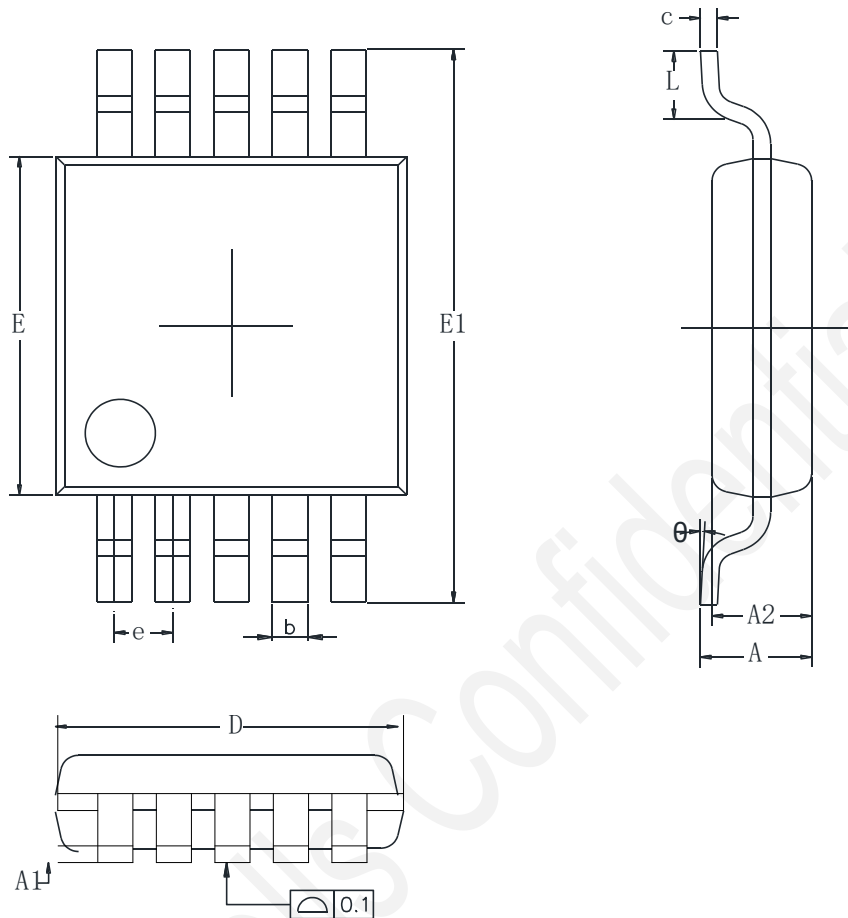
$$\text{Power [W]} = 0.2 \times \text{CURRENT\_LSB} \times \text{POWER} \quad (4)$$

Where

- POWER is the value read from the POWER register.
- CURRENT\_LSB is the lsb size of the current calculation as defined by Equation 2.

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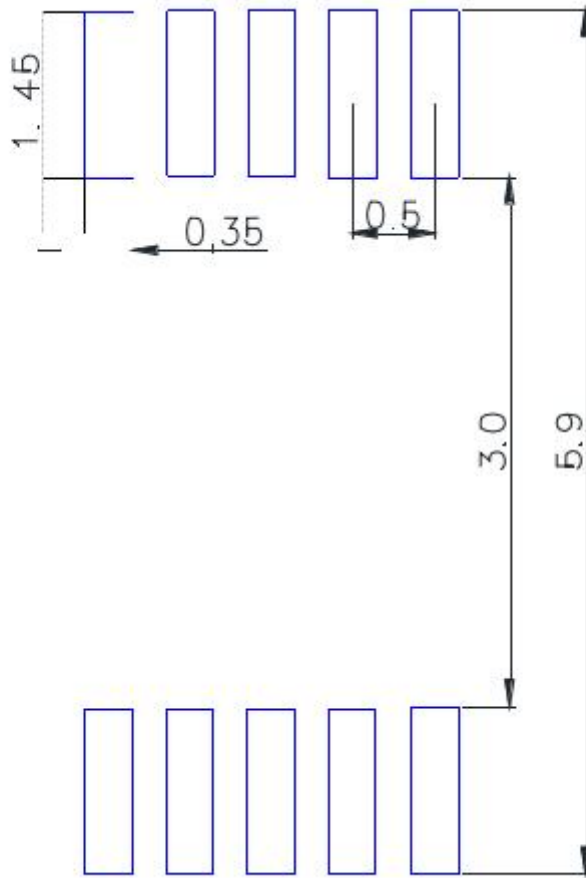
## 12 Package Outline Dimensions (MSOP-10)

**MSOP-10 Unit (mm)**


Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.250	0.004	0.010
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.700	5.100	0.185	0.201
e	0.500 (BSC)		0.020 (BSC)	
L	0.400	0.800	0.016	0.031
θ	0°	8°	0°	8°

**12.1 Recommend Land Pattern Layout (MSOP-10)**

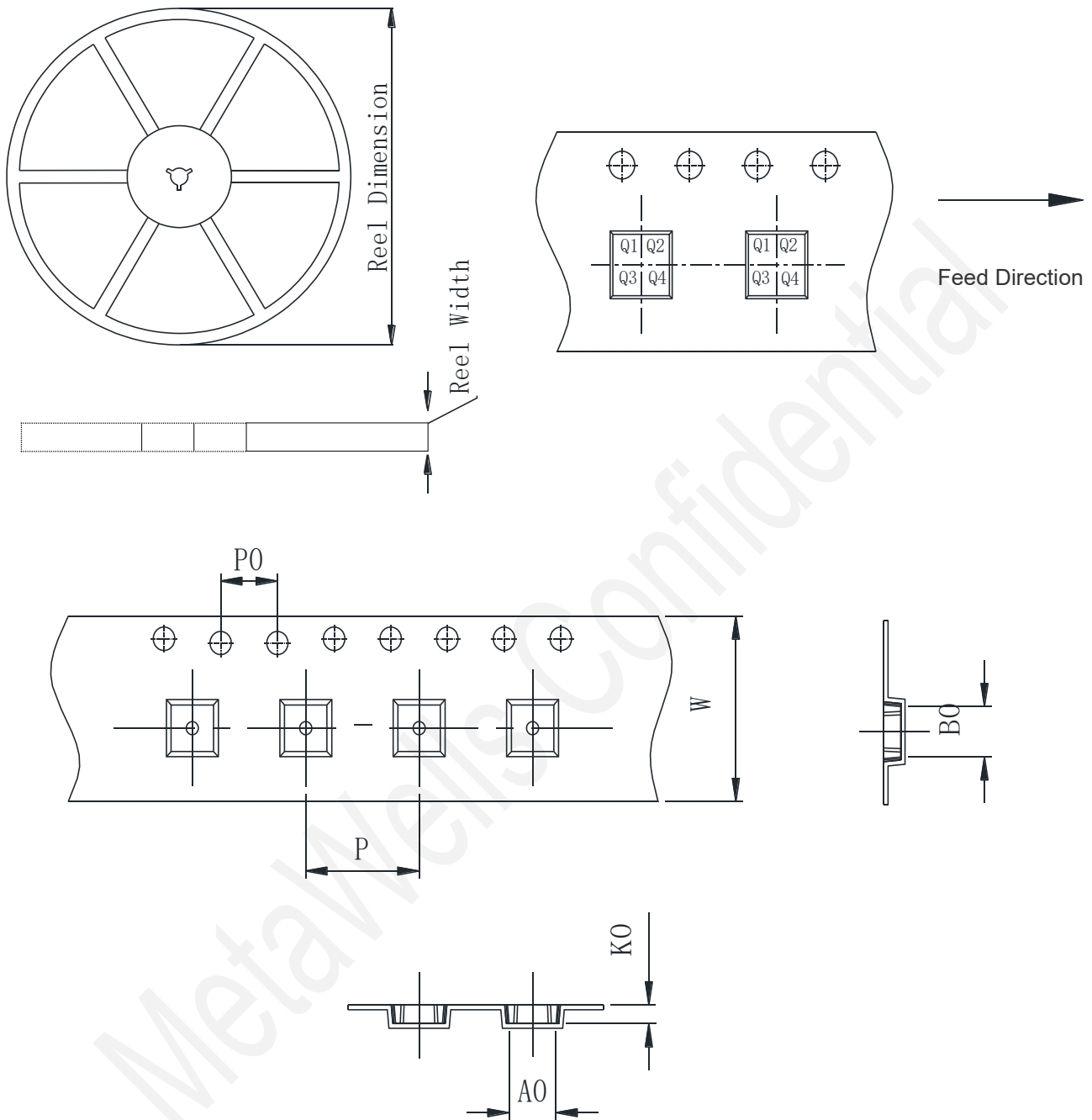
MSOP-10 Unit (mm)



Note:

1. All dimensions are in millimeter.
2. Recommend tolerance is within  $\pm 0.1\text{mm}$ .
3. Change without notice.

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**12.2 Packing information**


Package type	Reel size	Reel dimension (±3.0mm)	Reel width (±1.0mm)	A0 (±0.1mm)	B0 (±0.1mm)	K0 (±0.1mm)	P (±0.1mm)	P0 (±0.1mm)	W (±0.3mm)	Pin1
MSOP-10	13'	330	12.4	5.2/5.4	3.3/3.4	1.5/1.4	8.0	4.0	12.0	Q1

## 13 Version History

Version	Date	Changes
P0.1	2025-09-11	Initial release

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