PJ77204 Datasheet

4-channel Auto-Bidirectional Multi-Voltage Level Translator

Version：Rev.1.0

Release Date：2026-03-19

MetaWells Co., Ltd.

www.metawells.com

Contents

1 General Description

The PJ77204 supports bidirectional voltage translation without direction pin which minimizes system effort (for PMBus, I2C, SMBus or I3C, etc.). The PJ77204 supports up to 100MHz up translation and greater than 100MHz down translation at ≤ 30pf cap load and up to 40MHz up/down translation at 50pf cap load which allows the PJ77204 to support more consumer or telecom interfaces (MDIO or SDIO).

PJ77204 supports 5V tolerance on I/O port which makes it compatible with TTL levels in industrial and telecom applications. The PJ77204 is able to set up different voltage translation levels on each channel which makes it very flexible.

Available Package:

TSSOP-14 QFN2x1.7-12

2 Features

- Provides bidirectional voltage translation with no direction pin
- Supports up to 100MHz up translation and greater than 100MHz down translation at ≤ 30pf cap load and up to 40MHz up/down translation at 50pf cap load
- Allows voltage-level translation between
  - 0.85V and 1.8V, 2.5V, 3.3V, or 5V
  - 1.2V and 1.8V, 2.5V, 3.3V, or 5V
  - 1.8V and 2.5V, 3.3V, or 5V
  - 2.5V and 3.3V, or 5V
  - 3.3V and 5V
- Low standby current
- 5V tolerance I/O port to support TTL
- Low Ron provides less signal distortion
- High-impedance I/O pins for EN = Low
- Flow-through pinout for easy PCB trace routing
- Latch-up performance >200mA per JESD 17
- -40°C to 125°C Operating temperature range

3 Applications

- GPIO, MDIO, PMBus, SVID, UART, I2C, I3C

4 Ordering Information

4.1 Ordering Information

Order number	Marking ID	Package	MSL	Description
PJ77204B	77204 YMDNN	TSSOP-14	Level-3	Halogen free RoHS compliant in T/R, 4,000 pcs/Reel
PJ77204QW	A1W	QFN2X1.7-12	Level-3	Halogen free RoHS compliant in T/R, 4,000 pcs/Reel

Note:

(1) MetaWells can meet RoHS 2.0/REACH requirement. So most package types MetaWells offers only states halogen free, instead of lead free.

4.2 Marking Information

Marking	Package	Definition
77204 YMDNN	TSSOP-14	77204:Product code YMDNN : Y : Year code M : Month code D : Day code; NN: Serial Number
A1W	QFN2X1.7-12	A1:Product code ;W: Week code

5 Typical Application

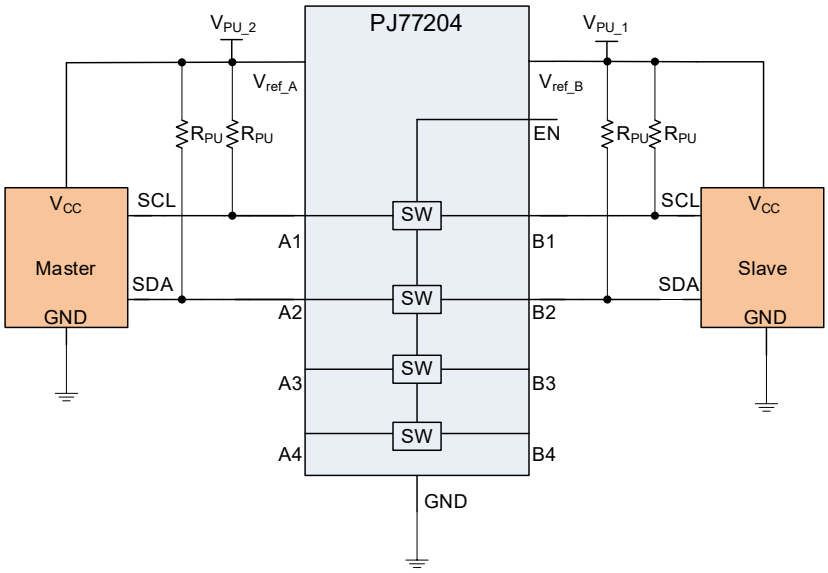


Figure 1 Typical Application Circuit

(1) For better translator operation, the Vref_B at least 1V higher than Vref_A.

6 Function Block

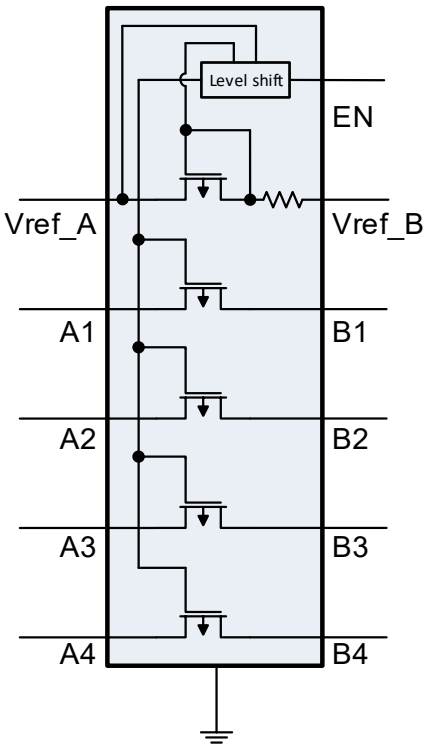
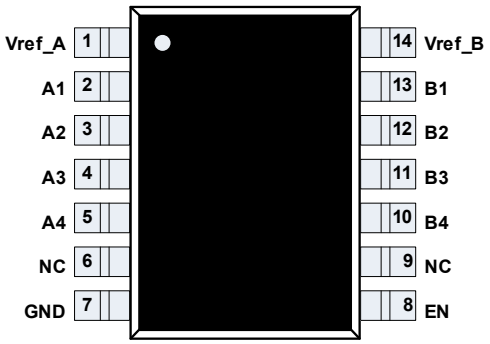
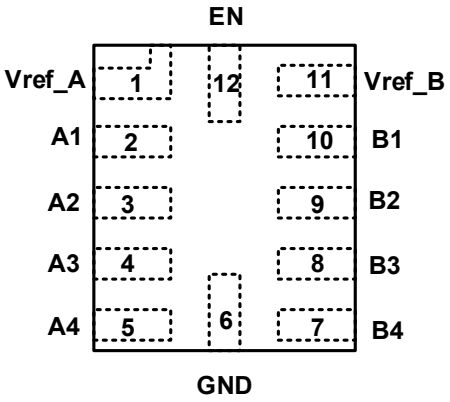


Figure 2 Function Block

7 Pin Configuration



TSSOP-14
(Package Code B)



QFN2x1.7-12
(Package Code QW)

8 Pin Description

PIN			Description
Name	TSSOP-14	QFN2x1.7-12	
Vref_A	1	1	A-port reference supply voltage, Power
A1	2	2	Input/output 1 of A port, I/O
A2	3	3	Input/output 2 of A port, I/O
A3	4	4	Input/output 3 of A port, I/O
A4	5	5	Input/output 4 of A port, I/O
NC	6,9		No connection
GND	7	6	GND
EN	8	12	Enable, high active. Input
B4	10	7	Input/output 4 of B port, I/O
B3	11	8	Input/output 3 of B port, I/O
B2	12	9	Input/output 2 of B port, I/O
B1	13	10	Input/output 1 of B port, I/O
Vref_B	14	11	B-port reference supply voltage, Power

9 Specification

9.1 Absolute Maximum Ratings[1]

Parameter	Symbol	Value	Unit
Input voltage[2]	V_I	-0.5 to 7	V
Input/output voltage[2]	$V_{I/O}$	-0.5 to 7	V
Max continuous channel current		128	mA
Input clamp current	I_IK	-50	mA
Maximum Junction Temperature	T_{jmax}	150	°C
Storage Temperature Range	T_{stg}	-65~150	°C
ESD HBM	ESD_HBM	±4000	V
ESD CDM	ESD_CDM	±1000	V

(1) Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at the "Absolute Maximum Ratings" conditions or any other conditions beyond those indicated under "Recommended Operating Conditions" is not recommended. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

9.2 Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Input/output Voltage	$V_{I/O}$	0 to 5.5	V
Reference Voltage A	Vref_A	0 to 5.5	V
Reference Voltage B	Vref_B	0 to 5.5	V
Enable input Voltage	EN	0 to 5.5	V
Max pass Switch Current	I_PASS	64	mA
Operating Ambient Temperature	T_A	-40~125	°C

9.3 Electrical Characteristics

Over recommended operating ambient temperature range (unless otherwise noted).
All limits are 100% tested at T_A=-40 to 125°C.

Parameter	Symbol	Test conditions	MIN	TYP	MAX	Unit
Input Clamp Voltage	V_IK	I_I = –18mA, EN = 0V	-1.2			V
Input Leakage Current	I_IH	V_I = 5V, EN = 0V			5	uA
Leakage from Vref_B to Vref_A	Icc_BA	Vref_B=3.3V, Vref_A=1.8V, V_{EN} = Vref_A, I_O = 0, V_I = 3.3 V or GND			3.5	uA
Total Current through GND	Icc_A+Icc_B	Vref_B=3.3V, Vref_A=1.8V, V_{EN} = Vref_A, I_O = 0, V_I = 3.3 V or GND		0.2		uA
Control pin current	I_IN	Vref_B=5.5V, Vref_A=4.5V, V_{EN} = 0 to Vref_A, I_O = 0			±1	uA
Power off leakage current	Ioff	Vref_B=Vref_A=0V, V_{EN} = GND, I_O = 0, V_I = 5V or GND			±1	uA
Input Capacitance	Ci_(ref_A/ref_B)	V_I = 3V or 0		17		pf
Input Capacitance	Ci_(EN)	V_I = 3V or 0		7		pf
Off Capacitance	$C_{io(off)}$	V_O = 3V or 0, EN = 0V		3	6	pf
On Capacitance	$C_{io(on)}$	V_O = 3V or 0, EN = 3V		10	13	pf
High-level input voltage	V_IH(EN)	Vref_A=1V to 1.5V	0.8×Vref_ A			V
		Vref_A=1.5V to 4.5V	0.7×Vref_ A			V
Low-level input voltage	V_IL(EN)	Vref_A=1V to 4.5V			0.3×Vref_ A	V
Input transition rise or fall rate for EN pin	Δt/Δv(EN)			10		ns/V
On-state resistance	R_{on}	V_I = 1.0V, I_O =10mA, EN = Vref_A=1.8V,Vref_B=3.3V		8	20	ohm
		V_I = 0, I_O =10mA, EN = Vref_A=1V Vref_B=1.8V		6	15	ohm
		V_I = 0, I_O =10mA, EN = Vref_A=1V Vref_B=3.3V		6	15	ohm
		V_I = 1.8V, I_O =15mA, EN = Vref_A=3.3V,Vref_B=5V		5	10	ohm
		V_I = 0, I_O =32mA, EN = Vref_A=2.5V Vref_B=5V		4	8	ohm
		V_I = 0, I_O =64mA, EN = Vref_A=3.3V Vref_B=5V		3	6	ohm
		V_I = 0, I_O =64mA, EN = Vref_A=1.8V Vref_B=5V		4	10	ohm
		V_I = 0, I_O =32mA, EN = Vref_A=1.0V Vref_B=5V		6	15	ohm
		V_I = 0, I_O =32mA, EN = Vref_A=1.8V Vref_B=5V		4	8	ohm

9.4 Interface Timing Requirements

9.4.1 Switching Characteristics AC Performance (Translating Down) (3.3V to 1.8V)[2]

Over recommended operating ambient temperature range, Vref_A=1.8V, Vref_B=3.3V, EN = 1.8V, Vpu_1=3.3V, Vpu_2=1.8V, R_L=NA, V_{IH} = 3.3V, V_{IL} = 0, V_M = 1.15V (unless otherwise noted) (see Figure 4).

Parameter	From (INPUT)	To (OUTPUT)	CL = 50pf		CL = 30pf		CL = 15pf		Unit
			TYP	MAX	TYP	MAX	TYP	MAX	
t_PLH	B	A	0.7	5.49	0.5	5.29	0.3	5.19	ns
t_PHL			0.9	4.9	0.7	4.7	0.5	4.5	ns
t_PLZ			13	18	12	16.5	11	15	ns
t_PZL			33	45	30	40	23	37	ns

9.4.2 Switching Characteristics AC Performance (Translating Down) (3.3V to 1.2V)[2]

Over recommended operating ambient temperature range, Vref_A=1.2V, Vref_B=3.3V, EN = 1.2V, Vpu_1=3.3V, Vpu_2=1.2V, R_L=NA, V_{IH} = 3.3V, V_{IL} = 0, V_M = 0.85V (unless otherwise noted) (see Figure 4).

Parameter	From (INPUT)	To (OUTPUT)	CL = 50pf		CL = 30pf		CL = 15pf		Unit
			TYP	MAX	TYP	MAX	TYP	MAX	
t_PLH	B	A	0.8	8	0.5	3.9	0.3	3.8	ns
t_PHL			0.9	4.7	0.7	4.5	0.6	4.3	ns

9.4.3 Switching Characteristics AC Performance (Translating Up) (1.8V to 3.3V)[1]

Over recommended operating ambient temperature range,Vref_A=1.8V, Vref_B=3.3V, EN = 1.8V, Vpu_1=3.3V, Vpu_2=1.8V, R_L=500ohm, V_{IH} = 1.8V, V_{IL} = 0, V_M = 0.9V (unless otherwise noted) (see Figure 4)

Parameter	From (INPUT)	To (OUTPUT)	CL = 50pf		CL = 30pf		CL = 15pf		Unit
			TYP	MAX	TYP	MAX	TYP	MAX	
t_PLH	A	B	0.6	5.7	0.4	5.3	0.2	5.13	ns
t_PHL			7	12	5	10	0.7	5.3	ns
t_PLZ			13	18	12	16.5	11	15	ns
t_PZL			33	45	30	40	23	37	ns

9.4.4 Switching Characteristics AC Performance (Translating Up) (1.2V to 1.8V)[1]

Over recommended operating ambient temperature range,Vref_A=1.2V, Vref_B=1.8V, EN = 1.2V, Vpu_1=1.8V, Vpu_2=1.2V, R_L=500ohm, V_{IH} = 1.2V, V_{IL} = 0, V_M = 0.6V (unless otherwise noted) (see Figure 4)

Parameter	From (INPUT)	To (OUTPUT)	CL = 50pf		CL = 30pf		CL = 15pf		Unit
			TYP	MAX	TYP	MAX	TYP	MAX	
t_PLH	A	B	0.65	7.25	0.4	7.05	0.2	6.85	ns
t_PHL			10	15	8	12	6	10	ns

(1) Translating up: the low-voltage side driving toward the high-voltage side.

(2) Translating down: the high-voltage side driving toward the low-voltage side.

10 Detailed Descriptions

10.1 Overview

The PJ77204 supports bidirectional voltage translation without the direction pin which minimizes system effort (for PMBus, I2C, I3C, SMBus, etc.). The PJ77204 supports up to 100MHz up translation and greater than 100MHz down translation at ≤ 30pf cap load and up to 40MHz up/down translation at 50pf cap load which allows the PJ77204 to support more consumer or telecom interfaces (MDIO or SDIO).

PJ77204 supports 5V tolerance on I/O port which makes it compatible with TTL levels in industrial and telecom applications. The PJ77204 is able to set up different voltage translation levels on each channel which makes it very flexible.

10.2 Auto Bidirectional Voltage Translation

The PJ77204 supports auto bidirectional voltage level translation that operational from 0.85 to 4.5V on the Vref_A supply and from 1.8 to 5.5V on the Vref_B supply. This allows bidirectional voltage translation between 0.95V and 5.5V without a direction pin in open-drain or push-pull applications. The PJ77204 also supports level translation applications with transmission speeds greater than 100Mbps for open-drain systems using a 30pf capacitance and 250ohm pull-up resistor.

This document references a threshold voltage denoted as Vth, which appears multiple times throughout this document when discussing the NFET between Vref_A and Vref_B. The value of Vth is approximately 0.6V at room temperature.

10.3 Device Functional Modes

For each channel (n), when either the An or Bn port is LOW, the switch provides a low impedance path between the An and Bn ports; the corresponding Bn or An port will be pulled LOW. The low Ron of the switch allows connections to be made with minimal propagation delay and signal distortion.

When the signal is being driven from Bn to An and the Bn port is driven HIGH, the switch will be OFF, clamping the voltage on the An port to the voltage set by Vref_A. When the signal is being driven from A to B and the An port is HIGH, the switch will be OFF and the Bn port will then be driven to a voltage higher than Vref_A by the pull-up resistor that is connected to the pull-up supply voltage. This functionality allows seamless translation between higher and lower voltages selected by the user, without the need for directional control.

When EN is HIGH, the translator switch is on, and the An I/O is connected to the Bn I/O, respectively, allowing bidirectional data flow between ports. When EN is LOW, the translator switch is off, and a high impedance state exists between ports. The EN input circuit is designed to be supplied by Vref_A. EN must be LOW to ensure the high impedance state during power-up or power-down.

10.4 Load Circuit for Output

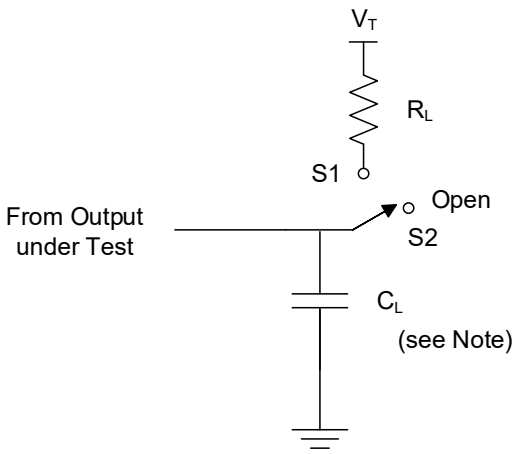
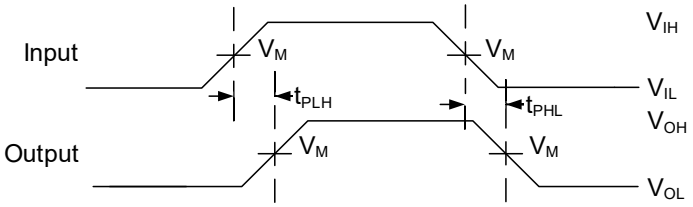
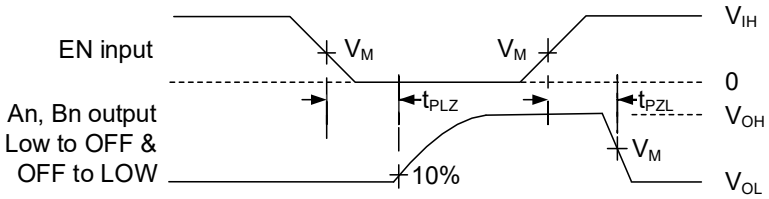


Figure 3 Load Circuit

10.5 Propagation Delay



(a) data input (An, Bn) to output (Bn, An)



(b) enable input (EN) to output (An, Bn)

Figure 4 Propagation Delay Timing

Notes:

(1) C_L includes probe and jig capacitance.

(2) All input pulses are supplied by generators having the following characteristics: PRR ≤10 MHz, ZO = 50 ohm, tr ≤ 2 ns, tf ≤ 2 ns.

(3) The outputs are measured one at a time, with one transition per measurement.

10.6 Application Curve

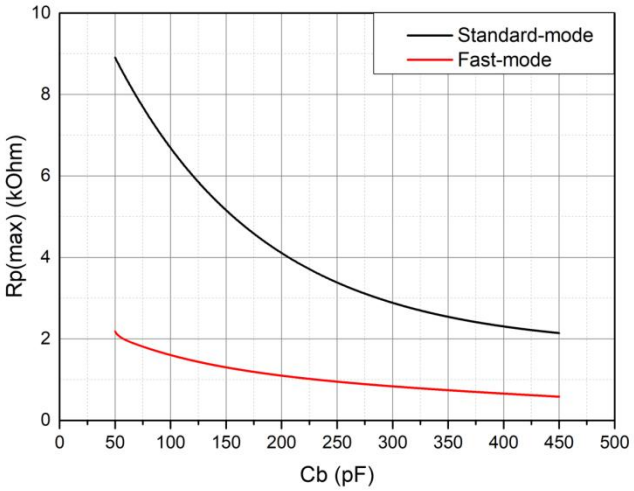


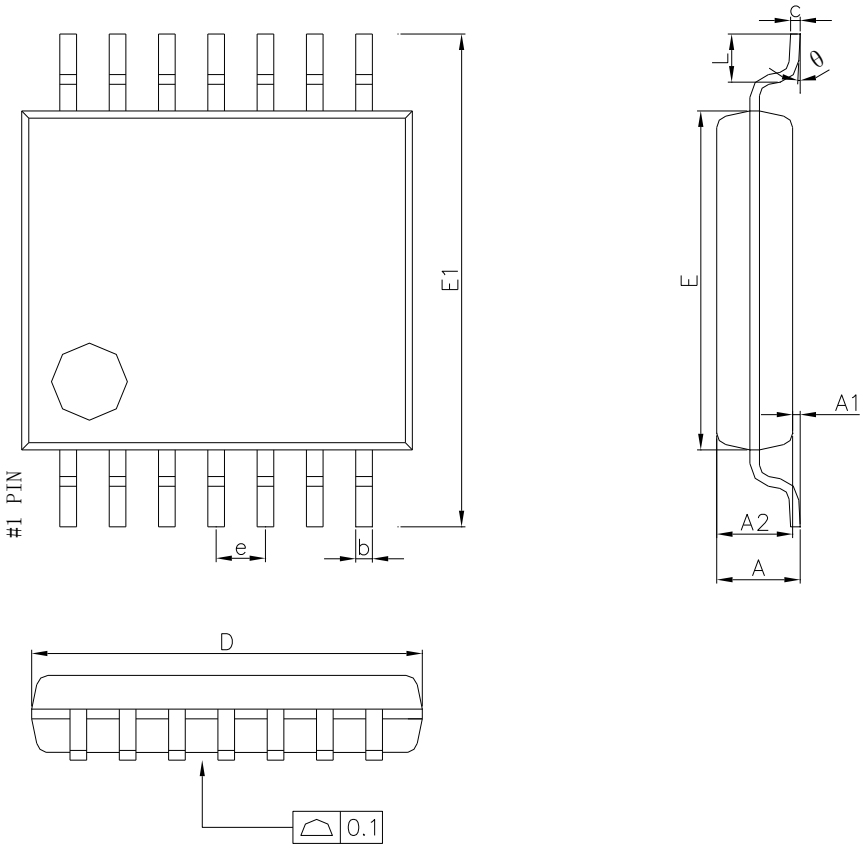
Figure 5 Maximum Pull-up Resistance (Rp(max)) vs Bus Capacitance (Cb)

11 Package Outline Dimensions and Recommend Land Pattern Layout

11.1 TSSOP-14

Package Outline Dimensions

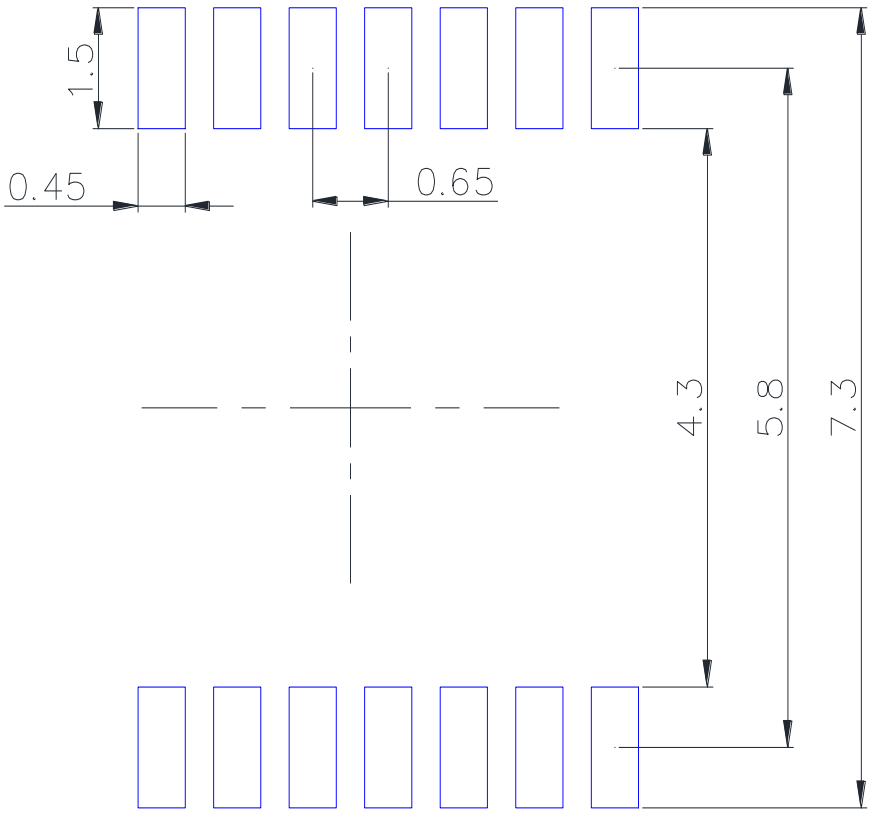
TSSOP-14 Unit (mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A		1.200		0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
C	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	4.300	4.500	0.169	0.177
E1	6.200	6.600	0.244	0.260
e	0.650(BSC)		0.026(BSC)	
L	0.400	0.800	0.016	0.031
θ	0°	8°	0°	8°

Recommend Land Pattern Layout

TSSOP-14 Unit (mm)



Notes:

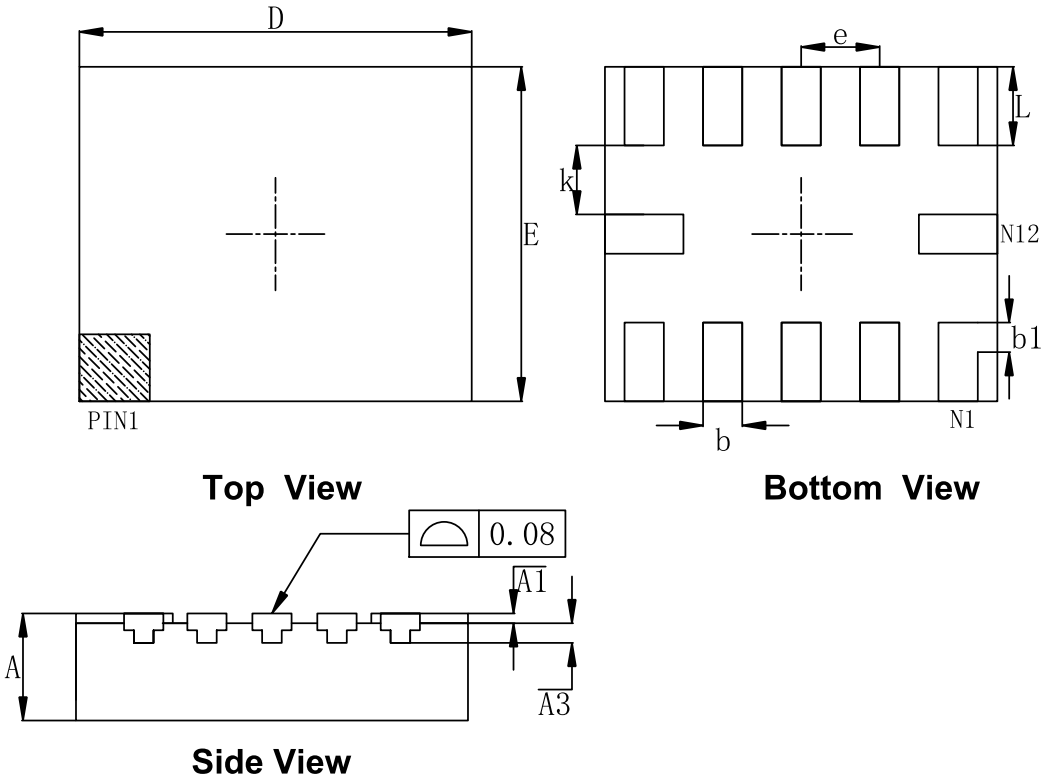
(1) All dimensions are in millimeter

(2) Recommend tolerance is within ±0.1mm

11.2 QFN2x1.7-12

Package Outline Dimensions

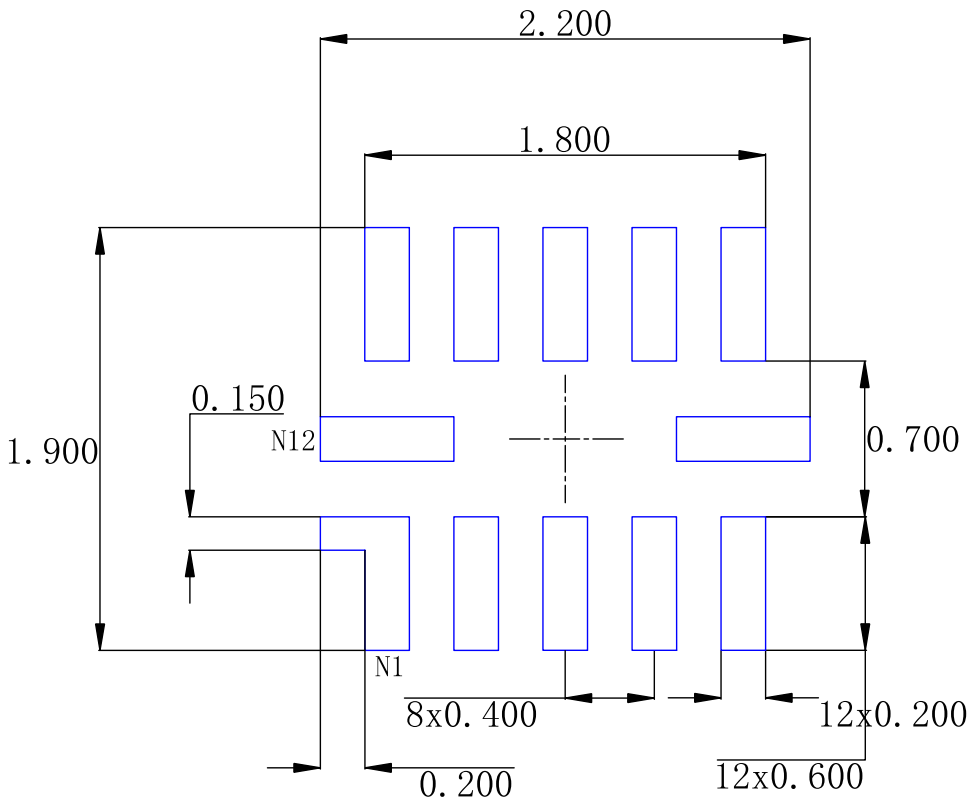
QFN2x1.7-12 Unit (mm)



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.000	0.050	0.000	0.002
A3	0.152REF		0.006REF	
E	1.600	1.800	0.063	0.071
D	1.900	2.100	0.075	0.083
b	0.150	0.250	0.006	0.010
b1	0.150REF		0.006REF	
k	0.250REF		0.010REF	
e	0.400BSC		0.016BSC	
L	0.400	0.600	0.016	0.024

Recommend Land Pattern Layout

QFN2x1.7-12 Unit (mm)

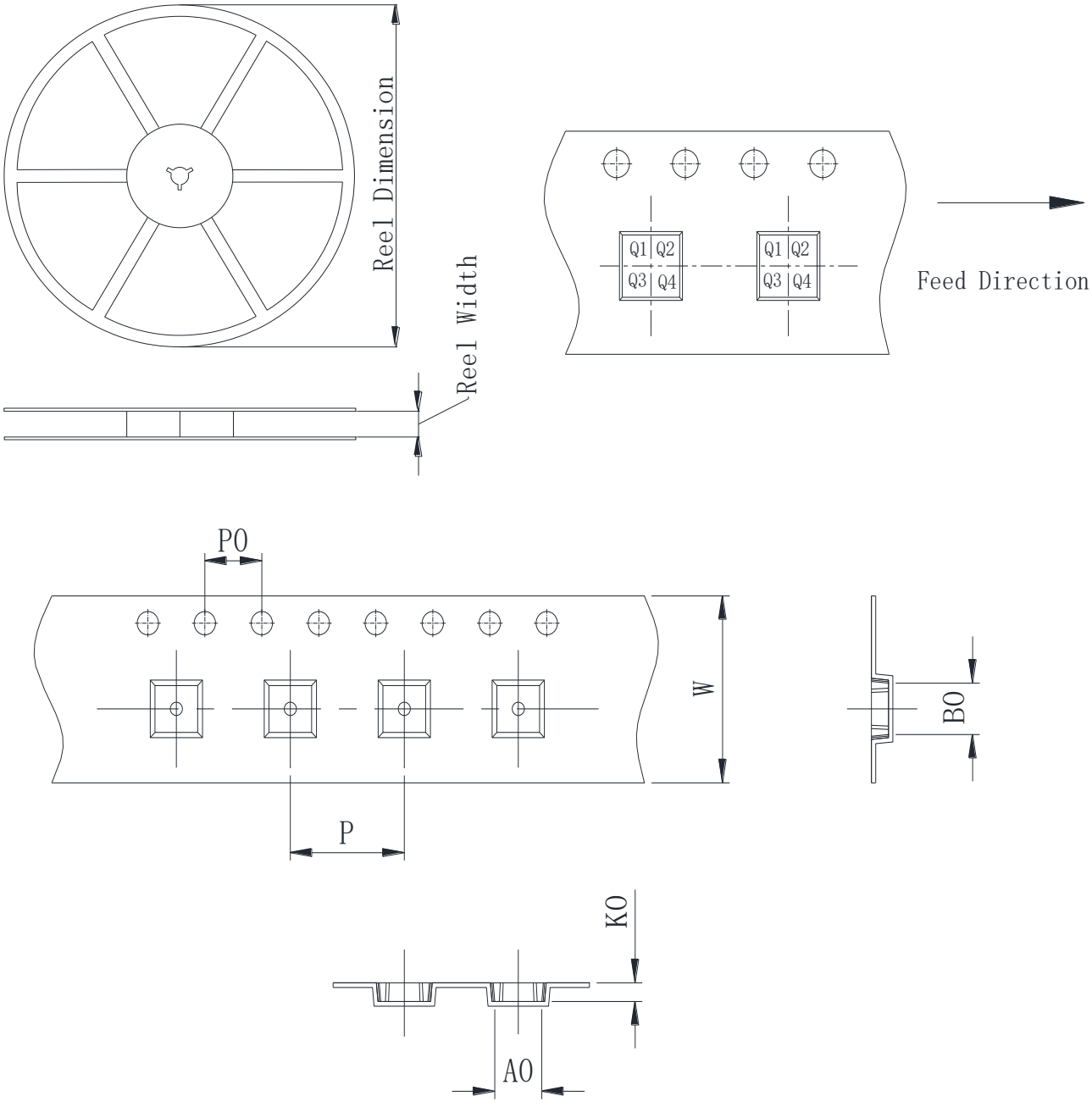


Notes:

(1) All dimensions are in millimeter

(2) Recommend tolerance is within ±0.1mm

12 Packing information



Package type	Reel size	Reel dimension (±3.0mm)	Reel width (±1.0mm)	A0 (±0.1mm)	B0 (±0.1mm)	K0 (±0.1mm)	P (±0.1mm)	P0 (±0.1mm)	W (±0.3mm)	Pin1
TSSOP-14	13'	330	12.4	6.8	5.4	1.2/1.3	8.0	4.0	12.0	Q1
QFN2x1.7-12	7'	180	9.5	1.9	2.3	0.75	4.0	4.0	8.0	Q1

13 Version History

Version	Date	Changes
Rev.1.0	2026-03-19	Initial release

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