PMC8000B Datasheet

15-Channel ADC Featuring I2C Interface

Version：Rev.1.0

Release Date：2026-04-15

MetaWells Co., Ltd.

www.metawells.com

General Description

The PMC8000B is an 8-bit precision analog-to-digital converter (ADC) designed for temperature sensing applications using external NTC thermistors with high accuracy, low power operation, and easy system integration, and its communication interface is I2C.

The PMC8000B provides up to 15 voltage-sensing inputs for temperature monitoring applications. It reads the voltage across an NTC resistor divider referenced to ground, digitizes the sensed values, and transfers the data to a microprocessor over the I²C bus to support advanced power-management functions.

The PMC8000B operates from a single supply voltage of 2.8V to 5.5V and is available in a compact WQFN 3×3-20 pin package.

Features

- Operation Voltage : 2.8 V to 5.5 V
- Low operating current: 100 μA (typical)
- 15-Ch Analog Voltage Input: VI1, VI2, VI3, VI4, VI5, VI6, VI7, VI8, VI9, VI10, VI11, VI12, VI13, VI14, VI15.
- Pin 4 selects the ADC accuracy and full-scale input range configuration.
- High-accuracy nonlinearity:
  - ±1.5LSB when Pin 4 is tied to GND
  - ±3LSB when Pin 4 is connected to GND through a resistor ≥10 kΩ
- ADC full-scale input range:
  - 1.0 V to 3.56 V when Pin 4 is tied to GND
  - 0 V to 2.56 V when Pin 4 is connected to GND through a resistor ≥10 kΩ
- High Accuracy A/D Resolution: 10mV/LSB
- Built-in Alert Flag Functions
- Built-in I2C Address Programming Functions
- Temperature Range: -40°C to 125°C

Applications

- Phone & NB Application
- Temperature Measurement
- Portable Instrumentation
- Consumer Goods

Ordering Information

Ordering Information

Order number	Marking ID	Package	Description
PMC8000BQLF	8000B YMDNN	WQFN3X3-20	Halogen free RoHS compliant in T/R,3,000 pcs/Reel

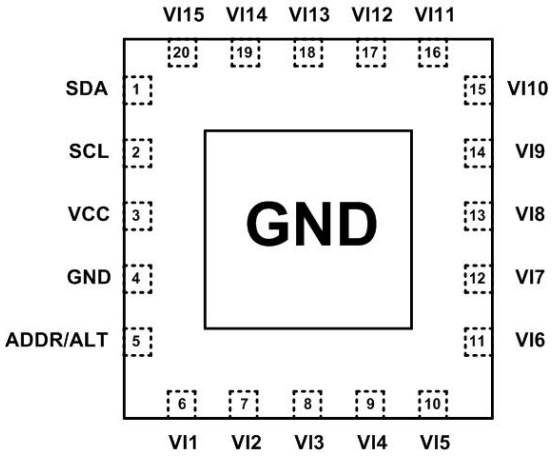
Note:

(1) MetaWells can meet RoHS 2.0/REACH requirement. So most package types MetaWells offers only states halogen free, instead of lead free.

Marking Information

Marking	Package	Definition
8000B YMDNN	WQFN3X3-20	8000B: Product code Y: Year code; M: Month code; D: Date code; NN: Serial number

Pin Configuration



WQFN 3x3-20P (Top View)

Pin Functions

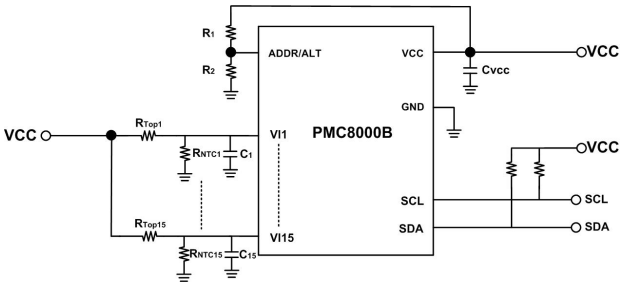
Pin		Function
Num	Name	
1	SDA	Digital interface data input or output pin, need a pull-up resistor to VCC.
2	SCL	Digital interface clock input pin, need a pull-up resistor to VCC.
3	VCC	PMC8000B power-supply pin; connect a 0.1 μF decoupling capacitor.
4	GND	PMC8000B Ground pin.
5	ADDR/ALT	Address Selection and Alert Function. A resistor-divider network is used to set the ADC's I²C address. After the ADDR value is configured, if any VIx input falls below its programmed threshold, the device generates an alert by pulling this pin low. This pin must not be connected to a capacitor and must not be left floating. External capacitance on the ADDR/ALT pin may distort the alert pulse waveform and is therefore not recommended.
6	VI1	Analog Voltage Input 1.
7	VI2	Analog Voltage Input 2.
8	VI3	Analog Voltage Input 3.
9	VI4	Analog Voltage Input 4.
10	VI5	Analog Voltage Input 5.
11	VI6	Analog Voltage Input 6.
12	VI7	Analog Voltage Input 7.
13	VI8	Analog Voltage Input 8.
14	VI9	Analog Voltage Input 9.
15	VI10	Analog Voltage Input 10.
16	VI11	Analog Voltage Input 11.
17	VI12	Analog Voltage Input 12.
18	VI13	Analog Voltage Input 13.
19	VI14	Analog Voltage Input 14.
20	VI15	Analog Voltage Input 15.

Application Schematic

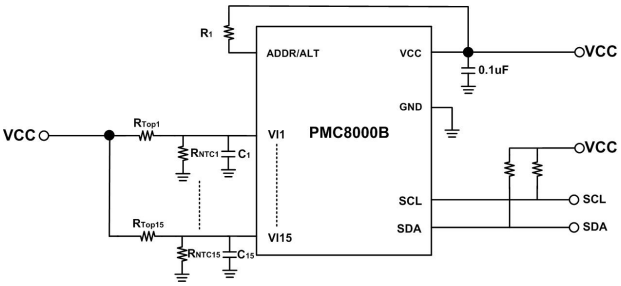
(1) **Typical Application Circuit**

Pin4 is GND.

The I2C address is configured by the ADDR/ALT pin



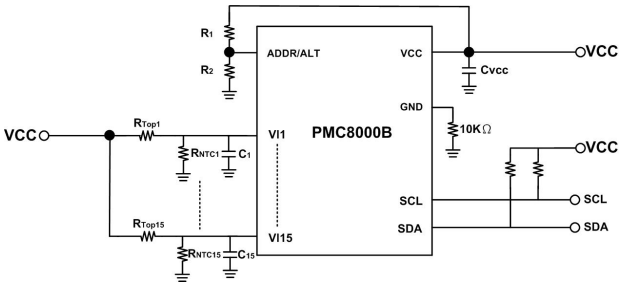
The default I2C address is applied



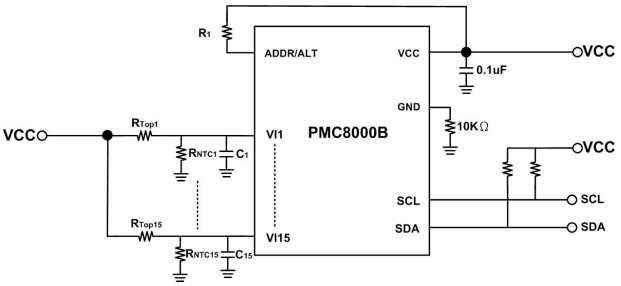
(2) **Typical Application Circuit**

Pin 4 is connected to GND through a 10 kΩ resister.

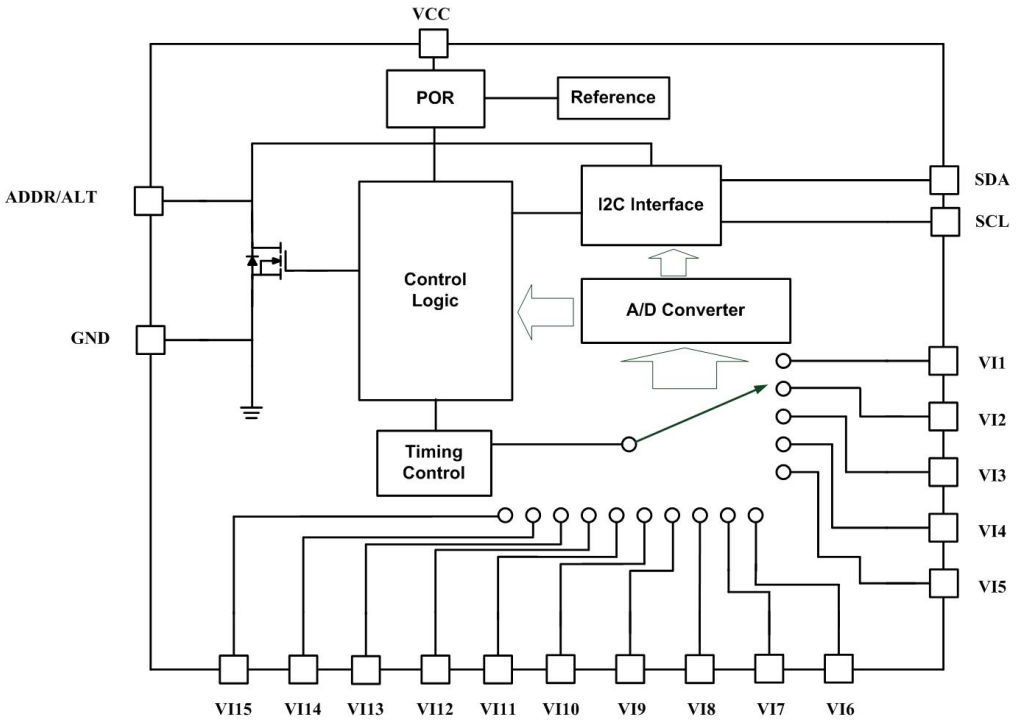
The I2C address is configured by the ADDR/ALT pin



The default I2C address is applied



Function Block



Absolute Maximum Ratings

Over operating free-air temperature range, unless otherwise noted.

Parameter		Min	Max	Units
VCC	PMC8000B Supply Voltage, VCC to GND	-0.3	6	V
VIx	VI1,VI2, VI3, VI4….VI15 Voltage	-0.3	VCC	V
Other Pins	SCL, SDA, ADDR/ALT	-0.3	VCC	V
T_{STG}	Storage Temperature Range	-65	150	°C
T_J	Operating junction temperature range	150		°C
T_{LEAD}	Lead Temperature (Soldering, 10 Seconds)	260		°C

Handling Ratings

Parameter	Definition	Min	Max	Units
ESD(1)	Human Body Model (HBM) ESD stress voltage(2)	-2	2	kV
	Machine Mode ESD stress voltage	-	0.2	kV
	Charged Device Model (CDM) ESD stress voltage(3), all pins	-1.5	1.5	kV

(1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges into the device.

(2) Level listed above is the passing level per ANSI, ESDA, and JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

Recommended Operating Conditions

Parameter		Min	Max	Units
VCC	Supply Voltage	2.8	5.5	V
VIx(a) (1)	VI1,VI2, VI3, VI4….VI15 Voltage	1	3.56	V
VIx(b) (1)	VI1,VI2, VI3, VI4….VI15 Voltage	0	2.56	V
Other Pins	SCL, SDA, ADDR/ALT	0	VCC	V
T_A	Operating Ambient temperature	-40	85	°C
T_J	Operating junction temperature range	-40	125	°C

(1) (a) is selected when Pin 4 is tied to GND. (b) is selected when Pin 4 is connected to GND through a 10 kΩ resistor.

(2) The VIx input voltage must not exceed the VCC supply voltage.

Electrical Characteristics

Test Condition: VCC = 5 V, TJ = -40 to 85°C, Typical values are at TJ = 25 °C, unless otherwise specified.

Parameter		Test Conditions	Min	Typ	Max	Units
Supply Input Voltage						
VCC	VCC Supply voltage range		2.8	-	5.5	V
VCC_{RTH}	VCC POR Threshold		2.3	2.5	2.7	V
VCC_{HYS}	VCC POR Hysteresis			0.3		V
Supply Current						
I_{VCC}	VCC Supply Current			80	100	μA
Voltage Monitor						
A/D	A/D Resolution			10		mV/LSB
	A/D Full Scale Range(a) (1)		1	-	3.56	V
	A/D Full Scale Range(b) (1)		0	-	2.56	V
	Input Bias Current		-	-	100	nA
	Differential nonlinearity(a) (1)		-	-	1.5	LSB
	Differential nonlinearity(b) (1)		-	-	3	LSB
	Integral nonlinearity(a) (1)		-	-	1.5	LSB
	Integral nonlinearity(b) (1)		-	-	3	LSB
	Vix(a) (1) Monitor time		0.48	0.6	0.72	mS
	Vix(b) (1) Monitor time		-	1.2	2.4	mS
Address Setting and Alert Output						
ADDR	Address Latch Time		-	-	10	mS
	Address 1 Voltage Range		92	95	100	
	Address 2 Voltage Range		82	85	88	%VCC
	Address 3 Voltage Range		72	75	78	%VCC
	Address 4 Voltage Range		**63**	65	68	%VCC
	Address 5 Voltage Range		52	55	58	%VCC
	Address 6 Voltage Range		42	45	48	%VCC
	Address 7 Voltage Range		32	35	38	%VCC
	Address 8 Voltage Range		22	25	28	%VCC
ALT	Alert Output Low Voltage	When Alert / ADDR pin pull low, IALT = 10mA	-	-	0.2	V
		When Alert/ADDR pin pull low, IALT = 50mA	-	-	0.8	V
ALT	Alert Pull Low Pulse Time		40	50	60	μS
	Alert Pull Low cycle Time		-	2	-	S
	Alert/ADDR Leakage Current		-	-	100	nA
I²C Interface						
F_{I2C}	I2C Clock Rate Range		1	400	440	KHz
V_{IH_I2C}	I2C Input High Voltage		1.4	-	-	V
V_{IL_I2C}	I2C Input Low Voltage		-	-	0.4	V

Parameter		Test Conditions	Min	Typ	Max	Units
I_{LKG_I2C}	I2C Leakage Current		0	-	100	nA
F_{I2C_CLK}	Frequency, SCL		-	-	400	KHz
$T_{CLK(H)}$	Pulse Duration, SCL High		600	-	-	nS
$T_{CLK(L)}$	Pulse Duration, SCL Low		1300	-	-	nS
T_R	Rise Time, SCL and SDA		20+0.1 CL(pF)	-	300	nS
T_F	Fall Time, SCL and SDA		20+0.1 CL(pF)	-	300	nS
T_{SETUP1}	Setup Time, SCL to SDA		100	-	-	nS
T_{HOLD1}	Hold Time, SCL to SDA		100	-	-	nS
T_{BUSFT}	Bus Free Time Between Stop and Start Condition		1300	-	-	nS
T_{SETUP2}	Setup Time, SCL to Start Condition		600	-	-	nS
T_{HOLD2}	Hold Time, Start condition to SCL		600	-	-	nS
T_{SETUP3}	Setup Time, SCL to Stop Condition		600	-	-	nS
C_L	Load Capacitance for Each Bus Line		-	-	400	pF

(1) (a) is selected when Pin 4 is tied to GND. (b) is selected when Pin 4 is connected to GND through a 10 kΩ resistor.

(2) All devices are 100% production tested at TA = +25°C; all specifications over the automotive temperature range is guaranteed by design, not production tested.

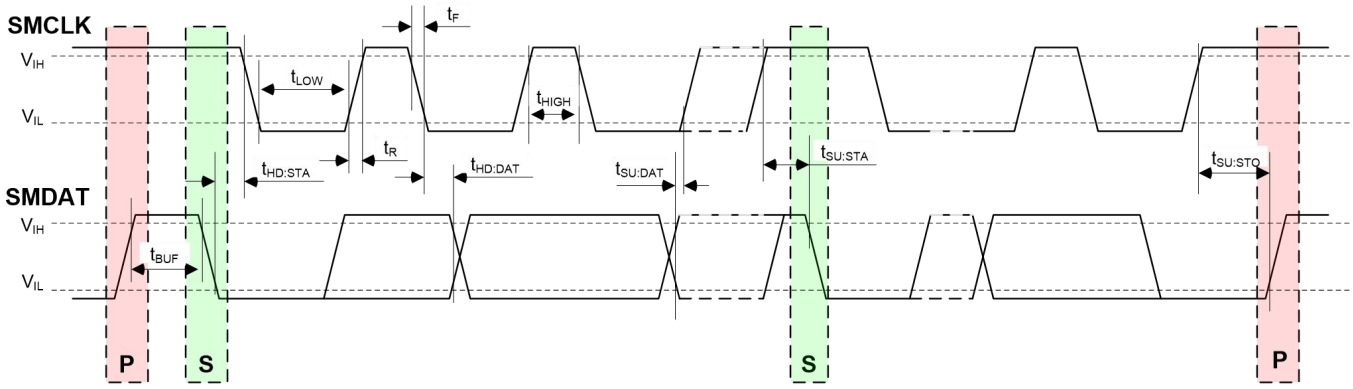


Figure-1. SMBus / I2C Timing Diagram

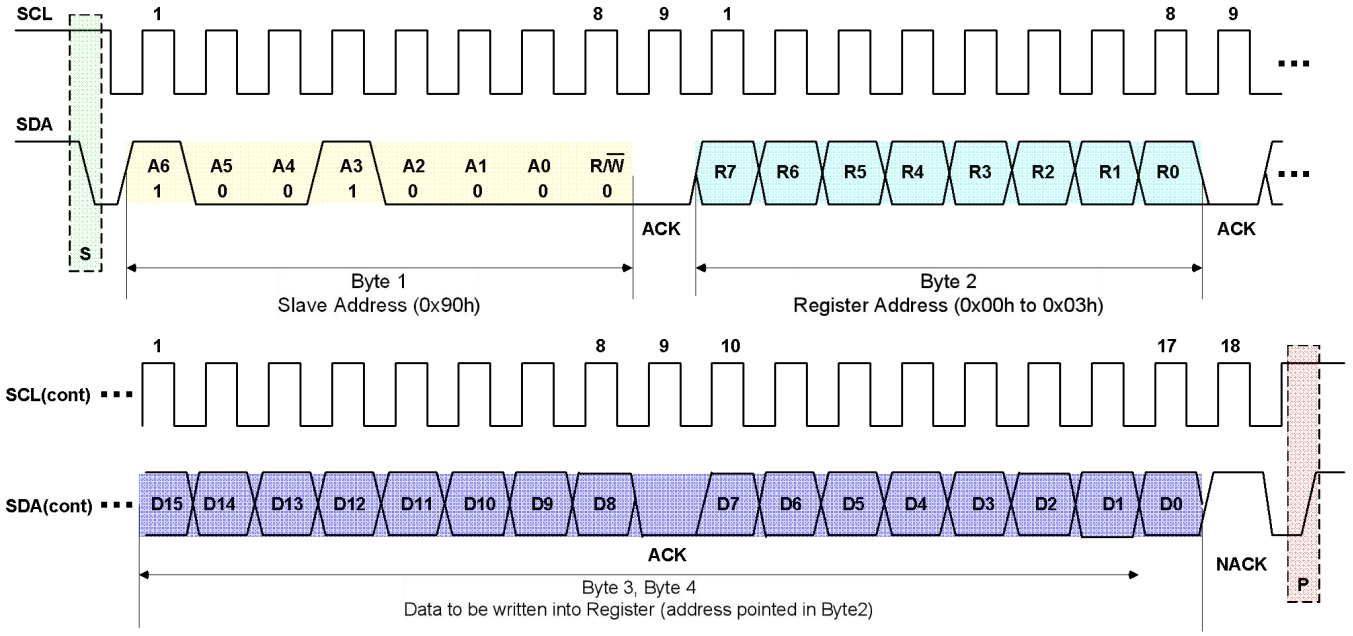


Figure-2. SMBus / I2C Write Word (2-Bytes) Timing Diagram

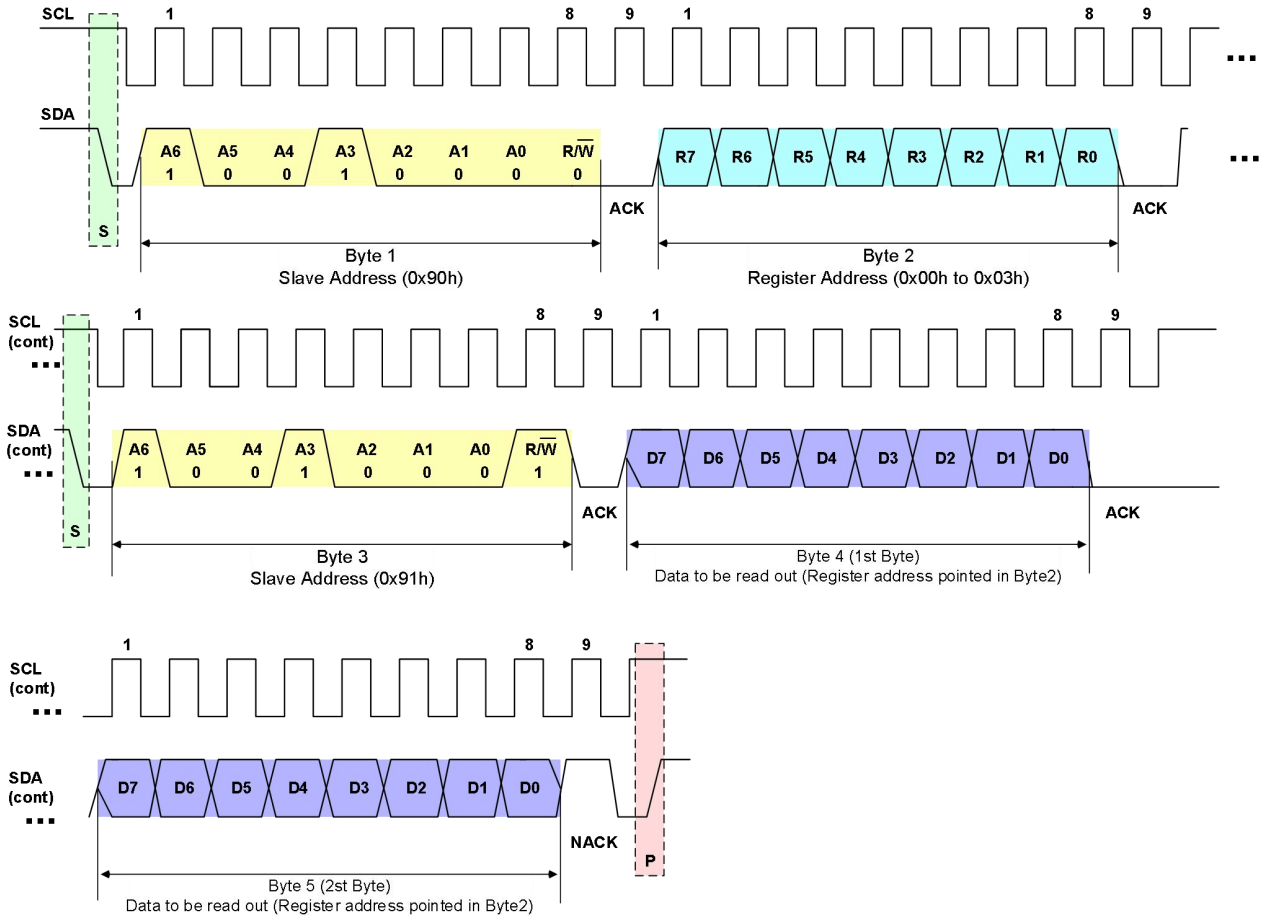


Figure-3. SMBus / I2C Read Word (2-Bytes) Timing Diagram

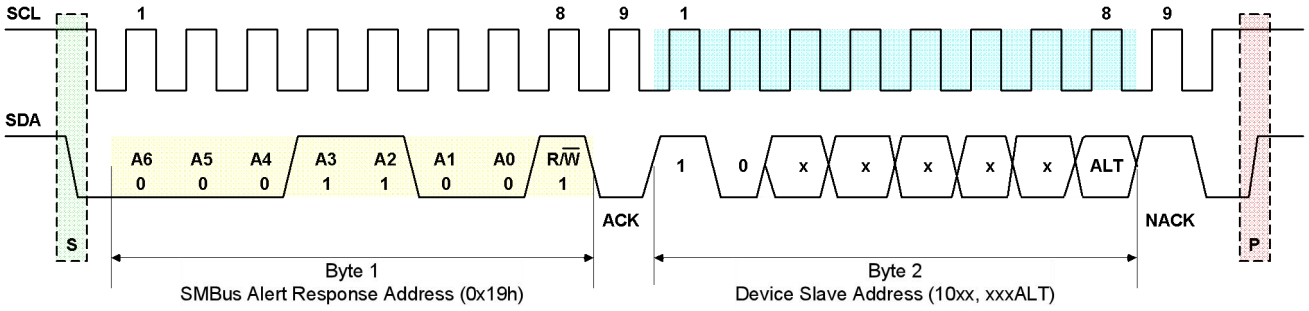
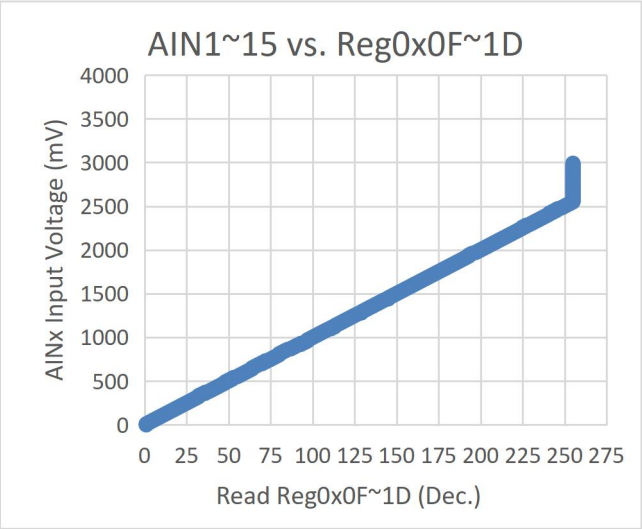
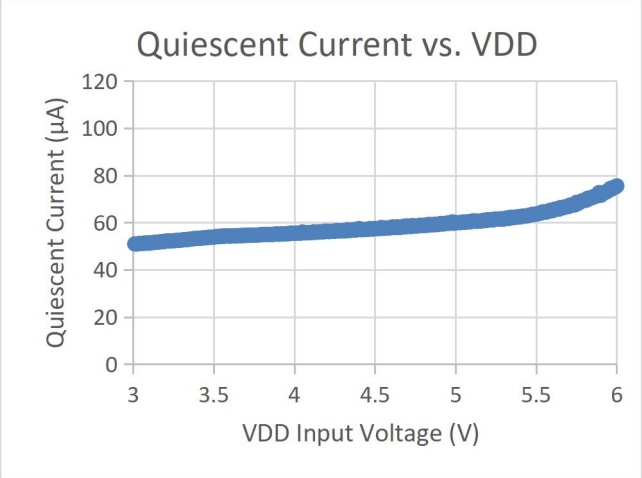
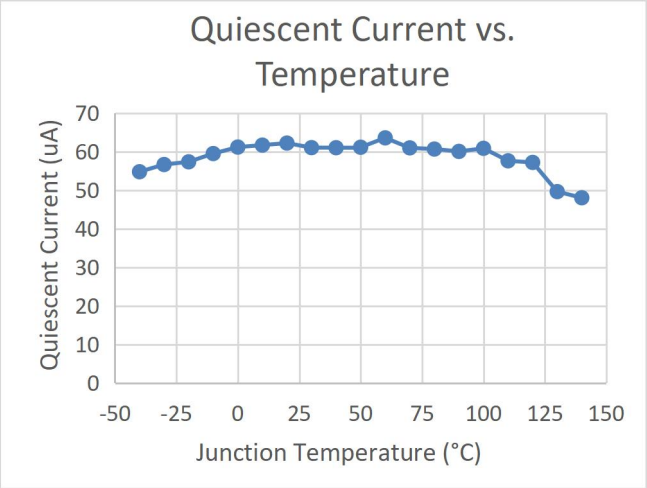


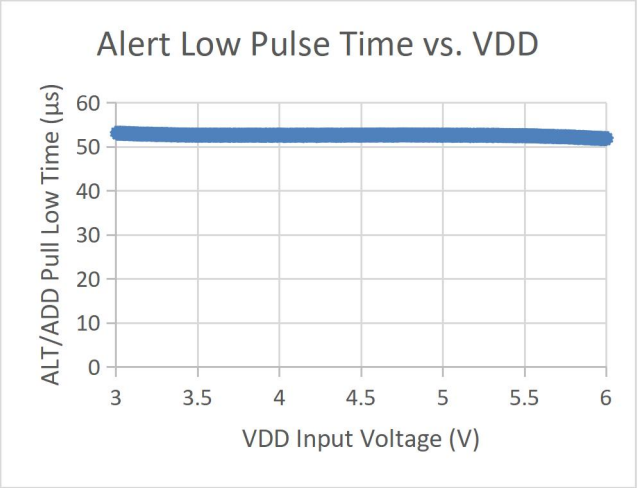
Figure-4. SMBus ALERT Response Diagram

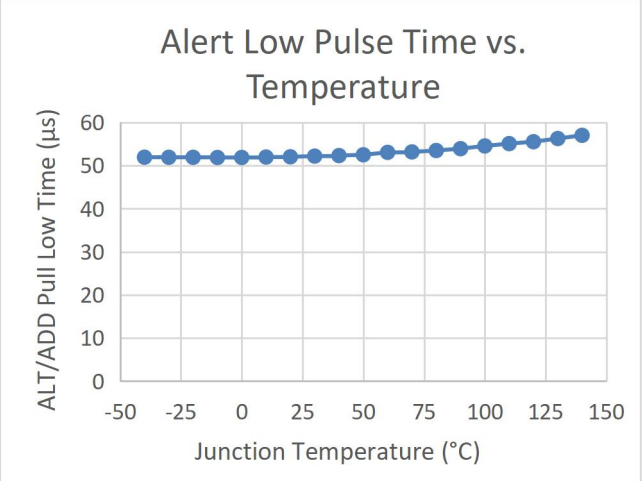
Typical Operating Characteristics



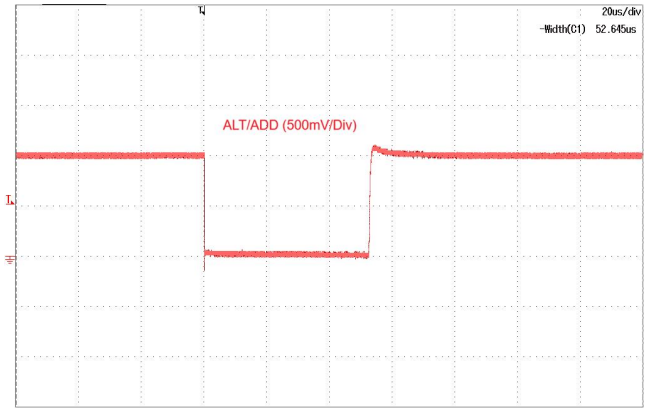






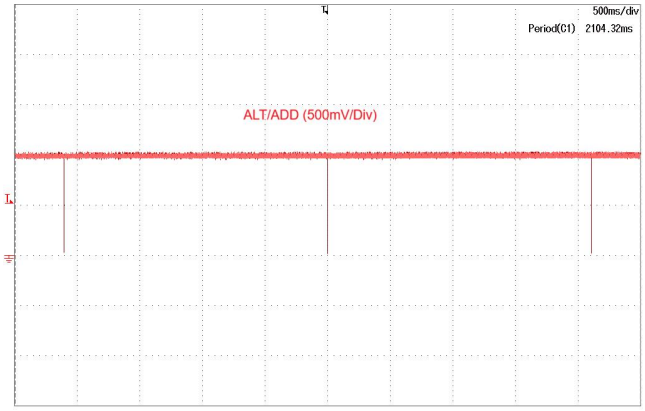


Alert Low Pulse



Time (500ms/Div)

Alert Low Pulse Cycle



Time (500ms/Div)

Function Description

Overview

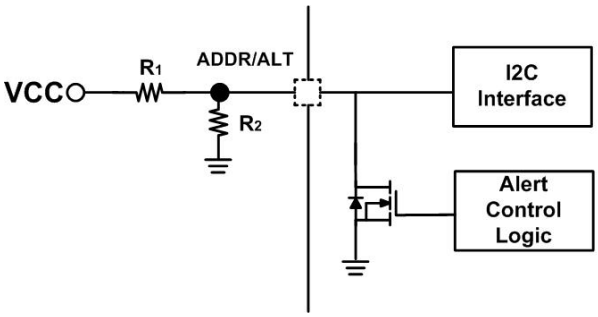
The PMC8000B is a multi-channel temperature monitoring device featuring an integrated 8-bit ADC.
It supports up to 15 temperature-sensing channels using external NTC thermistor resistor divider networks.
The measured voltages are digitized internally and reported to a host controller via an I²C interface for system-level monitoring applications.

I2C Address Programming

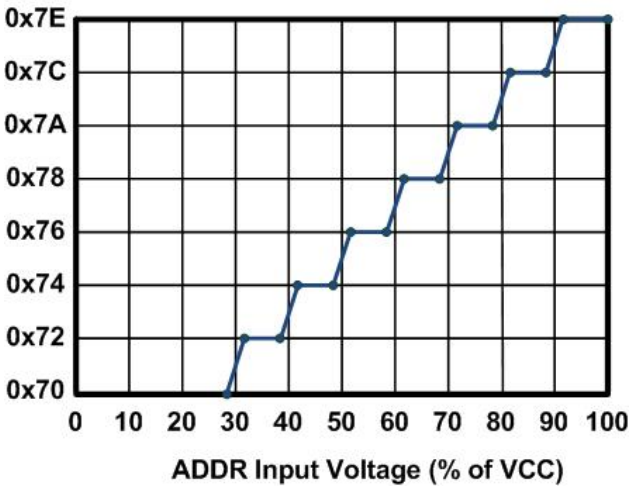
The PMC8000B features a programmable I2C slave address. The 7-bit slave address can be programmed from 0x70h to 0x7Eh, with the R/W bit appended by the I2C master during communication. During address recognition, the device compares the received 7-bit address with its internally programmed address and responds when a match is detected.

The I2C address is programmed through an external R1/R2 voltage divider connected to the ADDR/ALT pin.
The voltage on the ADDR/ALT pin is internally compared against eight predefined reference voltage levels, each corresponding to a selectable I²C address.

Note: If the address-programming function is not used, the ADDR/ALT pin must be pulled up to VCC through a resistor, and the PMC8000B operates with the default I2C address of 0x7Eh.



Address	0x70	0x72	0x74	0x76	0x78	0x7A	0x7C	0x7E
R1 (kOhm)	6	5.1	4.3	3.9	3.6	2	1.5	10
R2 (kOhm)	2	2.7	3.6	4.7	6.8	6.2	8.2	Open
ALT/ADDR (% of VCC)	25	35	45	55	65	75	85	100



Voltage Monitoring and I2C Programming Interface

The PMC8000B digitizes the VIx input voltages using a high-precision analog-to-digital converter (ADC) and communicates the results via the I²C interface.

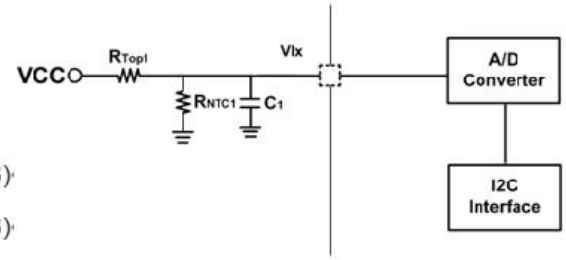
The VIx inputs are sampled sequentially, with a conversion time of 0.6 ms per channel.

VIx ADC Data Registers :

When the VCC supply voltage ranges from 2.8 V to 5.5 V, the ADC provides a resolution of 10 mV and a full-scale input range from 1.0 V to 3.56 V.

The conversion results for each VIx channel are stored in dedicated internal registers, as listed below.

VI1 A/D data store (TD1): Reg0x0F [7] (MSB) ~ Reg0x0F [0] (LSB)↵
VI2 A/D data store (TD2): Reg0x10 [7] (MSB) ~ Reg0x10 [0] (LSB)↵
.....↵
VI14 A/D data store (TD14): Reg0x1C [7] (MSB) ~ Reg0x1C [0] (LSB)
VI15 A/D data store (TD15): Reg0x1D [7] (MSB) ~ Reg0x1D [0] (LSB)



VIx Voltage and ADC Code Conversion

A is an 8-bit unsigned integer representing the ADC conversion result.

When the internal register value is read as A in integer decimal format from Reg0x03, Reg0x04, or Reg0x05, the relationship between the VIx input voltage and the corresponding digital code is defined as follows:

$$A = \frac{V_{VIx} - 1\,V}{10\,mV}$$

or equivalently,

$$V_{VIx} = (10\,mV \times A) + 1\,V$$

VIx Input Voltage Determination

The VIx input voltage is generated by an external resistor divider formed by VCC – Rtopx – RNTCx – GND, and is calculated as:

$$V_{VIx} = V_{CC} \times \frac{R_{NTCx}}{R_{topx} + R_{NTCx}}$$

Substituting the above equation into the ADC transfer function yields:

$$A = \frac{\left(V_{CC} \times \frac{R_{NTCx}}{R_{topx} + R_{NTCx}}\right) - 1\,V}{10\,mV}$$

Note:

1.If the VIx pin is not used, it must be pulled to a high logic level. An external capacitor C_x is recommended to bypass the VIx pin to improve noise immunity.

2.The valid output code range corresponds to the specified ADC input voltage range.

ALT

The ALT indicates the system status based on the monitored VIx conditions.
When a predefined threshold condition is detected on any VIx input, the PMC8000B activates the internal MOSFET on the Alert pin, momentarily pulling the pin low for 50 μs at a 2-second interval.

This pulsed alert behavior allows the host controller to periodically detect fault or warning conditions while minimizing power consumption.

Alert Threshold Level Setting

The ALT (Alert) threshold levels for each VIx channel are programmable through internal registers via the I²C interface, as listed below.

ALT Threshold Registers

VI1 ALT threshold (VI1th): Reg 0x00[7] (MSB) to 0x00[0] (LSB)

VI2 ALT threshold (VI2th): Reg 0x01[7] (MSB) to 0x01[0] (LSB)

……

VI14 ALT threshold (VI14th): Reg 0x0D[7] (MSB) to 0x0D[0] (LSB)

VI15 ALT threshold (VI15th): Reg 0x0E[7] (MSB) to 0x0E[0] (LSB)

ALT Condition Detection and Indication

For each VIx channel, the ALT function is enabled when the programmed threshold value exceeds the measured VIx data, that is:

$$VIxth > VIx$$

When any of the above conditions is met, the corresponding ALT indication bit in the internal status registers is set to logic ‘1’. The ALT indication bits are mapped to Reg0x1E[7:0] and Reg0x1F[6:0], as described below.

ALT Indication Bit Mapping

If Reg0x00 (VI1th) > Reg0x0F (VI1), then ALT_VI1=Reg0x1E[0] = 1; otherwise, Reg0x1E[0] = 0

If Reg0x01 (VI2th) > Reg0x10 (VI2), then ALT_VI2=Reg0x1E[1] = 1; otherwise, Reg0x1E[1] = 0

……

If Reg0x0D (VI14th) > Reg0x1C (VI14), then ALT_VI14=Reg0x1F[5] = 1; otherwise, Reg0x1F[5] = 0

If Reg0x0E (VI15th) > Reg0x1D (VI15), then ALT_VI15=Reg0x1F[6] = 1; otherwise, Reg0x1F[6] = 0

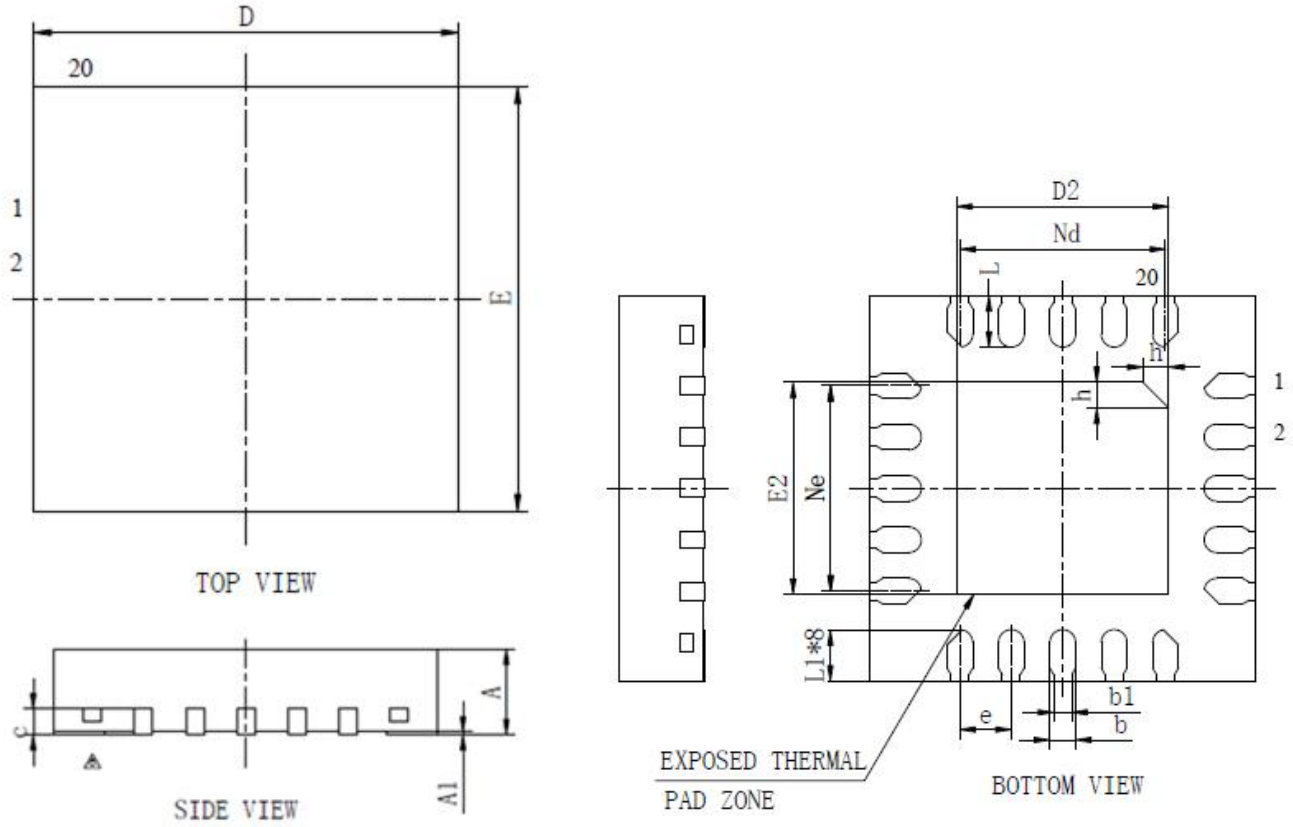
CHIP ID: Reg0xB2[7:0] = 0x1A

I2C Registers Summary

Register Address	Register Name	Bits								R/W	Default Value
		D7	D6	D5	D4	D3	D2	D1	D0		
0x00	VI1th	VI1th [7:0]								R/W	00H
0x01	VI2th	VI2th [7:0]								R/W	00H
0x02	VI3th	VI3th [7:0]								R/W	00H
0x03	VI4th	VI4th [7:0]								R/W	00H
0x04	VI5th	VI5th [7:0]								R/W	00H
0x05	VI6th	VI6th [7:0]								R/W	00H
0x06	VI7th	VI7th [7:0]								R/W	00H
0x07	VI8th	VI8th [7:0]								R/W	00H
0x08	VI9th	VI9th [7:0]								R/W	00H
0x09	VI10th	VI10th [7:0]								R/W	00H
0x0A	VI11th	VI11th [7:0]								R/W	00H
0x0B	VI12th	VI12th [7:0]								R/W	00H
0x0C	VI13th	VI13th [7:0]								R/W	00H
0x0D	VI14th	VI14th [7:0]								R/W	00H
0x0E	VI15th	VI15th [7:0]								R/W	00H
0x0F	VI1	VI1 [7:0]								R	00H
0x10	VI2	VI2[7:0]								R	00H
0x11	VI3	VI3[7:0]								R	00H
0x12	VI4	VI4 [7:0]								R	00H
0x13	VI5	VI5[7:0]								R	00H
0x14	VI6	VI6[7:0]								R	00H
0x15	VI7	VI7[7:0]								R	00H
0x16	VI8	VI8[7:0]								R	00H
0x17	VI9	VI9[7:0]								R	00H
0x18	VI10	VI10[7:0]								R	00H
0x19	VI11	VI11 [7:0]								R	00H
0x1A	VI12	VI12[7:0]								R	00H
0x1B	VI13	VI13[7:0]								R	00H
0x1C	VI14	VI14[7:0]								R	00H
0x1D	VI15	VI15[7:0]								R	00H
0x1E	ALT	ALT VI8	ALT VI7	ALT VI6	ALT VI5	ALT VI4	ALT VI3	ALT VI2	ALT VI1	R	00H
0x1F	ALT	Reserved	ALT VI15	ALT VI14	ALT VI13	ALT VI12	ALT VI11	ALT VI10	ALT VI9	R	00H
0xB2	CHIP ID									R	1BH

Package Dimension Outline & Land Pattern

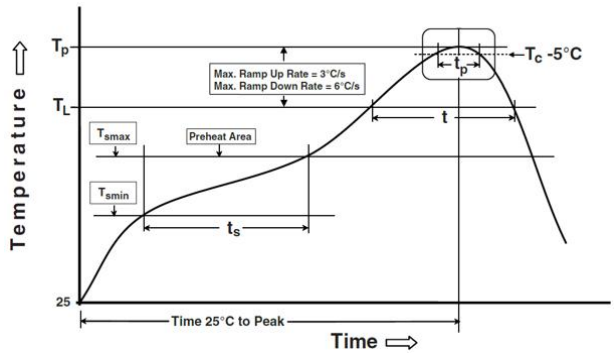
WQFN 3x3 -20 (mm)



Symbol	MILLIMETER		
	Min.	Nom.	Max.
A	0.70	0.75	0.80
A1	-------	0.02	0.05
b	0.15	0.2	0.25
b1		0.14 REF	
C		0.203 REF	
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e		0.40 BSC	
Ne		1.60 BSC	
Nd		1.60 BSC	
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
L1	0.30	0.40	0.50
h	0.20	0.25	0.30

Note: Dimensions in millimeters unless otherwise specified.

Classification Profile



Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	 150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217 °C 60-150 seconds
Peak package body temperature (T_p)	For users T_p must not exceed the Classification temp in Table below
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 5-1.	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.

Version History

Version	Date	Changes
Rev.1.0	2026-04-15	Initial release

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