PJ16606 Datasheet

5.8V-60V, 6A, High-Efficiency, Asynchronous Buck Converter with Adjustable Frequency

Version：Rev.1.0

Release Date：2026-04-15

PANJIT International Inc.

www.panjit.com.tw

General Description

The PJ16606 is a 6A non-synchronous step-down DC-DC converter operating over a wide input voltage range of 5.8V to 60V and providing a regulated low output voltage. It integrates a 80mΩ high-side MOSFET for high-efficiency power conversion. The device utilizes peak current mode control with Pulse-Skipping Modulation (PSM) to maintain high efficiency under light-load and standby conditions.

The switching frequency can be adjusted from 200 kHz to 2.2 MHz by setting an external resistor, allowing the system to be optimized for either high efficiency or a compact component footprint. The converter efficiently steps down a high input voltage to a low output voltage while supporting a minimum high-side MOSFET on-time of 50ns.

A fixed 4ms soft-start time limits inrush current during output voltage startup, and the device supports monotonic startup with a pre-biased output. Comprehensive protection features include cycle-by-cycle current limit, hiccup-mode over current protection, thermal shutdown, output over voltage protection, and input under voltage protection.

Available in a 8-lead, 5mm × 4mm ESOP package.

Features

- Wide Input range: 5.8V to 60V
- 6A Continuous Output Current
- FB Tolerance: ±2% over Full Temperature Range
- Integrated 85mΩ High-Side MOSFET
- Ultra Low Quiescent Current: 15μA (RTOP 1MΩ)
- Shutdown Current: 1μA
- Peak current mode control
- Pulse Skipping Mode (PSM) in Light Load
- Minimum On time: 50ns (Typ.)
- Output Soft-Start: 4ms
- Adjustable switching frequency: 200kHz to 2.2MHz
- Precision Enable Threshold for Programmable Input voltage under-voltage lockout (UVLO) Threshold and Hysteresis
- Linear increase in frequency during startup
- Monotonic Start up with Pre-biased Output
- Hiccup Mode for Output Over current Protection
- Over-voltage and Over-Temperature Protection
- Available in an ESOP-8 Package

Applications

- 12V, 24V, 48V Industry and Telecom Power Systems
- Industrial Automation and Motor Control
- Vehicle Accessories

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Ordering Information

Ordering Information

Order number	Marking ID	Package	Definition
PJ16606PP	16606 YMDNN	SOP-8 EP	Halogen free RoHS compliant in T/R,4,000pcs/Reel

Note:

(1) Panjit can meet RoHS 2.0/REACH requirement. So most package types Panjit offers only states halogen free, instead of lead free.

Marking Information

Marking	Package	Definition
16606 YMDNN	SOP-8 EP	16606:Product code YMDNN : Y : Year code M : Month code D : Day code ,NN: Serial Number

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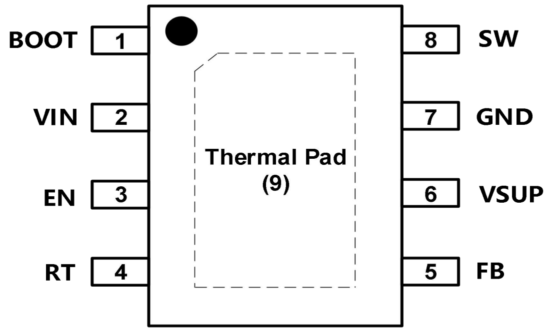
Pin Configuration



(Top View)

Pin Description

Table 1.

Pin No.	Pin Name	Type[1]	Description
1	BOOT	O	Boot-strap. Supply voltage for the internal high-side gate driver. Connect a 0.1μF ceramic capacitor between the SW and BOOT.
2	VIN	P, I	Input Power Supply Pin. Connect the power supply to this pin and connect a bypass capacitor between this pin and GND pin.
3	EN	I	Enable Input. Drive the EN pin below 1.05V to turn the converter off; float or connect to VIN to enable the converter. Connect the EN pin to the center node of a resistor divider between VIN and GND to set the UVLO threshold.
4	RT	I	Switching Frequency Pin. Connect a resistor to GND to set the switching frequency.
5	FB	I	Feedback Voltage Sense Input. Connect a resistor divider to set the output voltage.
6	VSUP	O	Internal 4V Regulator Output.
7	GND	G	Ground.
8	SW	O	Power Switch Output Pin. Connect to power inductor.
9	Thermal Pad	G	Heat dissipation path of die. Electrically tied to GND. Connect to PCB ground plane for proper function and thermal efficiency.

(1) Legend: P = Power Pin,D = Digital Pin,I = Input Pin,O = Output Pin,G=Ground

Typical Application

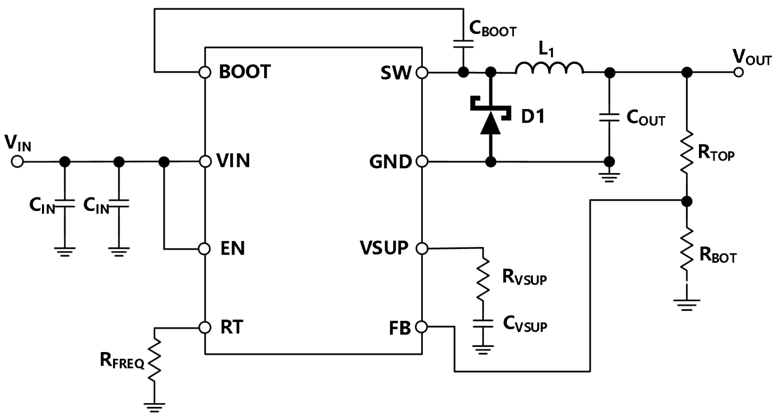


Figure 1. Typical Application Circuit

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Specifications

Absolute Maximum Ratings

Over operating free-air temperature unless otherwise noted(1)

Table 2.

Parameter	Min	Max	Unit
VIN, EN	−0.3	65	V
BOOT	−0.3	71	V
SW	−1	65	V
BOOT-SW	-0.3	6	V
VSUP, FB, RT	-0.3	6	V
Junction temperature	−40	150	°C
Storage temperature	−65	150	°C
Lead temperature (soldering, 10sec.)		260	°C

(1) Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

Table 3.

Parameters	Min	Typ	Max	Unit
Operating Junction Temperature(T_J)	-40		125	°C
Continuous Supply Voltage (V_{IN})	5.8		60	V
Output Voltage (V_{OUT})	0.8		57	V
Load Current Range	0		6	A

Electrostatic Discharge (ESD)

Table 4. ESD Rating

Parameters	Description	Rating	Unit
HBM	Human Body Model ANSI/ESDA/JEDEC JS-001-2024 Classification, Class: 2	±2000	V
CDM	Charged Device Mode ANSI/ESDA/JEDEC JS-002-2025 Classification, Class: C2b	±750	V

ESD Caution

Electrostatic Discharge Sensitive Device.
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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Thermal Resistance

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 5. Thermal Resistance

Item[1,2]	Description	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	34	°C/W
θ_{JC}	Junction-to-case (top) thermal resistance	72	°C/W

(1) The package thermal impedance is calculated in accordance to JESD 51-7.

(2) Thermal Resistances were simulated on a 4-layer, JEDEC board.

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Electrical Specifications

Limits apply over the recommended operating junction temperature range of –40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: VIN = 24V. VOUT is converter output voltage.

Table 6.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power supply						
V_{IN}	Operating input voltage		5.8		60	V
V_{IN_UVLO}	Input UVLO Threshold Hysteresis	V_{IN} rising		5.3 300		V mV
I_{SHDW}	Shutdown current from VIN pin	EN=0, no load		1		μA
I_Q	Quiescent current from VIN pin	EN floating, no load, non-switching, BOOT-SW=5V		10		μA
Power MOSFETs						
R_{DSON_H}	High-side MOSFET on-resistance	V_{BOOT}-V_{SW}=5V		85		mΩ
Reference						
V_{REF}	Reference voltage of FB			0.8		V
Current Limit and Over Current Protection						
I_{LIM_HS}	High-side power MOSFET peak current limit threshold			9.7		A
Enable and Soft-startup						
V_{EN_H}	Enable high threshold			1.2		V
V_{EN_L}	Enable low threshold			1.1		V
I_{EN_L}	Enable pin pull-up current	EN=1V		1		μA
I_{EN_H}	Enable pin pull-up current	EN=1.5V		4		μA
T_{SS}	Soft start time			4		ms
Switching Frequency						
F_{RANGE_RT}	Frequency rang using RT mode		200		2200	kHz
Fsw	Switching Frequency	RRT=200kΩ(1%)		500		kHz
T_{ON_MIN}	SW Minimum on-time	V_{IN}=24V		50		ns
Protection						
V_{OVP}	Feedback overvoltage with respect to reference voltage	V_{FB}/V_{REF} rising V_{FB}/V_{REF} falling		110 105		% %
V_{BOOTUV}	BOOT-SW UVLO Threshold	BOOT-SW falling		2.2		V
T_{SD}	Thermal shutdown threshold			170		°C
T_{SD_HYS}	Thermal shutdown Hysteresis			25		°C

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Typical Performance Characteristics

V_{IN} = 24V, V_{OUT} = 5V, L = 6.5μH, f_{SW} = 500kHz, T_A = 25°C, unless otherwise noted.

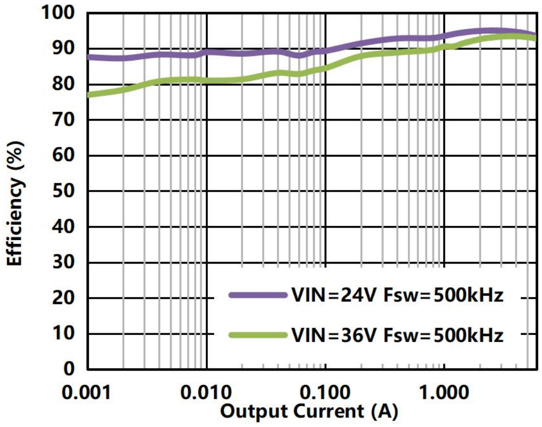

Figure 2. Efficiency vs Load Current, Vout=12V

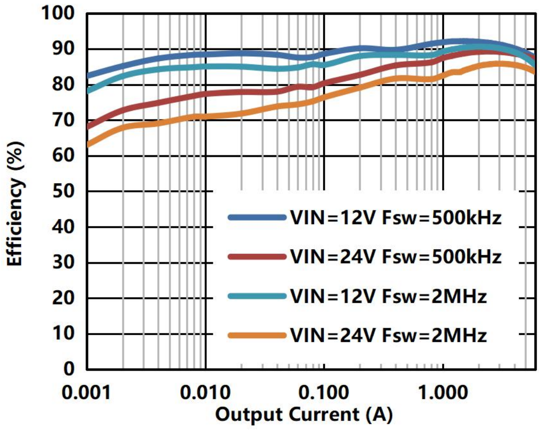

Figure 3. Efficiency vs Load Current, Vout=5V

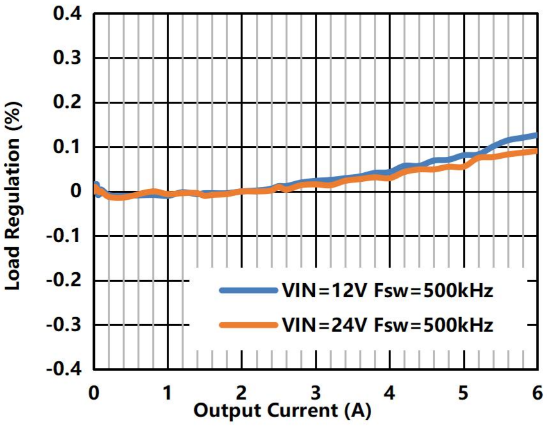

Figure 4. Load Regulation, Vout=5V

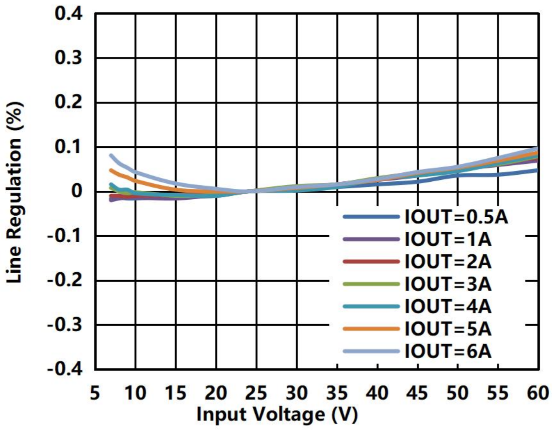

Figure 5. Line Regulation, Vout=5V

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Product Overview

The PJ16606 is a high performance, highly efficient buck converter operating from 5.8V to 60V input with 6A output capability, integrating an 85mΩ high-side MOSFET. The device employs constant-frequency peak-current-mode control for precise output voltage regulation, delivering excellent line and load transient response.

The switching frequency is programmable from 200kHz to 2.2MHz with an external resistor. In light-load conditions, the converter operates in Pulse Skipping Modulation (PSM) mode, achieving typical quiescent current of 15µA. Under heavy loads, the device runs in fixed-frequency Pulse Width Modulation (PWM) mode, with seamless transition between modes ensuring high efficiency across the full load range.

The PJ16606 includes input under-voltage lockout, output over-voltage protection, cycle-by-cycle current limit, short-circuit protection, and thermal shutdown.

Peak Current Mode Control

The PJ16606 operates on a fixed-frequency peak current mode control principle. In each switching cycle, an internal clock signal initiates the turn on of the integrated high-side MOSFET, causing the inductor current to rise. The high side MOSFET turns off once the inductor current reaches a threshold level set internally by the error amplifier. The error amplifier regulates the output by comparing the feedback (FB) voltage with an internal 0.8V reference. Integrated slope compensation ensures stability at duty cycles greater than 50%.

During light-load conditions, the device enters Pulse Skipping Mode (PSM) to maintain high efficiency. In this mode, switching cycles are selectively skipped, significantly reducing switching and gate drive losses. The controller consumes only 15 µA of quiescent current during the skipping intervals. The converter automatically resumes normal PWM operation when the load increases.

Internal Soft-Start

The device incorporates an internal soft-start circuit that ramps the output reference voltage from 0V to the nominal 0.8V reference level over a 4ms period.

Over Current Limit and Hiccup Mode

The PJ16606 provides cycle by cycle peak current limit with fold-back characteristic. During an overload or output short circuit event, the high-side MOSFET peak current is limited to a safe threshold, preventing inductor current runaway. If the output voltage remains below regulation for a prolonged period, the protection circuit automatically enters hiccup mode, periodically restarting the converter to reduce average short-circuit current and mitigate thermal stress.

Over voltage Protection

The PJ16606 incorporates output over voltage protection to limit voltage overshoot during transient conditions. This function is monitored through the FB pin voltage. When the FB voltage exceeds 110% of the 0.8V internal reference, the high-side MOSFET is immediately disabled, halting switching to prevent further output voltage increase. Normal operation resumes once the FB voltage falls below 105% of the reference, allowing the high-side MOSFET to turn on again. This protection enhances system reliability during load transients, fault recoveries, or light-load conditions.

Thermal Shutdown

The device monitors the die temperature. If the junction temperature exceeds 170°C, the internal thermal shutdown circuitry turns off the regulator, stops the MOSFET switching.Thermal shutdown is a non-latch protection, when the junction temperature falls below to 145°C, the part resumes normal operation with soft start automatically.

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Typical Application Circuit

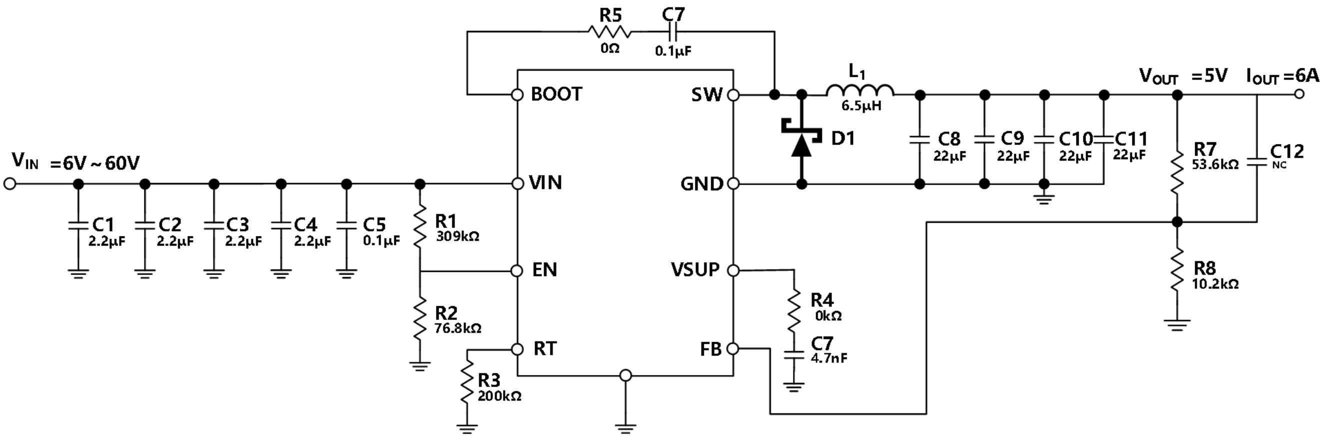

Figure 6. Typical Application Circuit (500kHz)

Application Information

Component selection steps are described in this section based on the example specifications listed in Table 8. The schematic of this design example is showed in Figure 6. Typical Application Circuit (500kHz)

Table 7. Parameter of Design Example

Parameter	Description
Input Voltage	V_{IN}=24V Normal, 6V to 60V
Output Voltage	V_{OUT}=5V
Output Current	I_{OUT}=6A
Switching Frequency	f_{sw}=500kHz

Output Voltage Setting

The external feedback resistors connected to FB sets the output voltage. The feedback resistor values can be calculated with the below equation.

$$R_7=\left(\frac{V_{OUT}}{V_{REF}}-1\right)\times R_8$$

While R_8=10.2kΩ, V_{REF}=0.8V, V_{OUT}=5V

Calculate R_7=53.6kΩ

Table 8. Recommended Resistor Values for Common Output Voltages

V_{OUT} (V)	R_{TOP}(kΩ)	R_{BOT}(kΩ)
3.3	31.6	10.2
5	53.6	10.2
12	143	10.2
24	294	10.2

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Switching Frequency

Higher switching frequencies allow smaller output inductors and capacitors, thus lowering voltage and current ripples. However, the higher frequency also bring additional switching loss, which reduce the converter's efficiency and thermal performance. In this design, a moderate 500 kHz switching frequency is chosen to balance compact size and high-efficiency operation.

The PJ16606's switching frequency is controlled by a single resistor connected to the RT pin. The resistor value can be calculated from the following equation:

$$R_3(k\Omega)=\frac{100000}{f_{sw}(kHz)}$$

Where:

fsw is desired switching frequency

For example, a 500kΩ resistor sets the switching frequency to 200kHz, a 200kΩ resistor sets the frequency to 500kHz. A bench test may be required to fine-tune the calculated resistance. Table 9 shows the typical relationship between f_{sw} and R_{FSW} .

Table 9. Switching Frequency vs R_{FSW}

F_{SW}	$R_3(R_{FSW})$
200kHz	500kΩ
500kHz	200kΩ
800kHz	125kΩ
1200kHz	83kΩ
2000kHz	45.3kΩ
2200kHz	39kΩ

Under Voltage Lock-Out(UVLO)

The input voltage under voltage Lock-Out(UVLO) threshold are configured using an external resistive divider, consisting of R1 connected between the input rail and EN pin, and R2 connected between EN pin and GND. UVLO features dual thresholds: an upper threshold for power-on (triggered as input voltage rises) and a lower threshold for power-down or brownout protection (triggered as input voltage drops).

Inductor Selection

The inductor value is determined by the switching frequency, input voltage, output voltage, and inductor ripple current. For the highest efficiency, choose an inductor with a low DC resistance. The performance of the inductor affects the transient behavior, efficiency, loop stability. Using a larger inductor value reduces the output ripple current and then reduces the output voltage ripple, and also leads to better efficiency, but it leads to slower transient behavior. A smaller inductor value offers a fast transient behavior, but it leads to larger inductor ripple current and then decreases efficiency.

The inductor value can be calculated by the following equation:

$$L=\frac{(V_{IN}-V_{OUT})\times D}{\Delta I_L \times f_{sw}}$$

where:

V_{IN} is the input voltage.

V_{OUT} is the output voltage.

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D is the duty cycle ($D=\frac{V_{OUT}}{V_{IN}}$)

f_{SW} is the switching frequency.

ΔI_L is the inductor ripple current, which is, for the most applications, typically between 20% and 40% of the maximum load current.

The peak inductor current, I_{PEAK} is calculated by the following equation:

$$I_{PEAK}=I_{LOAD}+\frac{\Delta I^2}{2}$$

The saturation current of the inductor must be higher than the device’ s peak current limit, and RMS current must also not be exceeded, as the following equation:

$$I_{RMS}=\sqrt{(I_{OUT})^2+\frac{\Delta I_L^2}{12}}$$

where:

V_{IN} is the DC load current.

Under overload or transient conditions, the inductor peak current can reach the device’s current limit (typically 9.7 A). It is recommended to select an inductor with a saturation current rating above 9.7 A.

The maximum output current of the PJ16606 is limited by the device’s peak current capability and the inductor’s current ripple. A smaller inductance increases ripple, which in turn reduces the available maximum output current. Therefore, the required maximum output current should be considered when selecting the inductance value.

Diode Selection

The PJ16606 requires an external freewheeling diode between SW and GND. A Schottky diode is recommended for its low forward voltage, which enhances system efficiency. The selected diode must have a reverse voltage rating exceeding VIN(MAX) and a peak current rating greater than maximum Inductor current.

It should be noted that diodes with higher voltage and current ratings typically exhibit increased forward voltage. A device with a minimum 60V reverse voltage rating is recommended to withstand input transients up to the PJ16606's rated voltage. The PDS760-13 Schottky diode, selected for the reference design, provides a favorable balance with a forward voltage of 0.48V at 6A and good thermal characteristics.

The diode's power dissipation includes conduction loss and AC switching loss. Conduction loss, calculated as output current multiplied by forward voltage, occurs when the diode carries current during the switch off-time. At elevated switching frequencies, AC losses from junction capacitance charging/discharging and reverse recovery become significant.

The PDS760-13 diode, featuring a junction capacitance of 400pF, exhibits a total dissipation of approximately 1.9W at maximum input voltage. This value is calculated using the following expression:

$$P_D=\frac{(V_{IN\_MAX}-V_{OUT})\times I_{OUT}\times V_d}{V_{IN\_MAX}}+\frac{C_j\times f_{sw}\times(V_{IN}+V_D)^2}{2}$$

If the application involves extended operation at light load or in sleep mode, it is beneficial to select a diode that offers low leakage current and a slightly higher forward voltage drop.

Input Capacitor Selection

The step-down converter has a discontinuous input current, therefore it requires a capacitor to supply the AC to the converter while maintaining the DC VIN. Ceramic capacitors with X5R or X7R dielectrics are strongly recommended because of the low ESR and small temperature coefficients. To filter the high frequency switching

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noise, it is recommended that use a lower value capacitor(0.1uF) with 0603 package size. Place the input capacitor as close as possible to the Vin pin.

The voltage rating of the input capacitor must be greater than the maximum input voltage. The input capacitor value is a function of the source impedance, one bulk capacitor is needed if the source impedance is over high. Make sure that the ripple current rating should not exceed the converter's maximum input ripple current calculated from the following equation:

$$I_{CIN\_RMS}=I_{OUT}\times\sqrt{\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}})}$$

The worst-case condition occurs at V_{IN} = 2 x V_{OUT}, where:

$$I_{CIN\_RMS}=\frac{I_{OUT}}{2}$$

For simplification, choose a C_{IN} with an RMS current rating greater than half of the maximum load current. Ensure that the voltage rating of the input capacitor must be greater than the maximum input voltage. The input voltage ripple caused by the capacitance can be calculated from the following equation:

$$\Delta V_{IN}=\frac{I_{OUT}}{f_{SW}\times C_{IN}}\times\frac{V_{OUT}}{V_{IN}}\times(1-\frac{V_{OUT}}{V_{IN}})$$

This example utilizes four parallel 2.2μF, 100V X7R ceramic capacitors, along with a closely placed 0.1μF capacitor for high-frequency filtering.

Bootstrap Capacitor Selection

A resistor (R_{BOOT}) in series with C_{BOOT} can reduce SW's rising rate and voltage spikes. This improves EMI performance and reduces voltage stress at a high VIN. A higher resistance is better for SW spike reduction, but can compromise efficiency. To make a trade off between EMI and efficiency, it is recommended to keep R_{BOOT} below 20Ω. The recommended C_{BOOT} value is between 0.1μF and 1μF.

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Layout Recommendation

The quality of the PCB layout is essential for the performance of the PJ16606. Bad PCB layout can degrade the output regulation, the EMI and EMC performance. For the best performance the PJ16606, it is recommended to adopt a 4-layer layout to improve thermal performance by referring to Figure 7 and following the guidelines.

1. Place the input capacitor, inductor, and output capacitor as close as possible to the IC, and use the short trace.
2. Keep the switching loop as small as possible.
3. Keep VIN, VOUT, GND paths as short and wide as possible.
4. Place the feedback divider as close as possible to the FB pin to prevent noise pickup.
5. Place enough PCB area and use multiple vias to connect the power planes to the internal layer for proper heat sinking.

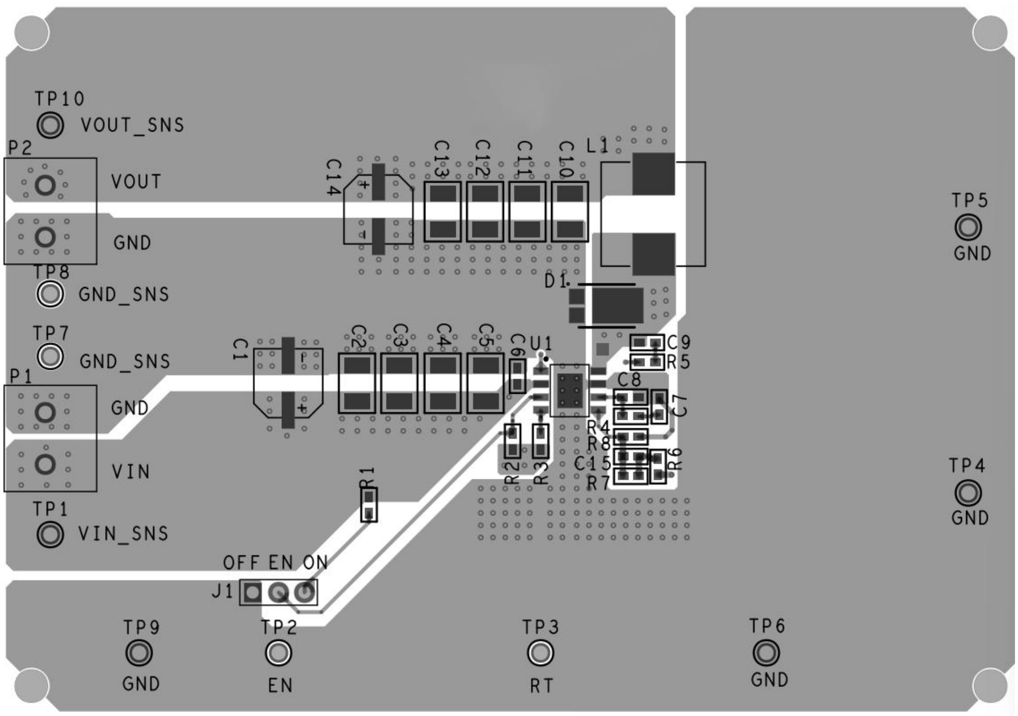

Figure 7. EVM TOP Layer Example

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Packing information

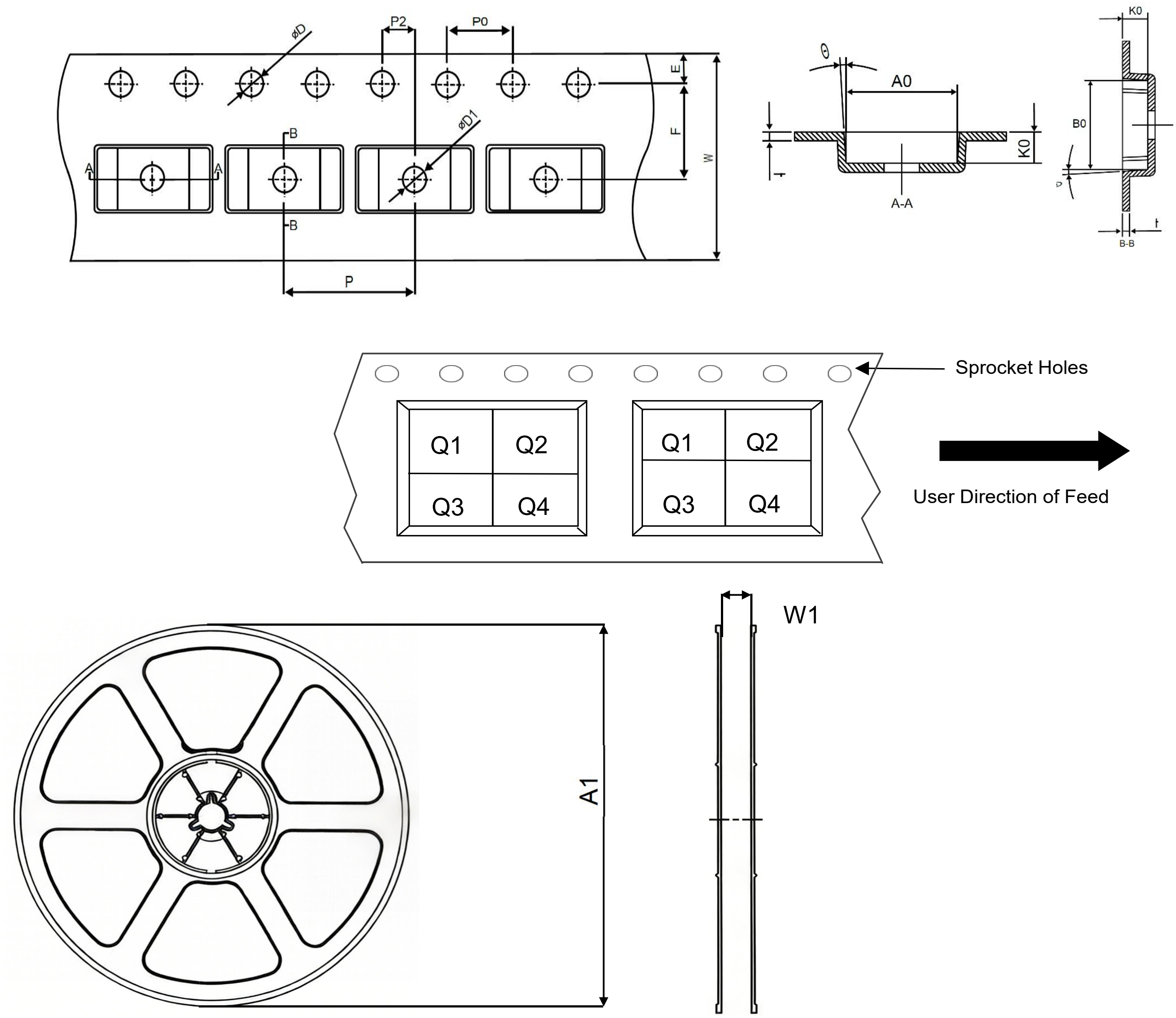

Figure 8. TAPE and Reel Information

Package Type	E (mm)	F (mm)	P2 (mm)	D (mm)	D1 (mm)	P0 (mm)	W (mm)	W1 (mm)	P (mm)	A0 (mm)	A1 (mm)	B0 (mm)	K0 (mm)	t (mm)	Pin1 Quadrant	Quantity
ESOP-8	1.75	5.50	2.00	1.50	1.55	4.00	12.00	12.40	8.00	6.55	330	5.30	2.00	0.25	Q1	4000

(1) All dimensions are nominal

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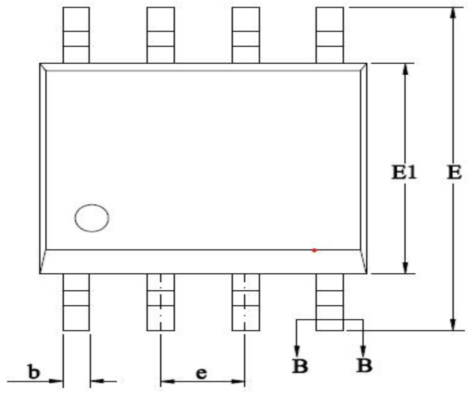
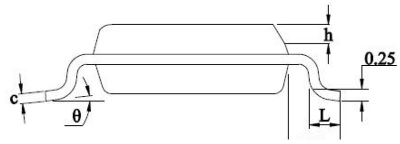
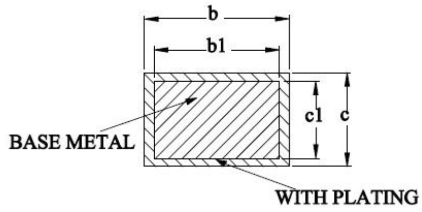
Package Outlines

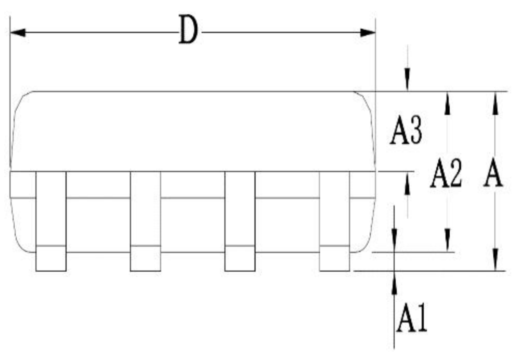


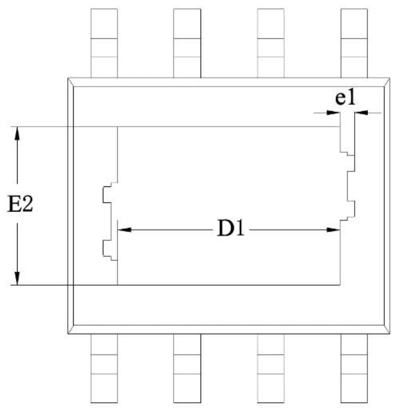
TOP VIEW





SECTION B-B





BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A			1.65
A1	0.00	-	0.10
A2	1.3	1.4	1.5
A3	0.60	0.65	0.70
b	0.39	-	0.47
b1	0.38	0.41	0.44
c	0.2	-	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
D1	2.09REF		
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
E2	2.09REF		
e	1.27BSC		
e1	0.16REF		
h	0.25	-	0.50
L1	1.05REF		
L	0.30	0.40	0.50

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Version History

Version	Date	Changes
Rev.1.0	2026-04-15	Initial release

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