PJ13943 Datasheet

3A Synchronous Step-Down Regulator with 30µA Quiescent Current

Version：Rev.1.0

Release Date：2026-04-22

MetaWells Co., Ltd.

www.metawells.com

General Description

The PJ13943 is a high efficiency synchronous monolithic step-down switching regulator with integrated internal high-side and low-side MOSFETs. It provides up to 3A output current with peak current mode control for fast loop response.

The PJ13943 operates over a wide input voltage range from 3.0V to 36V with only 30μA low quiescent current.

Standard features include thermal shutdown, UVLO, enable (EN) control and power good (PG) indicator.

During the overload or output short circuit, the cycle by cycle current limit and hiccup protection are provided. Thermal shutdown provides reliable and fault-tolerant operation.

It should be noticed that no capacitors should be placed between EN and GND, for preventing the chip from entering test mode.

Features

- **Wide Input Voltage Range: 3.0V to 36V**
- **410kHz Switching Frequency**
- **3A Output Current Capability**
- **Low Operating Quiescent Current: 30μA (Typ.) From 12V_{IN} to 3.3V_{OUT}**
- **±1.5% 1V Reference Over -40°C~125°C**
- **Peak Eff. >95% (Typ.) From 12V_{IN} to 5V_{OUT}**
- **Minimum On Time: 40ns (Typ.)**
- **Internal Compensation**
- **Precision Enable**
- **Cycle by Cycle Current Limit and Hiccup When Overload or Short Circuit**
- **Thermal Shutdown and Auto Recovery**

Applications

- **Automotive System: Cockpit, ADAS**
- **Consumer systems: Robotic Vacuum Cleaner, Drone.**
- **Battery Powered System: Power Tools, Home Appliance, GPS Tracker etc.**
- **Industrial and Medical Power Supplies**

Copyright © MetaWells Co., Ltd. All rights reserved.

Ordering Information

Ordering Information

Order number	Marking ID	Package	Description
PJ13943AQW	13943A YMDNN	QFN3X3-8	Halogen free RoHS compliant in T/R,3,000 pcs/Reel

Note:

(1) MetaWells can meet RoHS 2.0/REACH requirement. So most package types MetaWells offers only states halogen free, instead of lead free.

Marking Information

Marking	Package	Definition
13943A YMDNN	QFN3X3-8	13943A:Product code YMDNN : Y : Year code M : Month code D : Day code ,NN: Serial Number

Copyright © MetaWells Co., Ltd. All rights reserved.

Typical Application

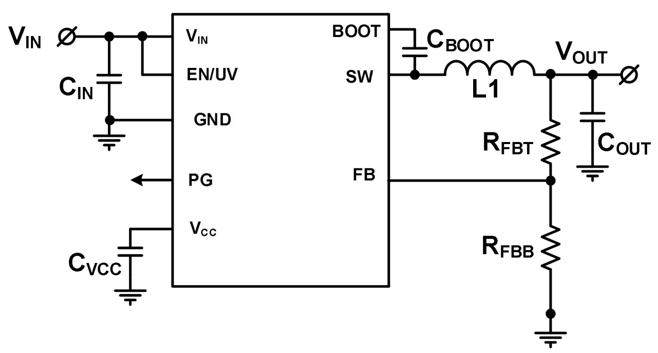


Fig.1 Schematic Diagram

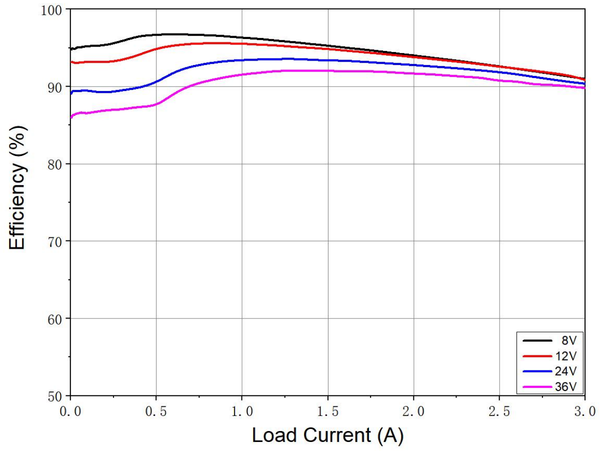
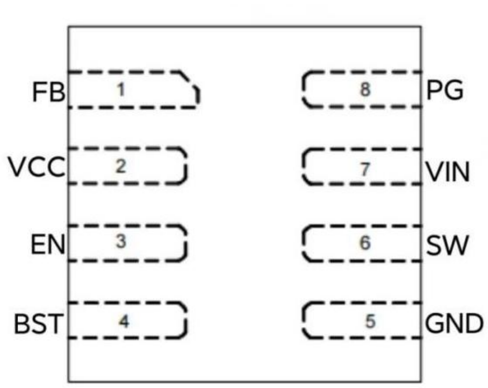


Fig.2 Efficiency vs. Output Current

Pin Configuration



QFN3X3-8 (Top View)

Pin Functions

Table 1. Pin Description

No.	Pin	Type[(1)]	Description
1	FB	I	Feedback Voltage
2	VCC	O	Internal Supply for Control Circuits
3	EN	I	Enable Input, no higher than Input Voltage, Do not place any capacitor between this pin and GND.
4	BST	I/O	Bootstrap Supply Voltage
5	GND	G	Power Ground
6	SW	I/O	Switching Node Output
7	VIN	P	Input Voltage
8	PG	I/O	Power Good Signal

(1) G = Ground, I = Input, O = Output, P = Power

Copyright © MetaWells Co., Ltd. All rights reserved.

Absolute Maximum Ratings

Parameter		Min	Max	Units
Input	VIN, EN to GND	-0.3	42	V
	FB to GND	-0.3	5.5	
	PG to GND	-0.3	6	
	BST to SW	-0.3	5.5	
Output	VCC to GND	-0.3	6	V
	SW to GND	-0.3	42	
T_J	Junction temperature	-40	150	°C
T_S	Storage temperature	-55	150	

Recommended Operating Conditions

Parameter		Min	Max	Units
Buck Regulator	VIN	3.0	36	V
	SW		36	
	FB	0	5	
Control	EN	0	VIN	V
	PG	0	5	
Output	VOUT	0	24	V
T_J	Junction temperature	-40	125	°C

ESD Ratings

Symbol	Definition	Value	Units
V_{ESD}	HBM	±2000	V
	CDM	±2000	

Copyright © MetaWells Co., Ltd. All rights reserved.

Electrical Characteristics

Limits apply over the recommended operating junction temperature -40°C to +125°C, unless otherwise stated. Minimum and Maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated the following conditions apply: V_{IN} = 12 V. V_{OUT} is converter output voltage.

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SD}	Shutdown Supply Current	V_{EN}=0V			8	μA
I_Q	Non-Switching Quiescent Current	V_{FB}=1.05V			20	μA
R_{DSON_H}	High Side MOSFET ON Resistance			105	190	mΩ
R_{DSON_L}	Low Side MOSFET ON Resistance			65	135	mΩ
I_{LKG_SW}	Switch Leakage	V_{EN}=0V,V_{SW}=12V			1	μA
I_{LIMIT_H}	High Side MOSFET Current Limit (1)		3.5	4.5	5.8	A
I_{LIMIT_L}	Low Side MOSFET Current Limit (1) (2)		2.8			A
f_{SW}	Switching Frequency		350	410	470	kHz
f_{FB}	Fold-Back Frequency	V_{FB}<700mV	210	280	350	kHz
D_{MAX}	Maximum Duty Cycle	V_{IN}=V_{OUT}=12V, I_{OUT}=1A	96	98.5		%
T_{ON_MIN}	Min. Turn On Time(2)			40		ns
V_{FB}	Feedback voltage		0.985	1.00	1.015	V
I_{FB}	Current into FB pin	V_{FB}=1V	-100		100	nA
V_{EN_H}	Enable High Threshold		1.185	1.235	1.285	V
V_{EN_L}	Enable Low Threshold		0.95	1.03	1.09	V
V_{EN_HYS}	Enable Hysteresis Threshold			205		mV
V_{EN_LKG}	Enable Pin Leakage Current	V_{EN}=2V		-0.6		nA
V_{IN_UV}	Under Voltage Lockout Thresholds	Rising Threshold		2.85	3.2	V
		Falling Threshold	2.2	2.65		V
		Hysteresis		200		mV
V_{CC}	Internal Power Supply	4V≤VIN, I_{LOAD}=0mA	3.32	3.5	3.68	V
	VCC Load Regulation	4V≤VIN, I_{LOAD} =5mA		1.5	3	%
Tss	Internal Soft-Start Time		2	5	9	ms
T_{SD}	Thermal Shutdown			165		°C
T_{SD_HYS}				15		°C
V_{PG_R}	Power Good Threshold Rising	% of V_{FB}	91	94	97	%
V_{PG_F}	Power Good Threshold Falling	% of V_{FB}	89	92	95	%
PG_{Vth_HYS}	PG Threshold Hysteresis	% of V_{FB}		2		%
t_{PG}	Power Good Glitch Filter Delay		40	130	160	μs
R_{PG}	PG Pull-Down Resistance	V_{EN}=4V		95	250	Ω
		V_{EN}=0V		85	200	
I_{LKG_PG}	PG Leakage Current				100	nA

(1) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.

(2) Derived from bench characterization. Not tested in production.

Copyright © MetaWells Co., Ltd. All rights reserved.

Functional Diagram

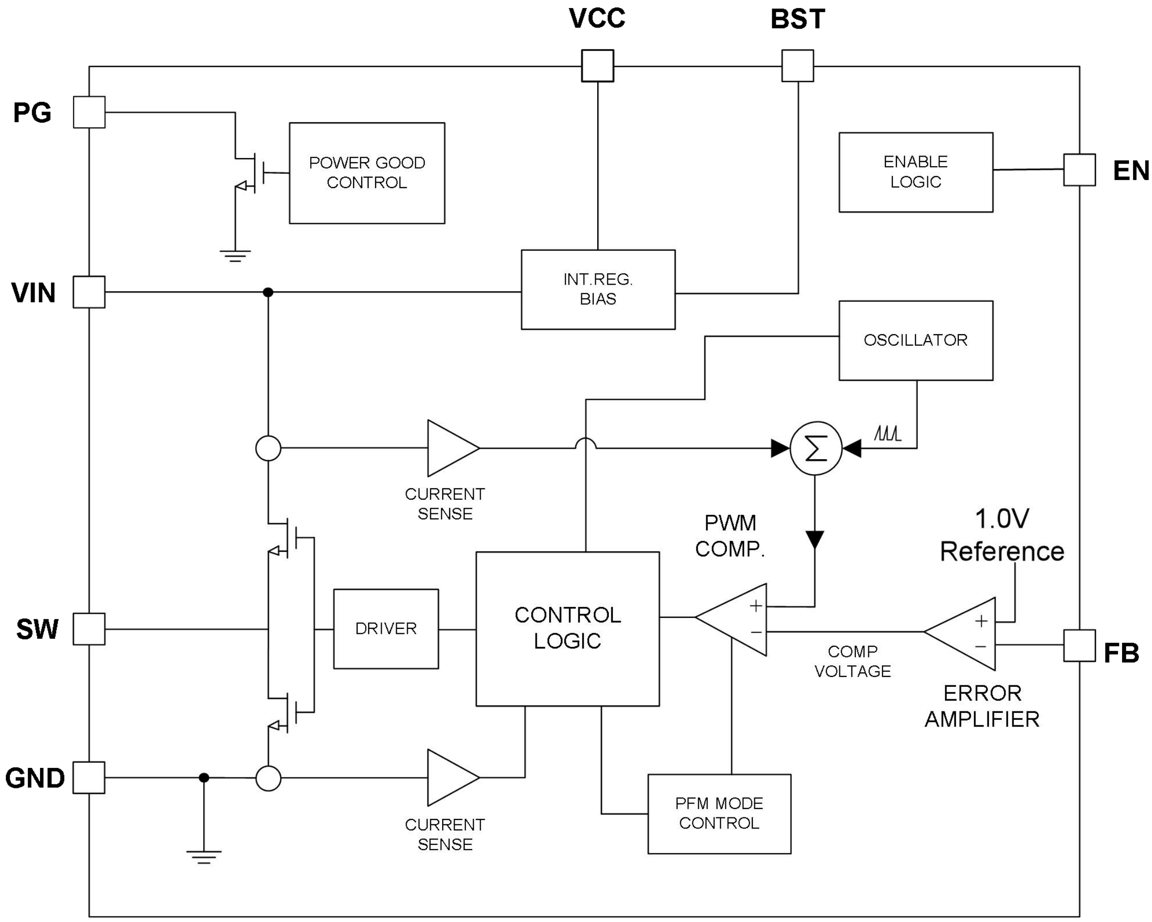


Fig.3 Functional Diagram

Copyright © MetaWells Co., Ltd. All rights reserved.

Typical Characteristics

Unless otherwise specified the following conditions apply: V_{IN} = 12V, f_{SW} = 410kHz, L = 10uH, C_{OUT} = 44uF, T_J =25°C

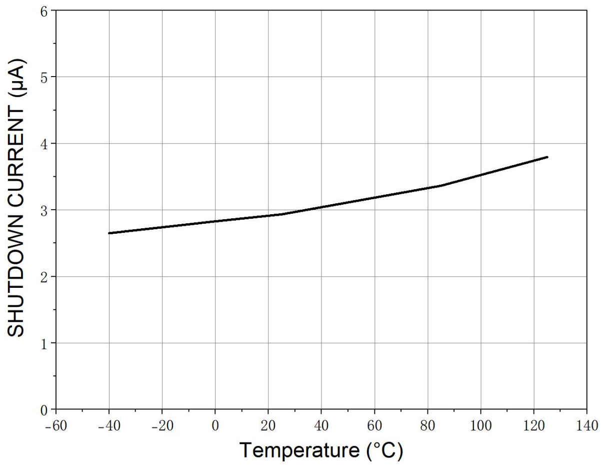


Fig.4 Shutdown Current vs. Junction Temperature

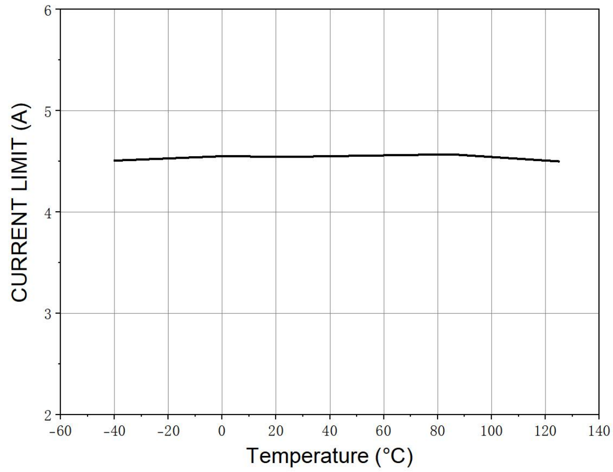


Fig.5 Current Limit vs. Junction Temperature at Duty = 40%

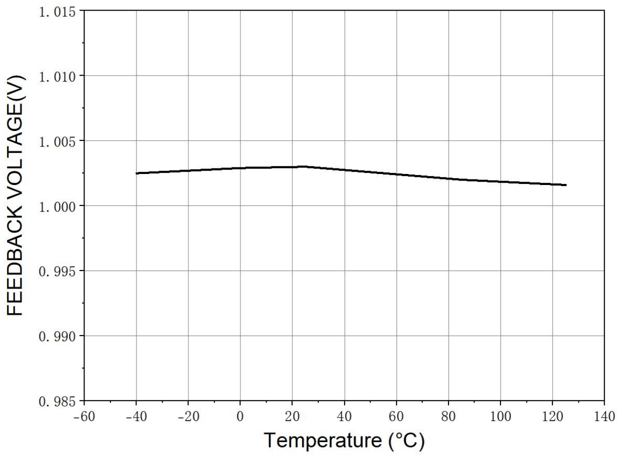


Fig.6 Feedback Voltage vs. Junction Temperature

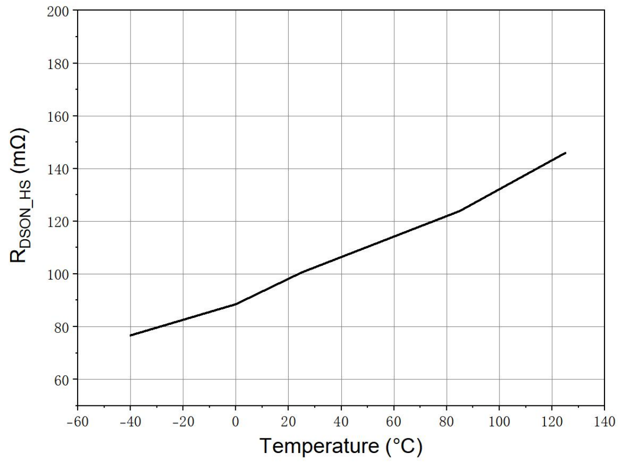


Fig.7 R_{DSON_HS} vs. Junction Temperature

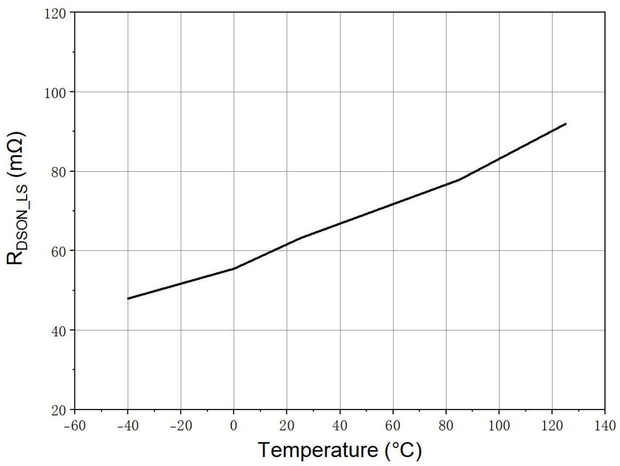


Fig.8 R_{DSON_LS} vs. Junction Temperature

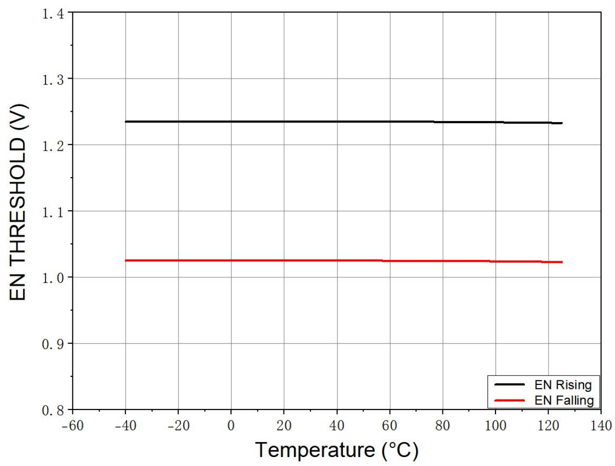


Fig.9 EN Threshold vs. Junction Temperature

Copyright © MetaWells Co., Ltd. All rights reserved.

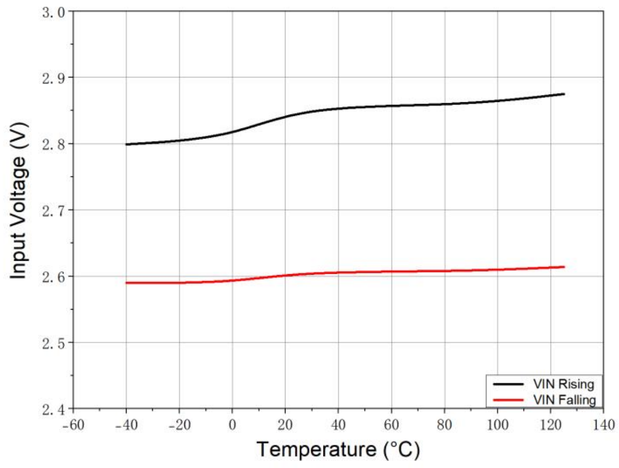


Fig.10 V_{IN} UVLO vs. Junction Temperature

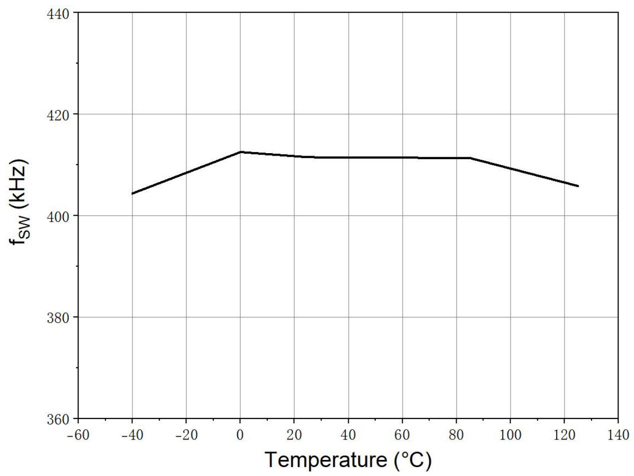


Fig.11 Switching Frequency vs. Junction Temperature

Copyright © MetaWells Co., Ltd. All rights reserved.

Product Overview

The PJ13943 is a synchronous, step-down, switching regulator with integrated high-side and low-side power MOSFETs. The PJ13943 can provide 3A of output current with very high efficiency from light load to full load. The PJ13943 features a wide input voltage from 3.0V to 36V, switching frequency 410 kHz. The internal soft start limits inrush current during power on. The PJ13943 also integrated compensation circuit inside the chip to simplify the loop design. Another highlighted feature is Its very low operational quiescent current which makes it suitable for battery powered applications.

Light Load Operation

The PJ13943 utilizes advanced Pulse Frequency Modulation (PFM) control to improve efficiency in light load working condition. When the loading current decreases, the device approaches discontinuous conduction mode first and the COMP voltage decreases accordingly. The low-side power switch is turned off when the zero current detection is triggered to improve system efficiency. When the COMP voltage drops to the low clamped threshold voltage, the device will skip pulse and decrease switching frequency by extend the non-switching period. During this period, the output voltage decreases due to load current or capacitor discharge. The high-side power switch will resume to turn on once the COMP voltage is higher than the threshold. The device will try to obtain few switching pulses with minimum peak inductor current to reduce the output ripple and the COMP voltage will drop to the clamped value again and trigger another non-switching period.

Precision Enable and Shutdown

The PJ13943 uses the EN pin to implement start-up and shutdown conditions. This input pin features a precision analog threshold of 1.235V. When the voltage on the EN pin is greater than 1.235V, the converter turns on; when the voltage falls below 1.03V, the converter shuts down. Note that the EN voltage must never exceed VIN, otherwise the device will enter test mode. Additionally, no capacitor should be connected between the EN pin and GND.

Soft-Start with Pre-Biased Capability

The PJ13943 implements a soft-start circuits to prevent the inrush current during start up. The soft start time is fixed internally. When the start-up period begins, the output voltage slowly ramps up. The PJ13943 also supports a monotonic start-up with pre-biased loads. If output voltage is pre-biased to a certain value during start-up, the device disables switching for both high-side and low-side power switches until soft-start reference voltage exceeds the feedback voltage.

Over-Current Protection and Hiccup Mode

The PJ13943 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. If, during current limit, the voltage on the FB input falls below about 0.5 V due to a short circuit, the device enters into hiccup mode. In this mode, the device stops switching for about 30 ms and then goes through a normal re-start with soft start. If the short-circuit condition remains, the device runs in current limit for about 5 ms (typical) and then shuts down again. This cycle repeats as long as the short circuit-condition persists. This mode of operation helps reduce the temperature rise of the device during a hard short on the output. The output current is greatly reduced during hiccup mode. Once the output short is removed and the hiccup delay is passed, the output voltage recovers normally.

Copyright © MetaWells Co., Ltd. All rights reserved.

Low Drop-out Mode

As the duty cycle is increasing, where the input voltage approaches the output voltage level, the required off time of high-side power switch will approach its minimum off time. When the minimum off time is reached, the PJ13943 will automatically extend the high-side on time and reduce the switching frequency. The device can realize 98.5% max duty cycle in drop-out condition. In this condition, the dropout voltage difference between input and output is influenced by the on-resistance of power switch, the DCR of power inductor, and the maximum duty cycle achieved.

Minimum On Time

As the duty cycle is decreasing, where the conversion ratio is very low, the required on time of high-side power switch will approach its minimum on time. The PJ13943 features typical 40ns ultra-low minimum on time and can support smaller duty cycle for high frequency power systems. Also, the device can automatically reduce the switching frequency, when the minimum on time is reached.

Power Good

The device employs an open-drain output PGOOD signal to check whether the output voltage is operating within the normal range. The external pull up voltage resource is recommended to be less than 5V (such as VCC) with a 100kΩ resistor. Once the feedback voltage is within the 92% and 107% of internal reference voltage, the PGOOD pull-down will be disabled and pulled up by the externally resistor. Once the feedback voltage is lower than 92% or greater than 107% of internal reference voltage, the PGOOD will be pulled low. To prevent glitching both the upper and lower thresholds include about 2% of hysteresis. Also, if UVLO, over temperature protection or EN pin is pulled low, the PGOOD will be pulled low accordingly.

Copyright © MetaWells Co., Ltd. All rights reserved.

Application Information

Fig.12 shows a typical application circuit for the PJ13943. Thanks to the high integration in the PJ13943, the application circuit based on PJ13943 only need input capacitor, output capacitor, output inductor and feedback resistors which are needed to be selected based on applications specifications. Table 2 shows some typical external component values.

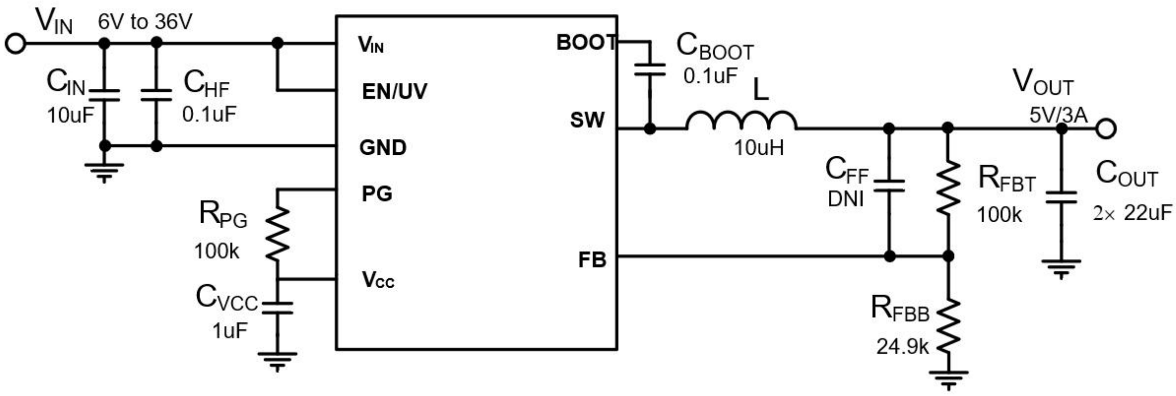


Fig.12 Typical Application Circuit (410kHz)

Table 2. Typical External Component Values

f_{sw}(kHz)	V_{OUT}(V)	L(μH)	C_{OUT}	R_{FBT}(kΩ)	R_{FBB}(kΩ)	C_{IN}+C_{HF}	C_{BOOT}	C_{VCC}	C_{FF}
410	3.3	10	2*22μF	100	43	10μF+100nF	100nF	1uF	DNI
410	5	10	2*22μF	100	24.9	10μF+100nF	100nF	1uF	DNI

Setting Output Voltage

The external feedback resistors connected to FB sets the output voltage. The feedback resistors value can be calculated with the below equation.

$$R_{FBB}=\frac{V_{REF}R_{FBT}}{V_{OUT}-V_{REF}}$$

While R_{FBT}=100kΩ, V_{REF}=1V, V_{OUT}=5V

Calculate R_{FBB}=24.9kΩ

Inductor Selection

For higher efficiency, choose an inductor with a lower DC resistance. A larger-value inductor results in less ripple current and a lower output ripple voltage, but also has a larger physical size, higher series resistance, and lower saturation current. A good rule for determining the inductor value is to allow the inductor ripple current to be approximately 20% to 40% of the maximum load current. The minimum inductance value can be calculated with the below equation.

$$L_{MIN}=\frac{V_{OUT}(1-D)}{f_{SW}\times\Delta I_L}$$

While V_{OUT}=5V, f_{SW}=410kHz, ΔI_L=30%×3A=0.9A, D=5V/12V=0.417

Calculate L=10uH.

Copyright © MetaWells Co., Ltd. All rights reserved.

Output Capacitor Selection

The output capacitor maintains the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. For best results, use low ESR capacitors to keep the output voltage ripple low. The output voltage ripple can be estimated with equation. Generally, required the output voltage ripple is less than 1% of the output voltage.

$$\Delta V_{OUT}=\frac{V_{OUT}\times(1-D)}{8\times f_{SW}^{2}\times L\times C_{OUT}}$$

Input Capacitor Selection

The input capacitor can be electrolytic, tantalum, or ceramic. When using electrolytic or tantalum capacitors, add a small, high-quality ceramic capacitor (like X7R,C0G etc.) as close to the IC as possible. When using ceramic capacitors, ensure that they have enough capacitance to provide a sufficient charge to prevent excessive voltage ripple at the input. From the below equation, can easily calculate the input voltage ripple. Generally, required the input voltage ripple is less than 10% of the input voltage.

$$\Delta V_{IN}=\frac{I_O\times D\times(1-D)}{f_{SW}\times C_{IN}}$$

C_{FF} Capacitor Selection

When some cases need improvement of load transient response or the margin of loop-phase, a feedforward capacitor can be used across R_{FBT}, especially when values of R_{FBT} > 1000kΩ are used. The minimum capacitation value can be calculated with the below equation

$$C_{FF}\leq\frac{C_{OUT}\times V_{OUT}}{110\times R_{FBT}\times\sqrt{\frac{R_{FBB}}{R_{FBT}+R_{FBB}}}}$$

Bootstrap Capacitor Selection

A bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the internal MOSFETs. A ceramic capacitor of 0.1uF and 16V voltage rating is required.

VCC Capacitor Selection

The VCC pin is the output of the internal LDO used to supply the control circuits of the converter. This output requires a ceramic capacitor connected from VCC to GND for proper operation. It is highly recommended placing a ceramic capacitor of 1uF and 16V voltage rating. In general, avoid loading this output with any external circuitry. However, this output can be used to supply the pullup for the PGOOD function. The nominal output voltage on VCC is 3.5V. Do not short this output to ground or any other external voltage. Also, if over temperature protection or EN pin is pulled low, the VCC pin output will be low.

EN Resistor Selection

The PJ13943 has undervoltage lockout feature with default rising threshold of 2.85 V. It can be adjusted by using EN pin with external resistor divider. The UVLO threshold integrates a 200mV hysteresis to make a desired hysteresis for input voltage.

V_{UVLO_R} is the desired system level undervoltage protection rising threshold voltage, V_{UVLO_F} is the desired system level undervoltage protection falling threshold voltage. The R_{ENT} and R_{ENB} value can be calculated with the below equation.

Copyright © MetaWells Co., Ltd. All rights reserved.

$$V_{UVLO\_R}=(\frac{R_{ENT}}{R_{ENT}+R_{ENB}})\times V_{ENR}$$

$$V_{UVLO\_F}=(\frac{R_{ENT}}{R_{ENT}+R_{ENB}})\times(V_{ENR}-0.2)$$

No capacitors should be placed between EN and GND, for preventing the chip from entering test mode.

Copyright © MetaWells Co., Ltd. All rights reserved.

Application Waveforms

Unless otherwise specified the following conditions apply: V_{IN} = 12V, V_{OUT} = 5V, f_{SW} = 410kHz, L=10uH, C_{OUT} =44uF, T_J =25°C.

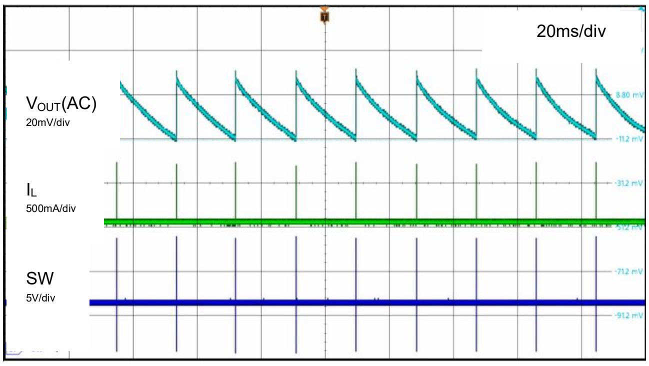


Fig.13 Steady State at I_{LOAD}=0A

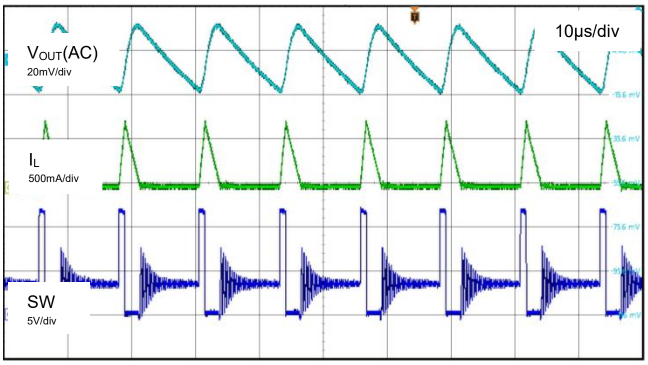


Fig.14 Steady State at I_{LOAD}=100mA

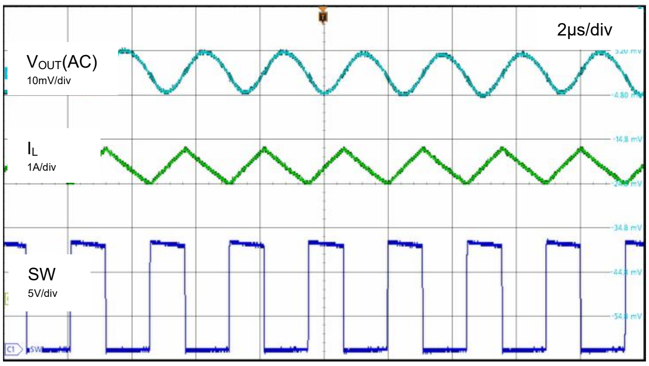


Fig.15 Steady State at I_{LOAD}=3A

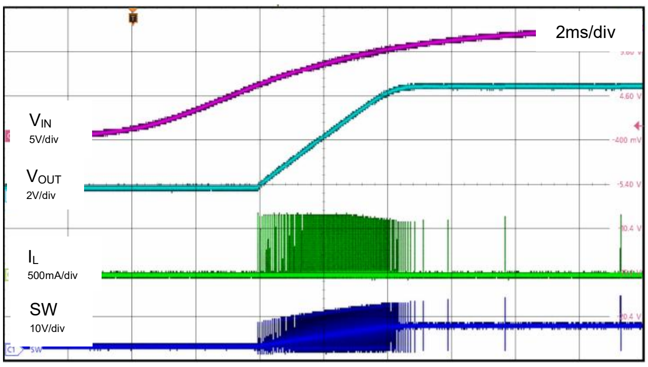


Fig.16 Startup through VIN at I_{LOAD}=0A

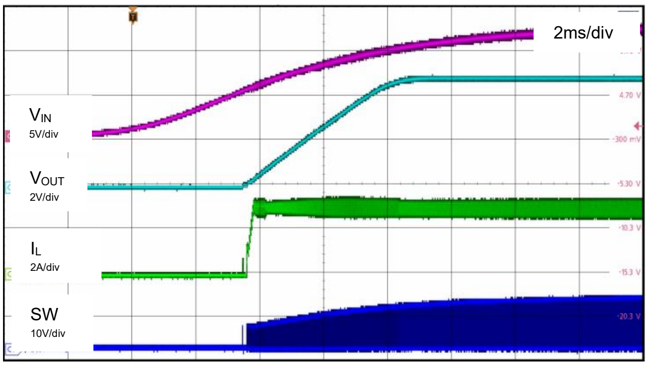


Fig.17 Startup through V_{IN} atI_{LOAD}=3A

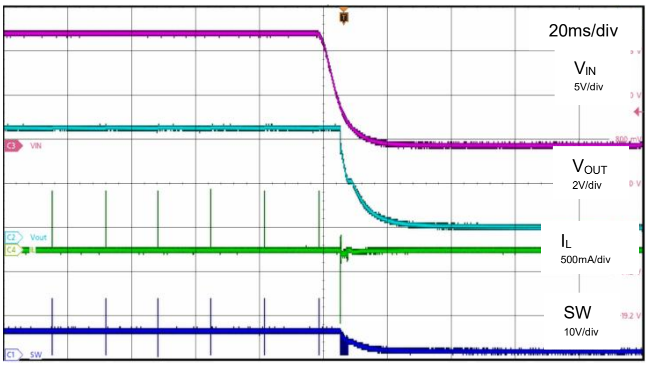


Fig.18 Shutdown through V_{IN} at I_{LOAD}=0A

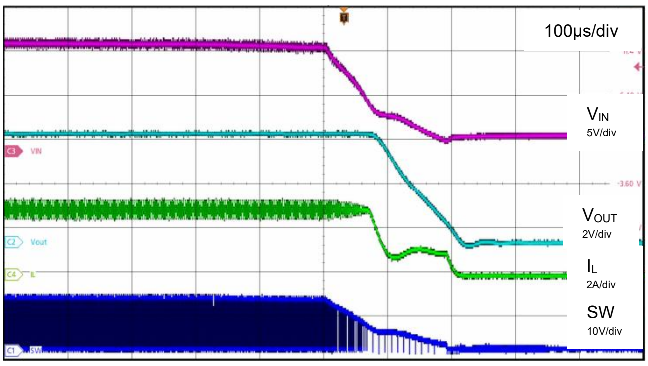


Fig.19 Shutdown through V_{IN} at I_{LOAD}=3A

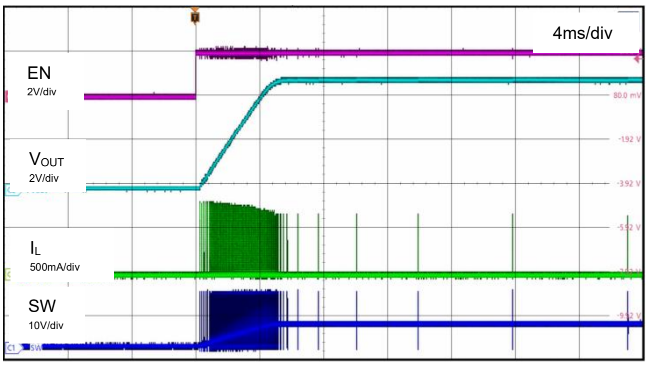


Fig.20 Startup through EN atI_{LOAD}=0A

Copyright © MetaWells Co., Ltd. All rights reserved.

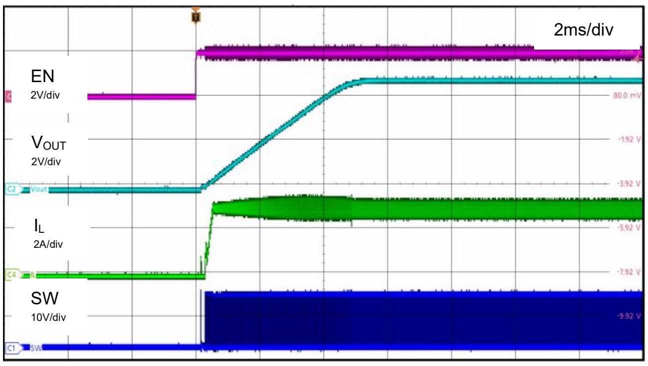


Fig.21 Startup through EN at I_{LOAD}=3A

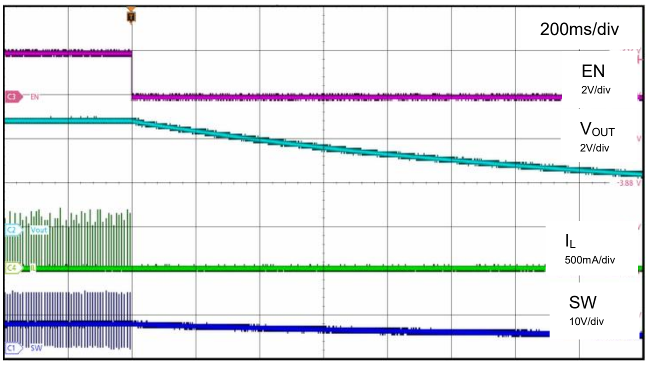


Fig.22 Shutdown through EN at I_{LOAD}=0A

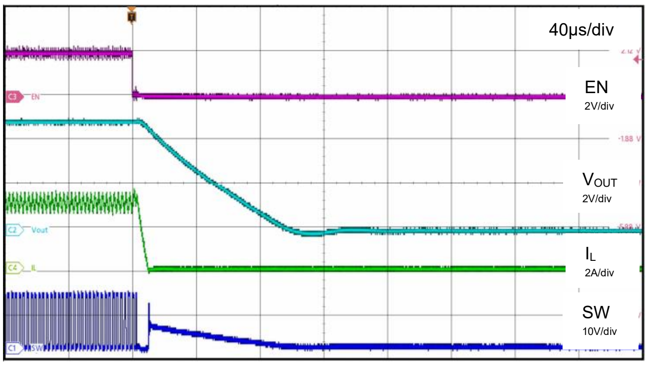


Fig.23 Shutdown through EN at I_{LOAD}=3A

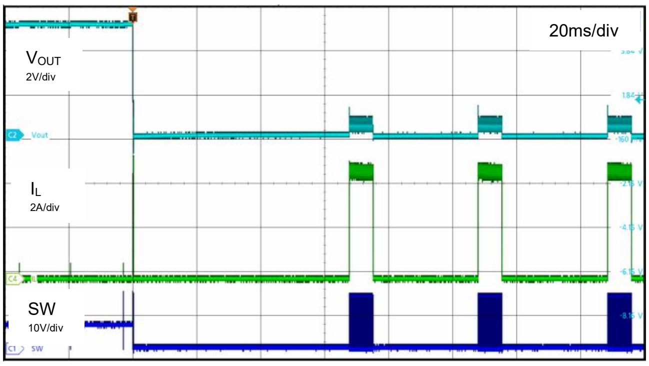


Fig.24 Short Circuit Protection at Io=0A

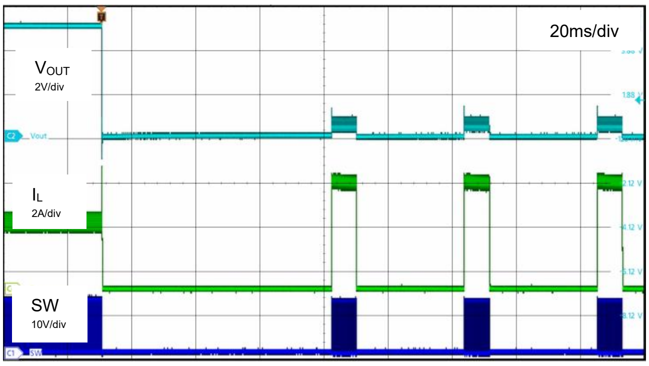


Fig.25 Short Circuit Protection at Io=3A

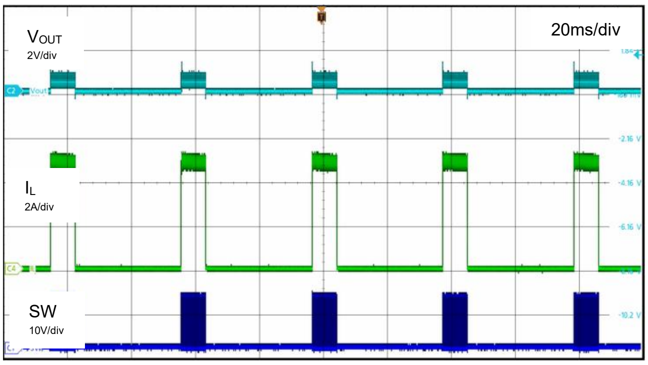


Fig.26 Short Circuit Steady

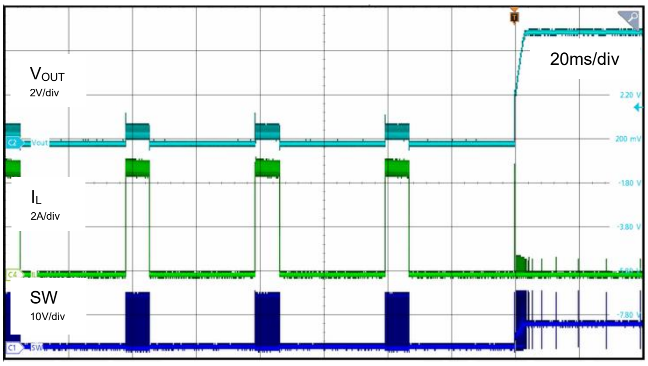


Fig.27 Short Circuit Recovery at Io=0A

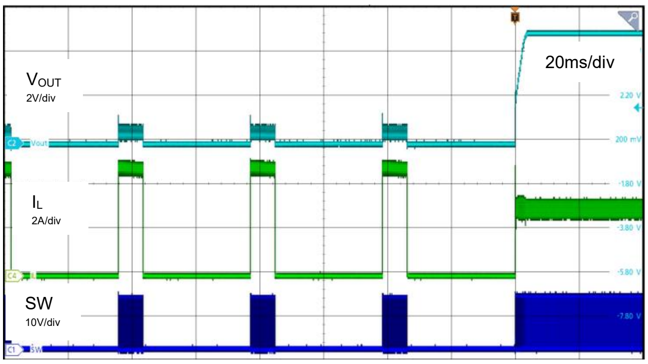


Fig.28 Short Circuit Recovery at Io=3A

Copyright © MetaWells Co., Ltd. All rights reserved.

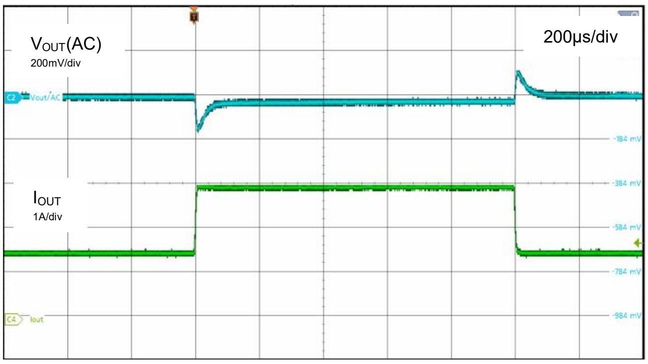


Fig.29 Load Transient at I_{LOAD} from 1.5A to 3A, 1.6A/μs

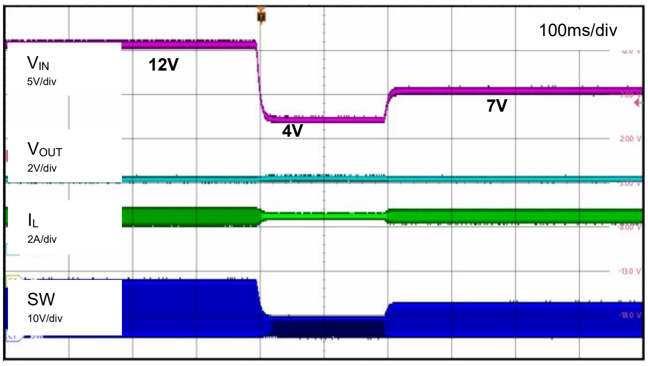


Fig.30 Cold-Crank at V_{OUT}=3.3V, I_{OUT}=3A

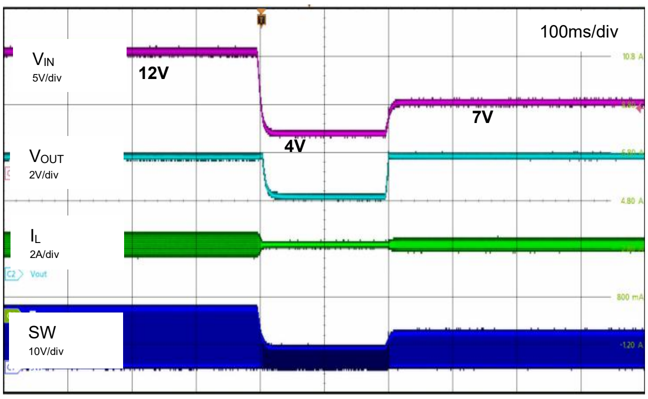


Fig.31 Cold-Crank at V_{OUT}=5V, I_{OUT}=3A

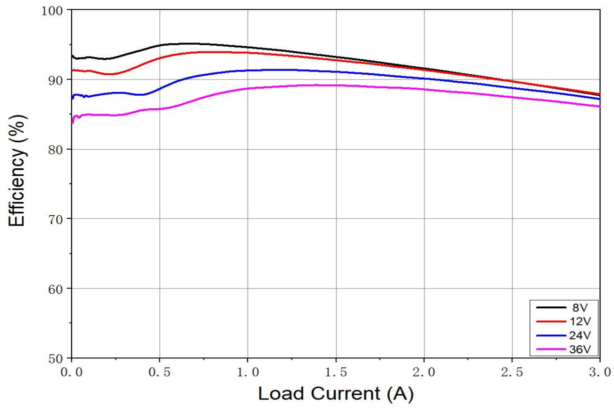


Fig.32 Efficiency VS. Load Current at V_{OUT}=3.3V

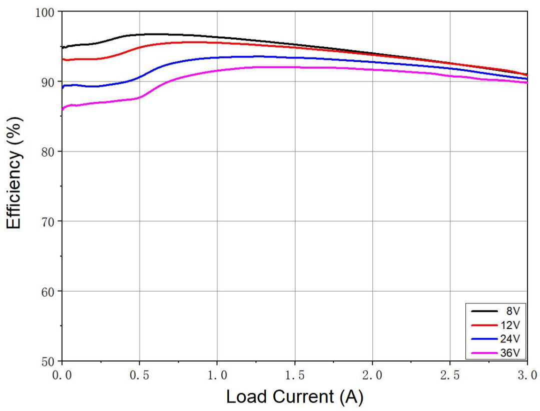


Fig.33 Efficiency VS. Load Current at V_{OUT}=5V

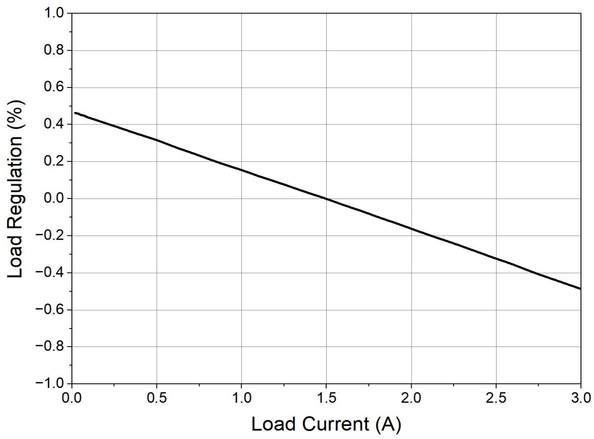


Fig.34 Load Regulation VS. Load Current at V_{IN}=12V

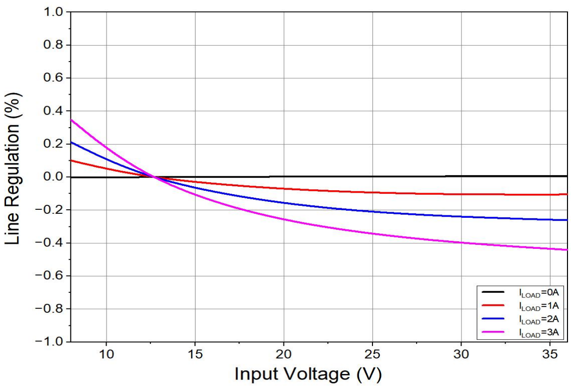


Fig.35 Line Regulation VS. Input Voltage at V_{OUT}=5V

Copyright © MetaWells Co., Ltd. All rights reserved.

PCB Layout Guidelines

PCB layout is critical for stable operation of switching regulator PJ13943, especially for thermal design and EMI design. For best results, please refer to Fig. 36 and follow the guidelines below.

1. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible.
2. Make sure top switching loop with power have lowest impendence of grounding.
3. Use a large ground plane to connect to GND directly. And add vias near GND.
4. Output inductor should be placed close to the SW pin to minimize the SW area.
5. The FB terminal is sensitive to noise so the feedback resistor should be located as close as possible to the IC.
6. Keep the connection of the input capacitor and VIN as short and wide as possible.

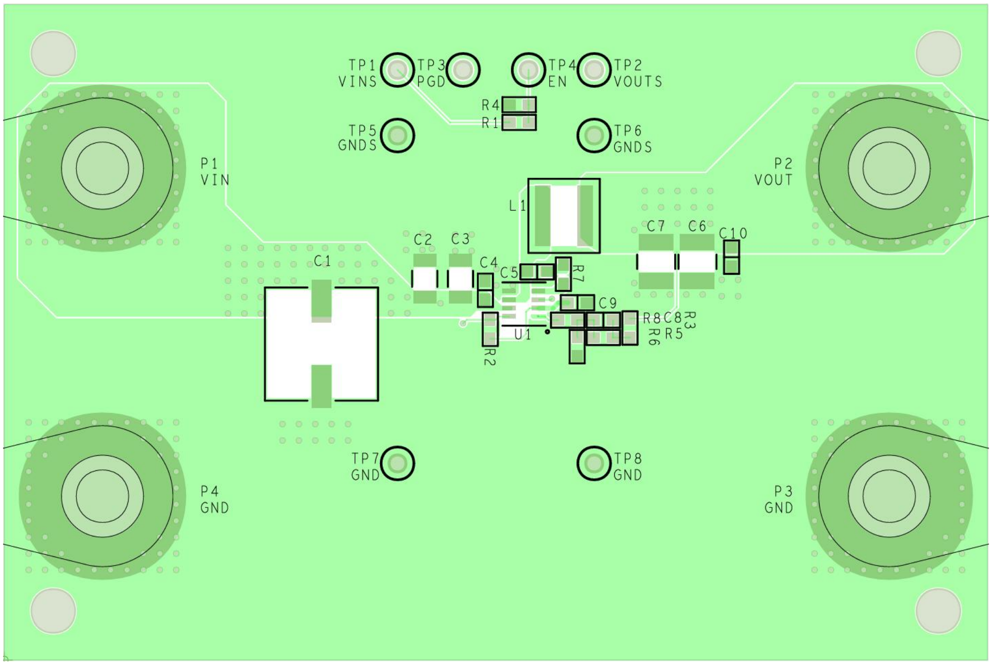


Fig.36 Layout Example

Copyright © MetaWells Co., Ltd. All rights reserved.

Package Information

Tape and Reel Information

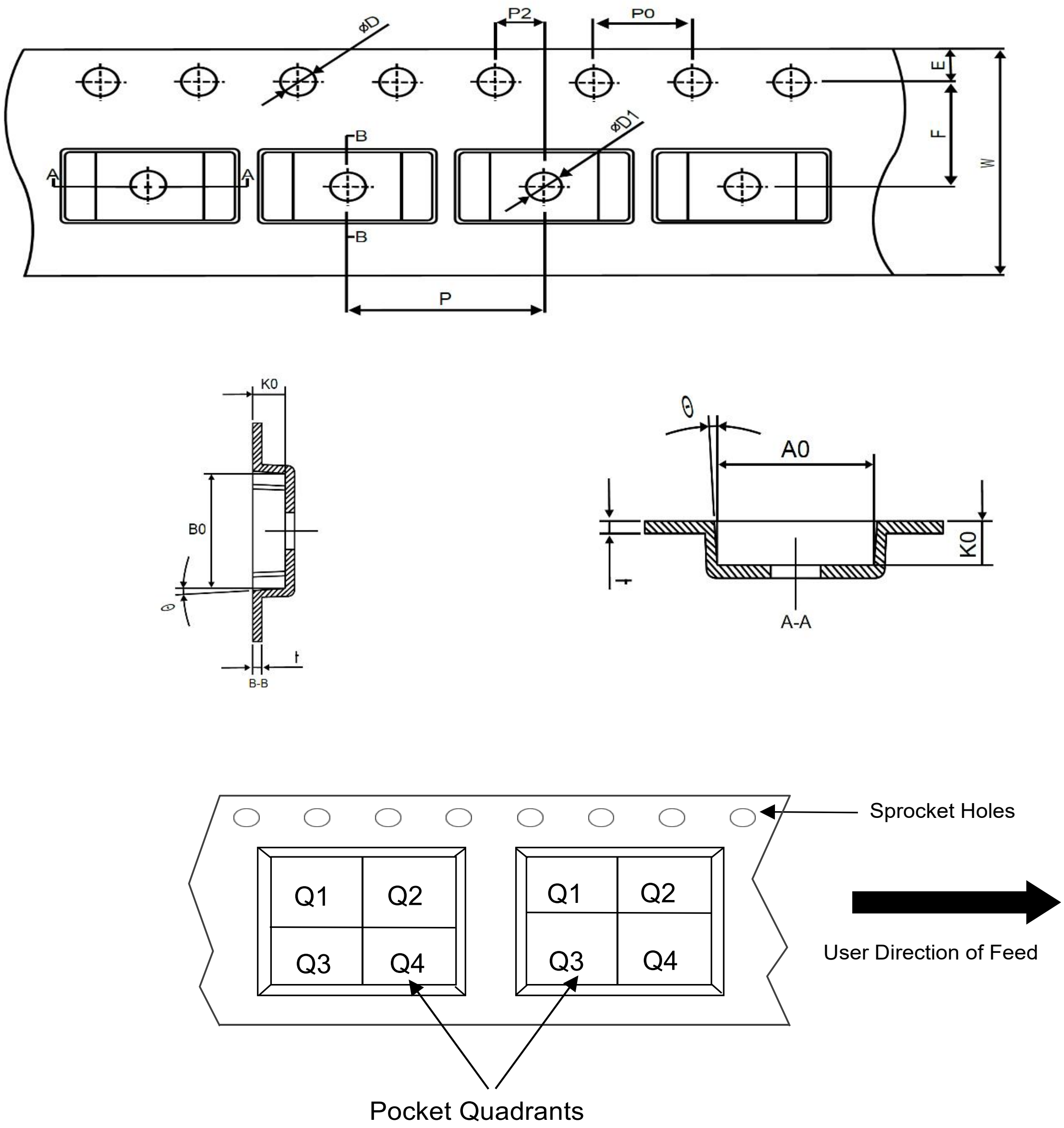


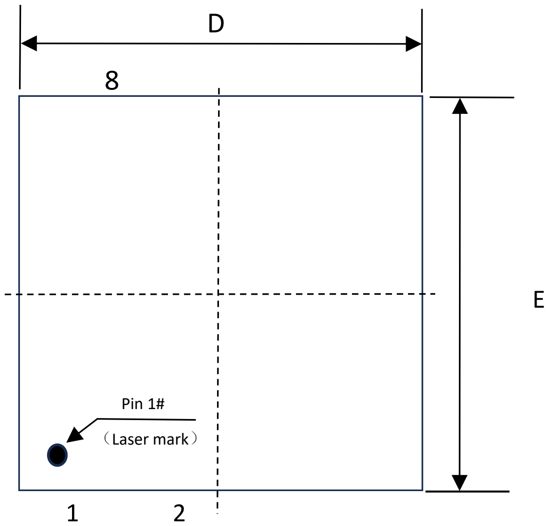
Fig.37 TAPE and Reel Information

Device	Package Type	A0 (mm)	B0 (mm)	K0 (mm)	P (mm)	P0 (mm)	W (mm)	Pin1 Quadrant	Quantity
PJ13943	QFN3X3-8	3.30	3.30	1.10	8.00	4.00	12.00	Q1	3000

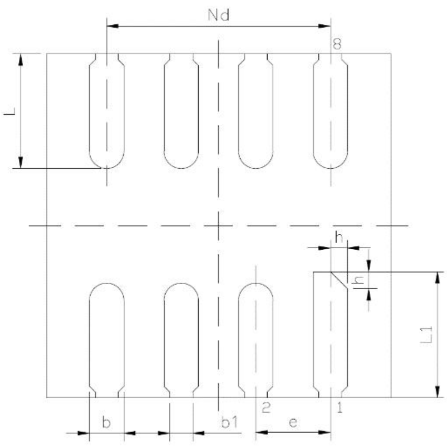
(1) All dimensions are nominal

Copyright © MetaWells Co., Ltd. All rights reserved.

Package Outlines



Top VIEW



BOTTOM VIEW

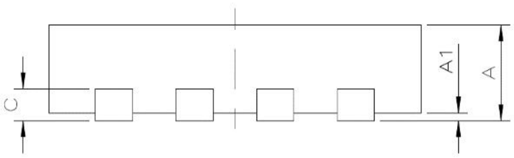


Fig.38 QFN3X3-8 Package

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.25	0.30	0.35
b1	0.20REF		
c	0.203REF		
D	2.90	3.00	3.10
e	0.65BSC		
Nd	1.95BSC		
E	2.90	3.00	3.10
e	0.65BSC		
L	0.90	1.00	1.10
L1	1.00	1.10	1.20
h	0.10	0.15	0.20

Copyright © MetaWells Co., Ltd. All rights reserved.

Version History

Version	Date	Changes
Rev.1.0	2026-04-22	Initial release

Copyright © MetaWells Co., Ltd. All rights reserved.

Disclaimer

MetaWells Co., Ltd. and all other MetaWells Co., Ltd. trademarks are the exclusive property of MetaWells Co., Ltd.. Any mention of additional trademarks or registered trademarks in this document is made in acknowledgment of their respective owners.

Without the consent of MetaWells Co., Ltd. , any modification to any part or subsection of the company's product specifications and datasheets is strictly prohibited in any form or manner. MetaWells Co., Ltd. reserves the rights to make changes of the content herein the document follow PCN procedure. Please refer to our website for latest document. It is recommended that customers obtain the latest version of relevant information and verify its timeliness and completeness before placing an order. All products are sold in accordance with the terms and conditions provided in the sales contract at the time of order confirmation, which includes warranty scope, intellectual property rights, and liability limitations.

During the sales period, MetaWells Co., Ltd. guarantees that the performance of the products will be in accordance with the company's standard warranty. The company utilizes testing and other quality control techniques to ensure the necessity to maintain this warranty. Except for government-mandated requirements, there is no need for special testing of measurement tables or other instruments.

Customers must acknowledge that our products are not intended or manufactured for use in life support systems or other high-risk activities or environments. The utilization of our products in such applications may lead to severe consequences, including personal injury, loss of life, property damage, or environmental harm. Our products are explicitly not warranted for deployment in high-risk activities, and we shall bear no responsibility towards customers or third parties for such usage.

MetaWells Co., Ltd. commits to providing technical support, assistance, advice, and information, in line with our current capabilities, including guidance related to the design, development, or debugging of purchased boards or other applications. However, we hereby disclaim all warranties concerning technical support, merchantability, or fitness for a particular purpose. We do not guarantee the error-free operation of boards or applications in conjunction with our support services, and we shall not be held liable for any consequences arising from the utilization of our support services.

Copyright© MetaWells Co., Ltd.

Website：www.metawells.com